AGH University of Science and Technology

SALT ver3 Simulations Update

Marek Idzik on behalf of AGH-UST

Faculty of Physics and Applied Computer Science
AGH University of Science and Technology

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Outline

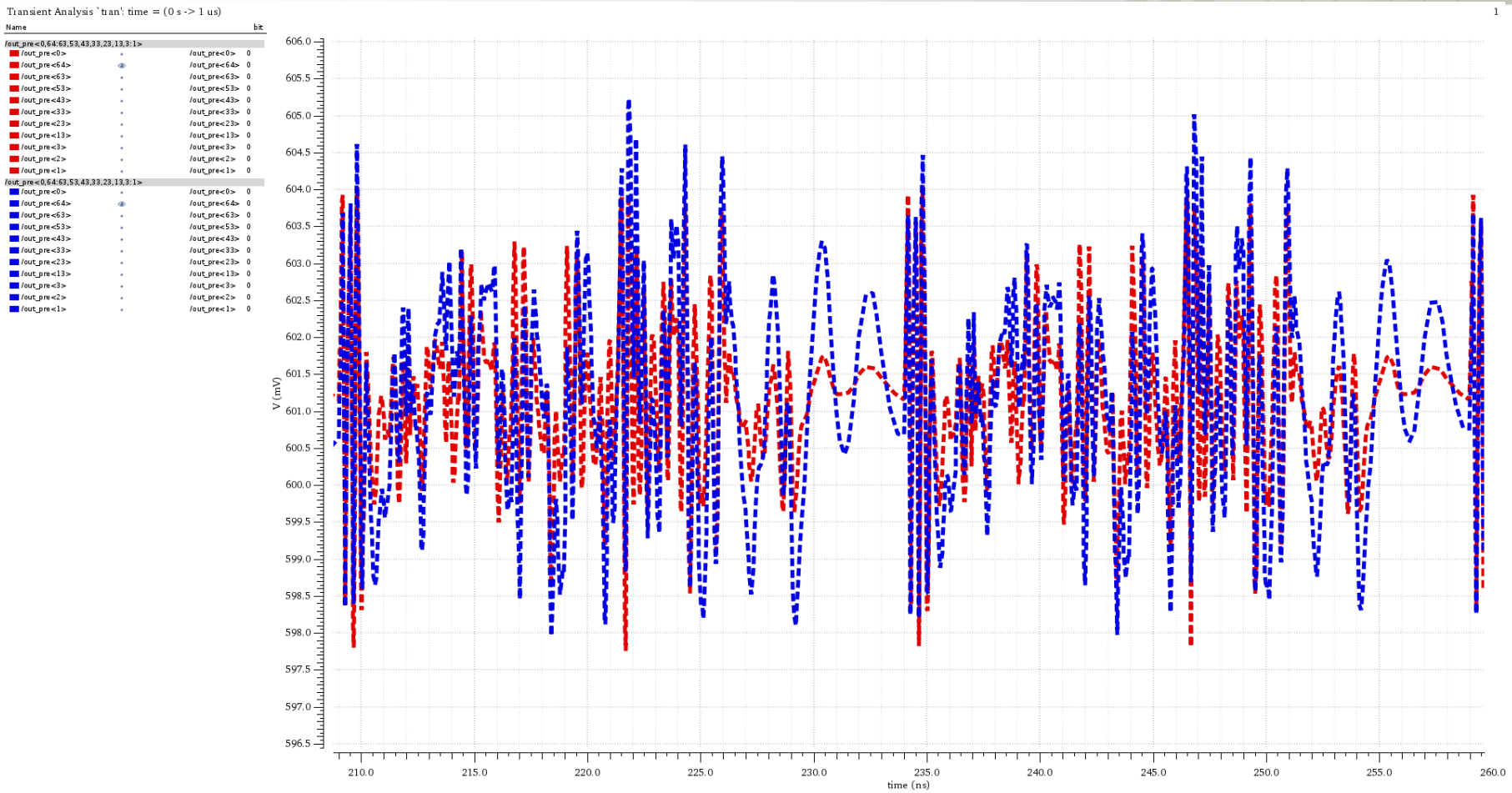
- In following slides simulations done for SALT3, which was submitted in October 2018, are shown
- In first slides the comparison of SALT ver3 and SALT ver3.1 is shown. By SALT3 we understand ver3.1. The only difference between ver3 and ver3.1 is small capacitance in the preamplifier, which was added to slow it down slightly, in order to eliminate the possibility of generation of 500-600MHz oscillations at the preamplifier output.

SALT3 - Simulations
Part I – 128 extracted channels

• Simulations shown in next slides were done for 128 channels (analog FE+ADC) on extracted RC or C level and with ideal power supply. To take into account parasitics:

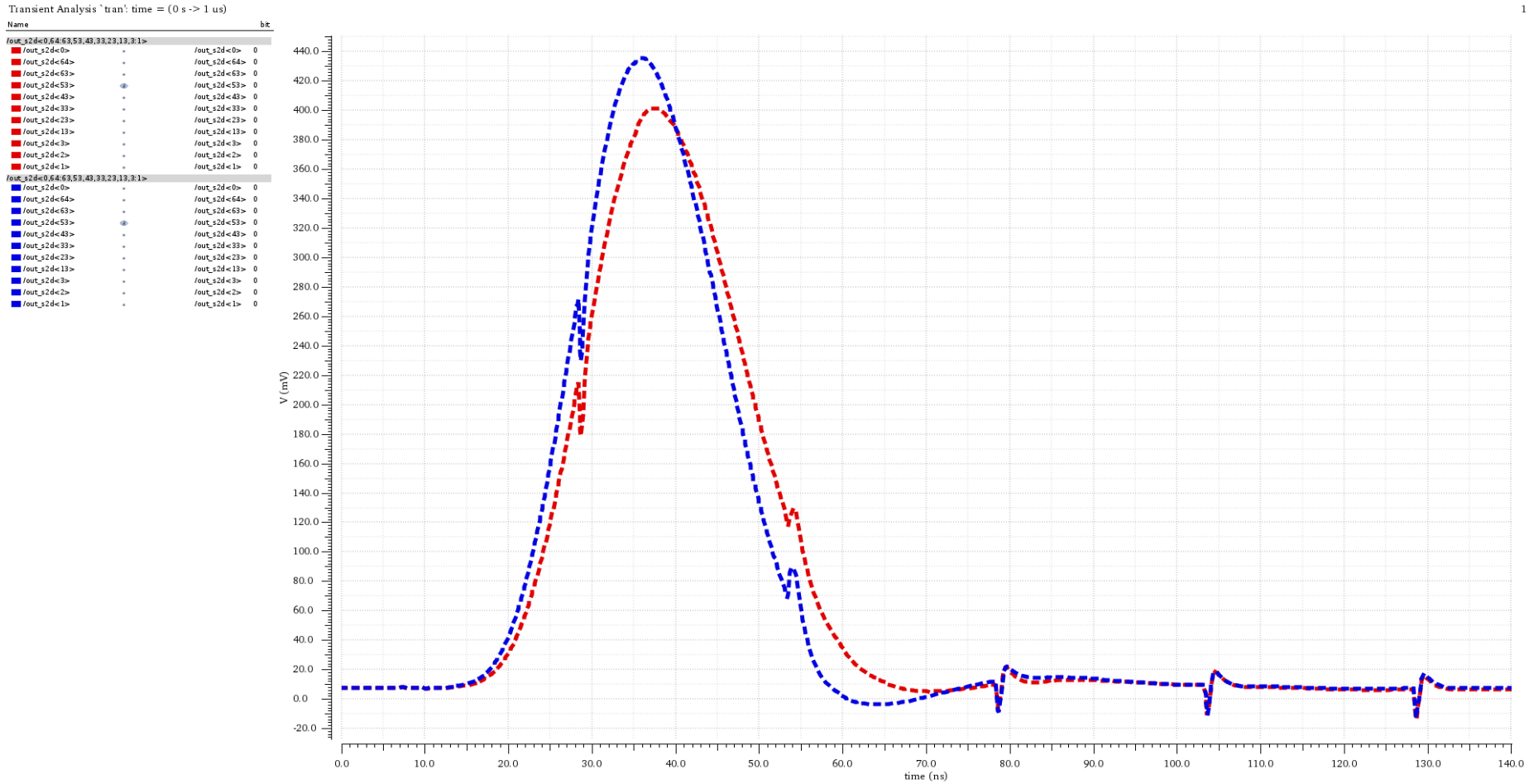
- We do not extract the whole SALT but only single channel (x 128) and biasing circuitry.
- The schematic L-R power distribution network is added between extracted channels
- Bond inductances are added between supply pads and ideal power supply

SALT3 simulation results – ext RC
Transient, Pre out v3 vs v3_1(slower preamp)



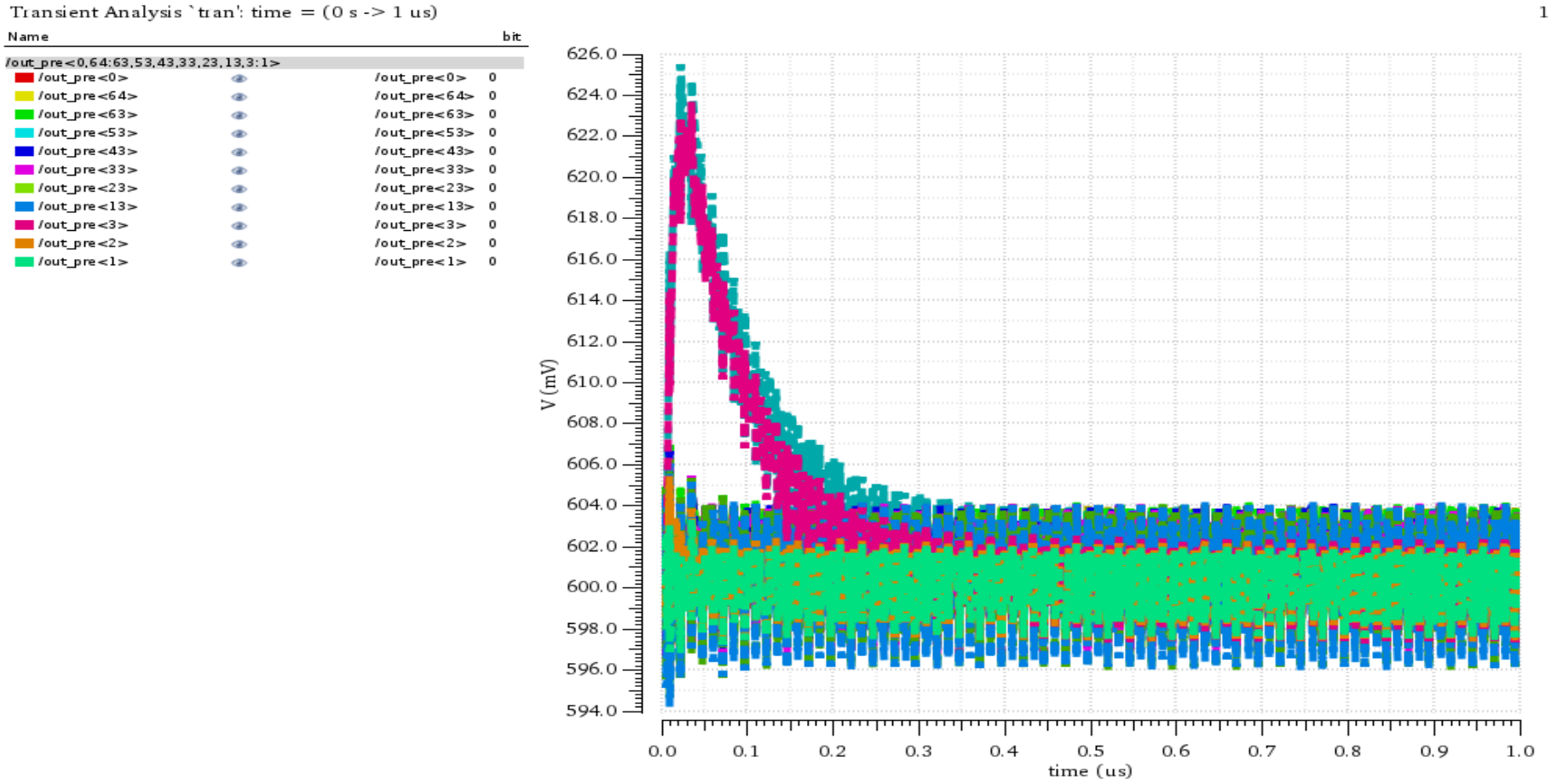
- ADC delay=7, default inductances (Lchan=1), Cchan_decADC=40pF
- Slower preamp (v3_1=red) more stable

SALT3 simulation results – ext RC
Transient, S2Dif out v3 vs v3_1(slower preamp)



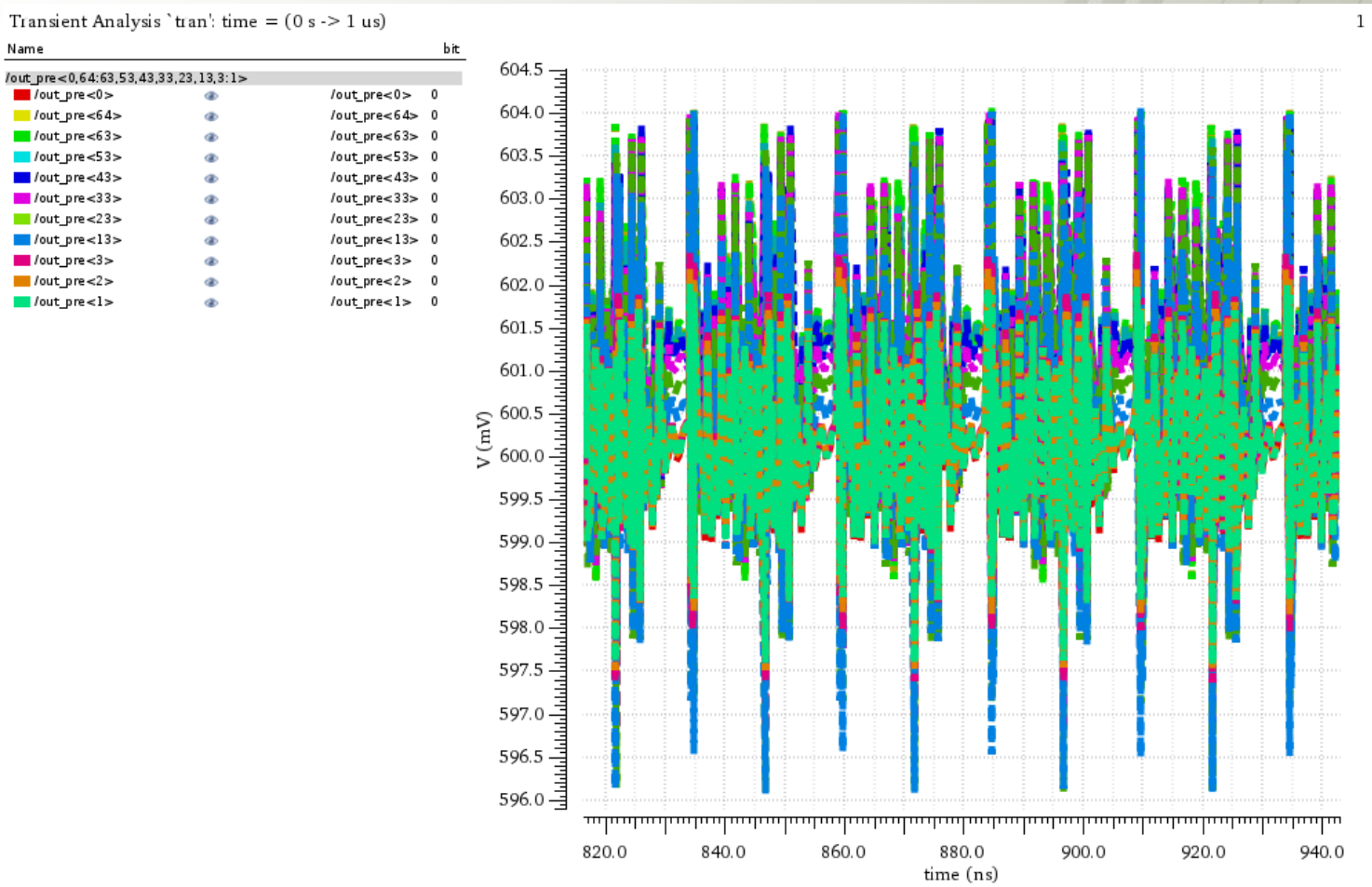
- ADC delay=7, default inductances (Lchan=1), Cchan_decADC=40pF
- Slower preamp (v3_1=red) gives slower pulse (Tpeak~34ns) but tail OK

SALT3 simulation results – ext RC
Transient, pre out v3_1(slower preamp)



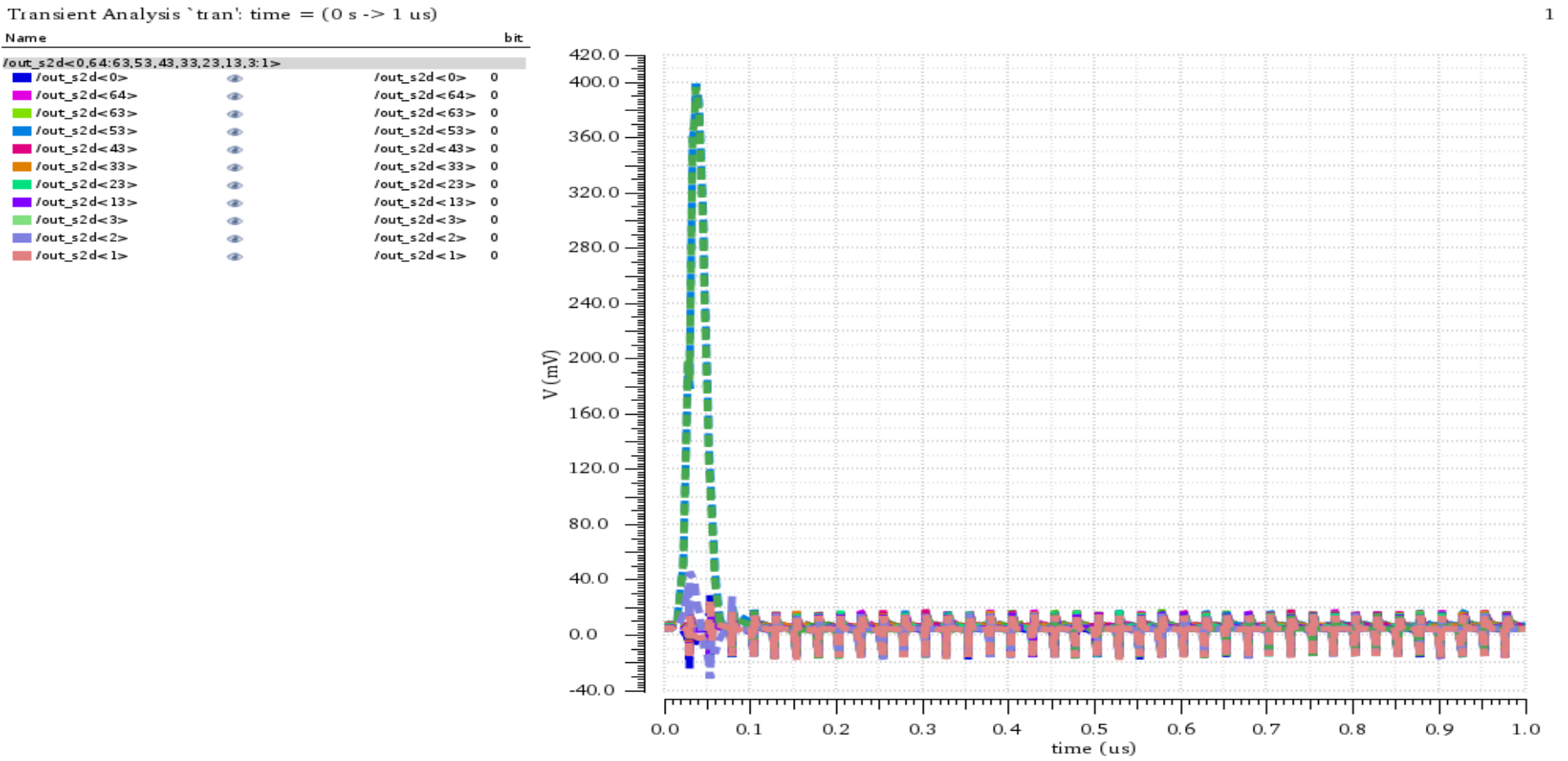
- ADC delay=7, default inductances (Lchan=1), Cchan_decADC=40pF

SALT3 simulation results – ext RC
Transient, pre out v3_1 baseline



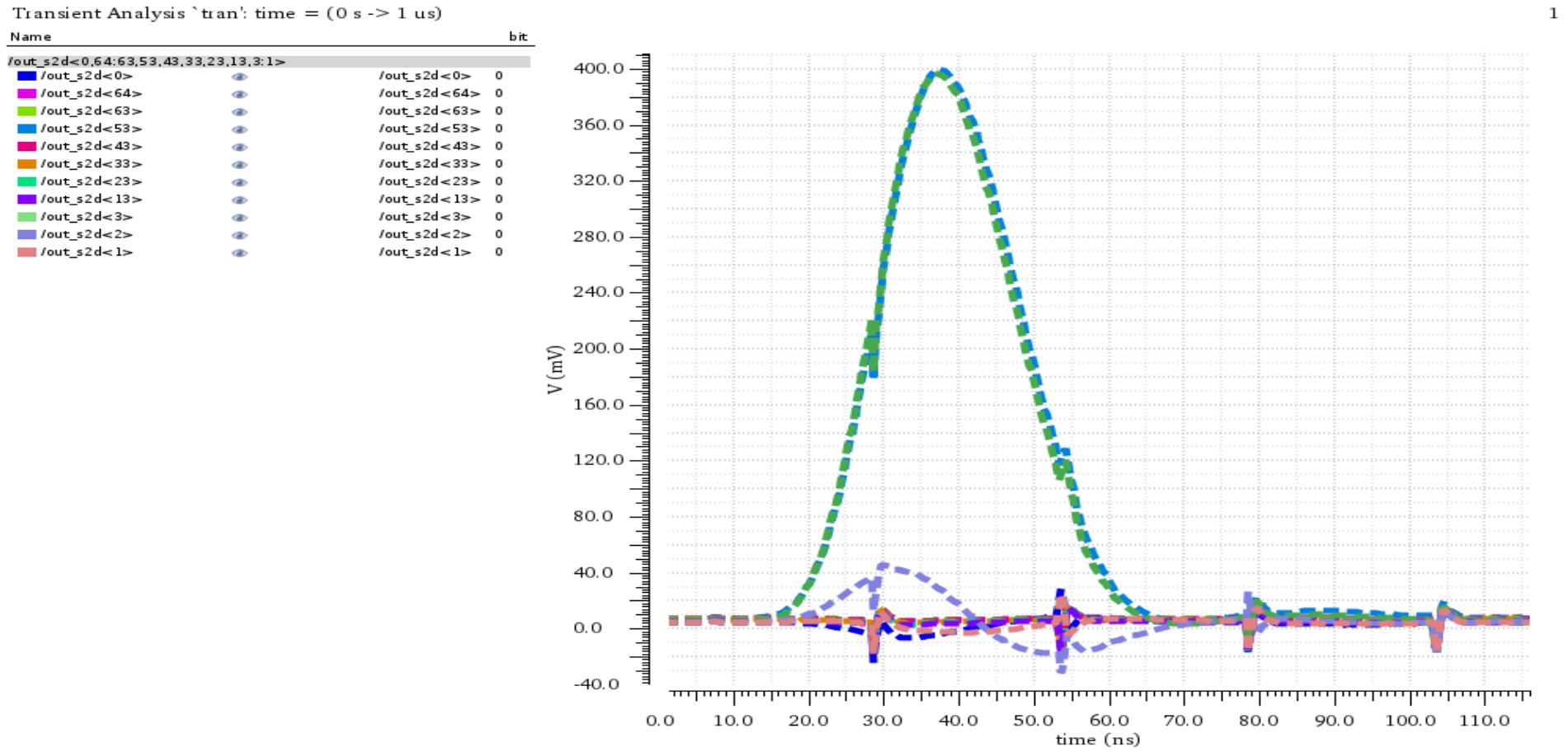
- ADC delay=7, default inductances (Lchan=1), Cchan_decADC=40pF

SALT3 simulation results – ext RC
Transient, S2D out v3_1



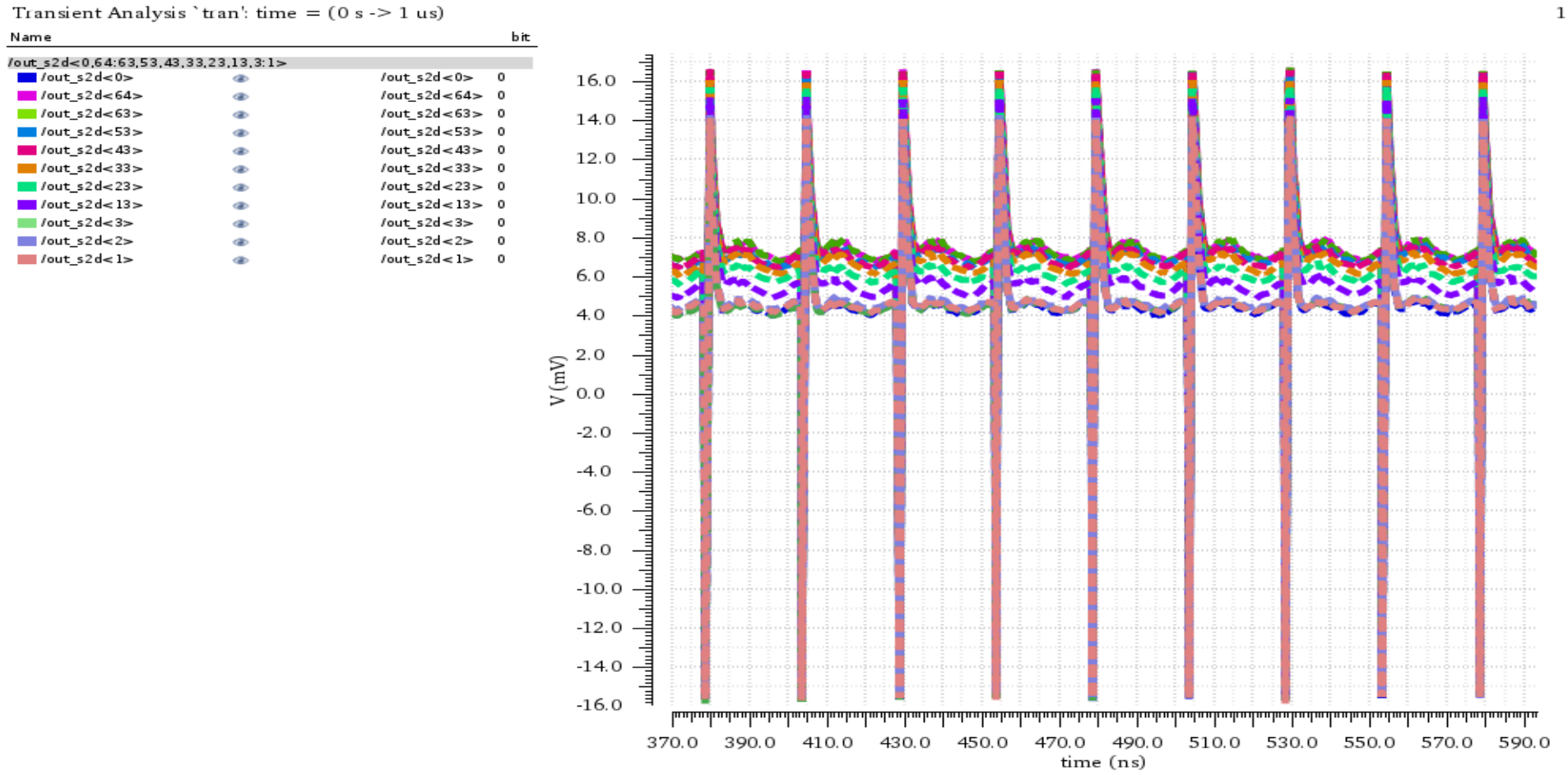
- ADC delay=7, default inductances (Lchan=1), Cchan_decADC=40pF

SALT3 simulation results – ext RC
Transient, S2D out v3_1, pulse shape



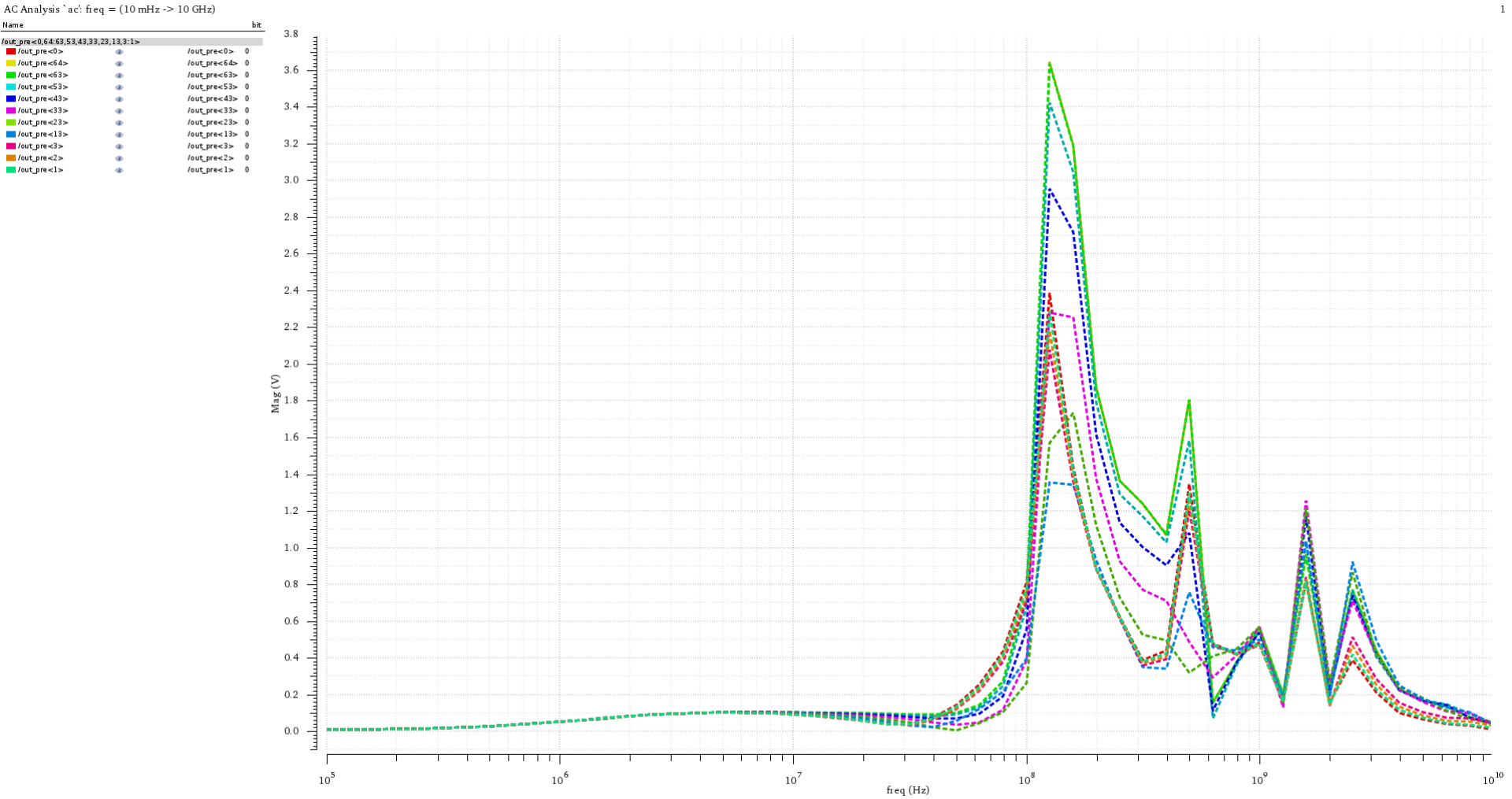
- ADC delay=7, default inductances (Lchan=1), Cchan_decADC=40pF

SALT3 simulation results – ext RC
Transient, S2D out v3_1, baseline



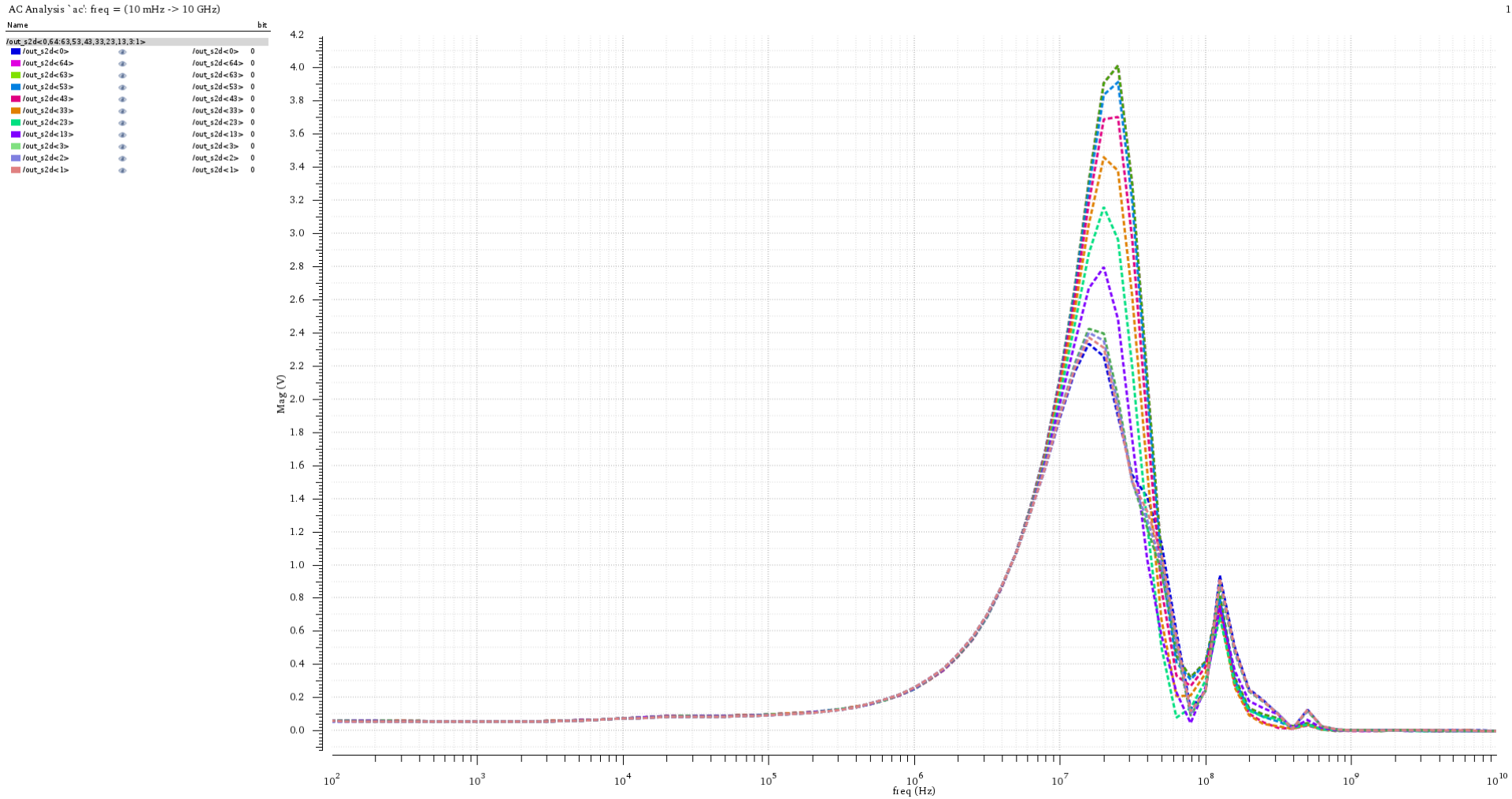
- ADC delay=7, default inductances (Lchan=1), Cchan_decADC=40pF

SALT3 simulation results – ext RC AC, pre out v3_1



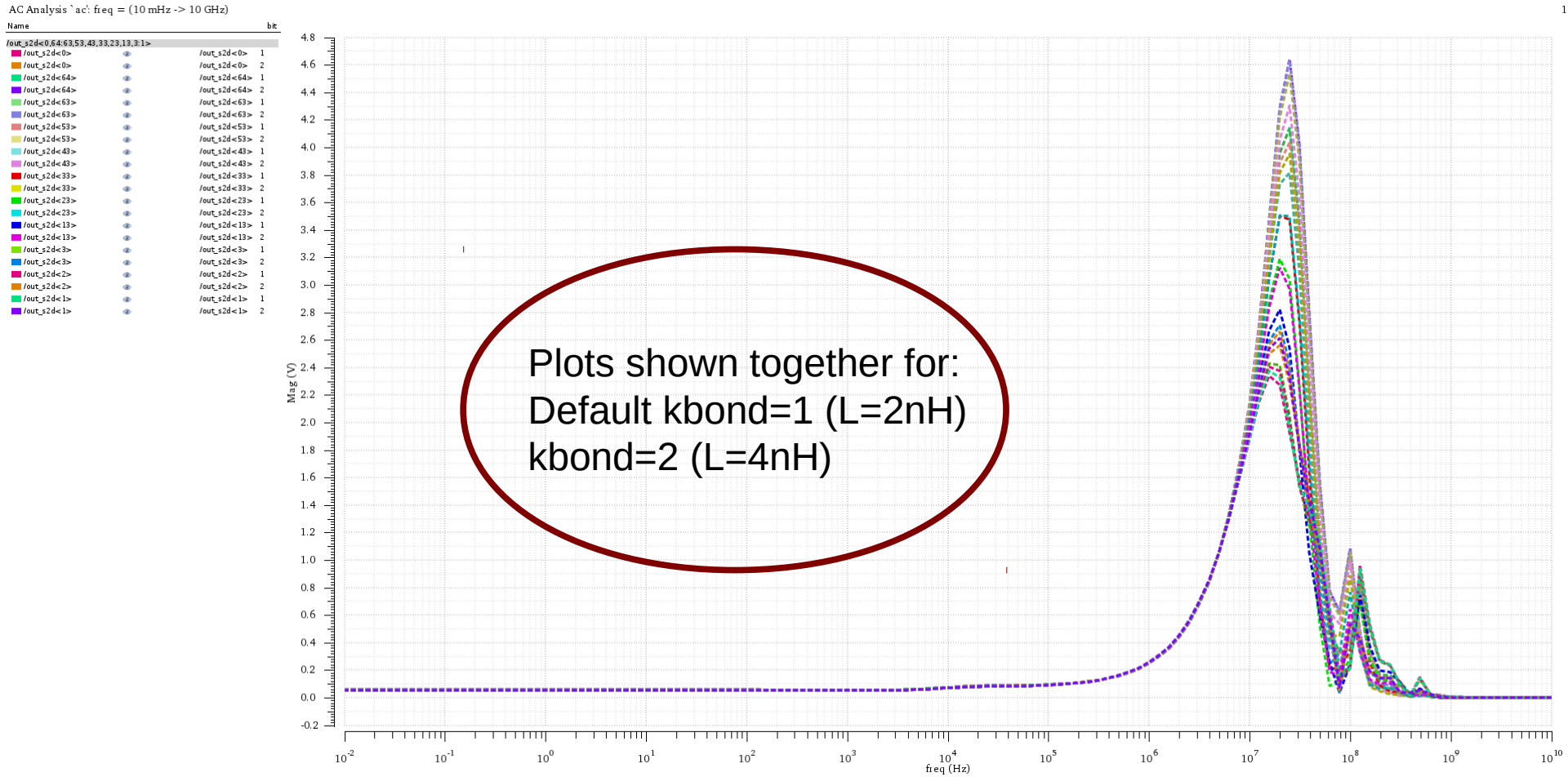
- @40MHz ~0.1, 1st peak@125MHz, 2nd peak@500MHz

SALT3 simulation results – ext RC AC, S2Diff out v3_1



- peak @25MHz, @40MHz<=2.1

SALT3 simulation results – ext C
AC, S2Diff out v3_1 versus bond inductance



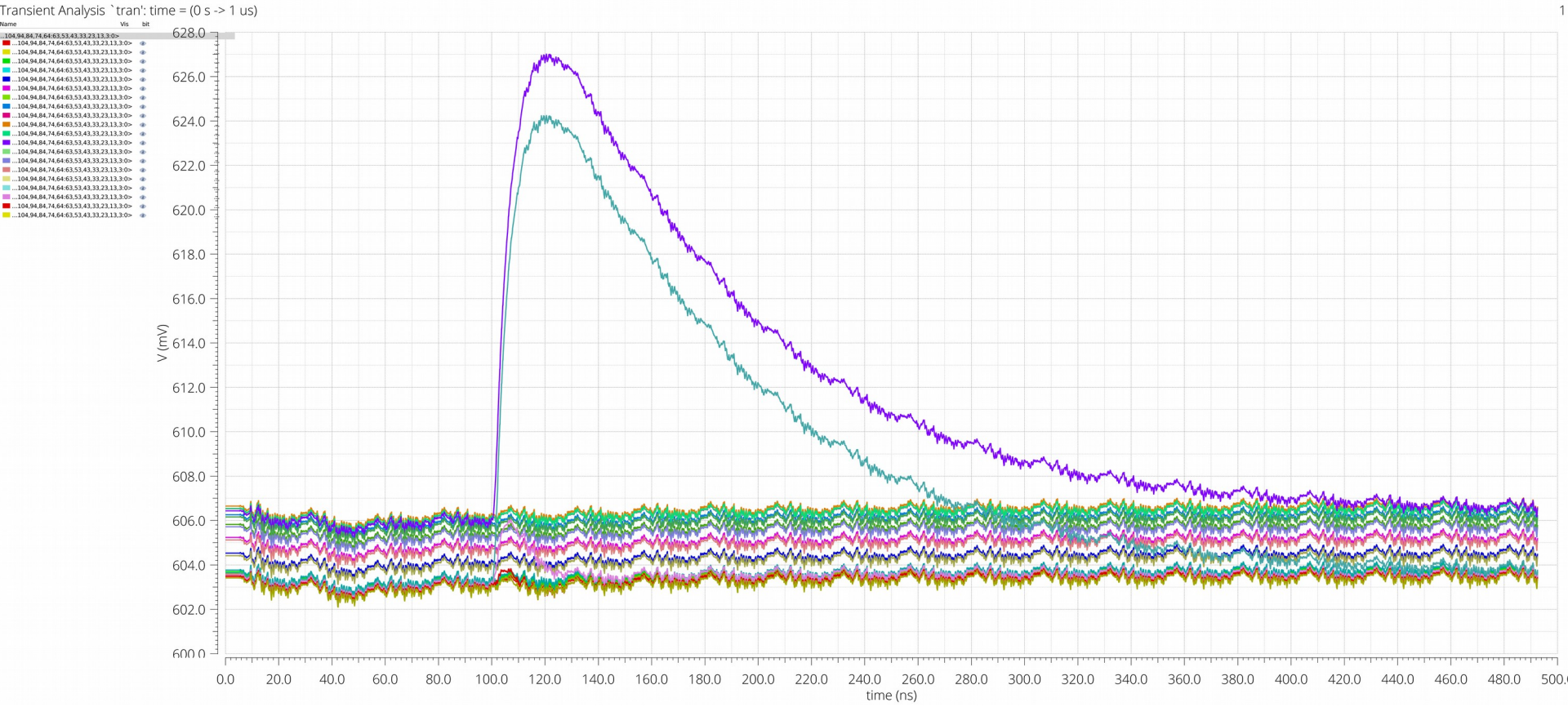
- For different channels double L bond causes ~15% worse PSRR

SALT3 - Simulations
Part II – complete mixed-mode SALT

• Simulations shown in next slides are done for the extracted view of the whole SALT (mixed-mode part), containing not only 128 channels but also the whole power distribution, monitoring circuitry etc… . Simulations are done on extracted RC or C level

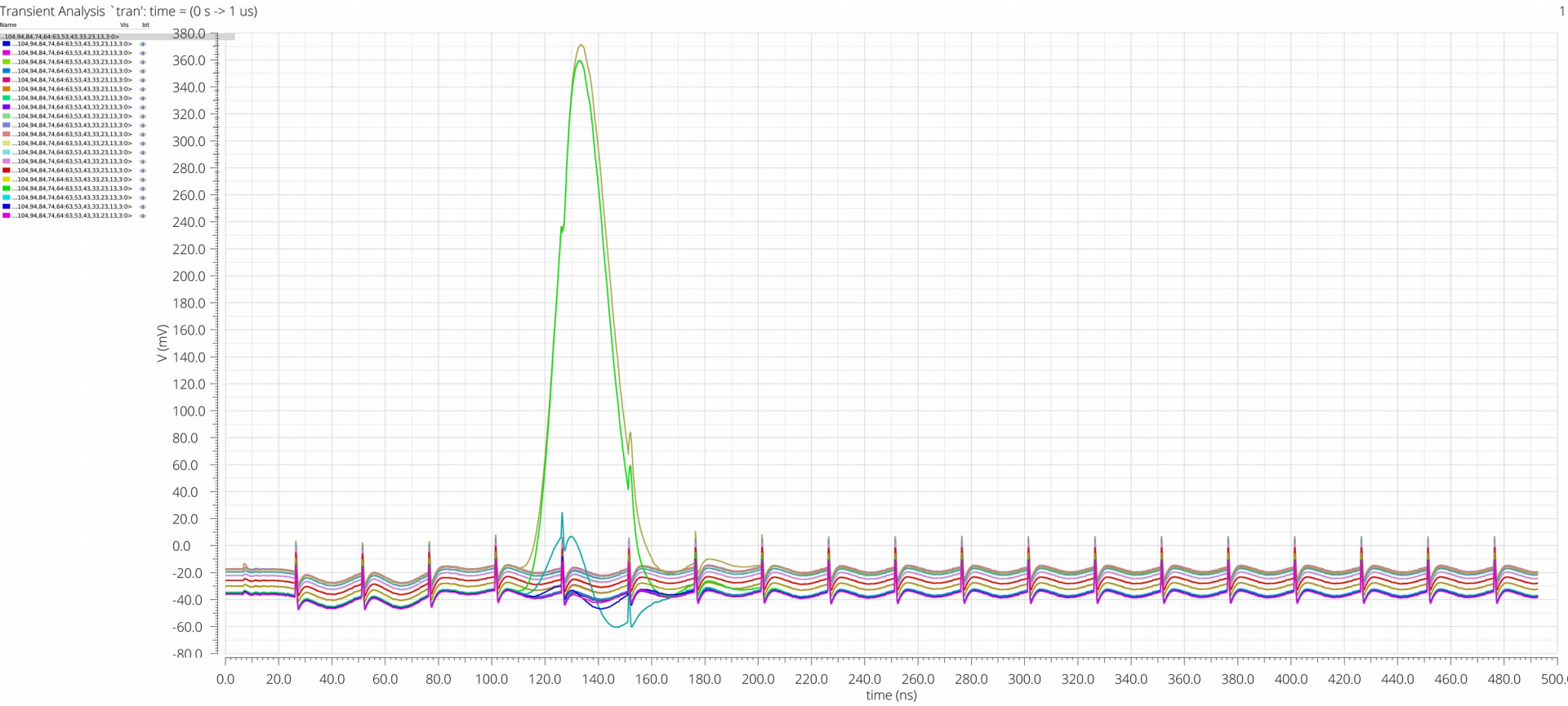
- Simulations on full extracted RC level were running at CERN
- Bond inductances are added, but internal chip inductances are not there - Cadence does only RC extraction…
- Since ADC power supply and decoupling will come from the digital mesh, in the simulations (done on mixed-mode part of SALT only) the ADC decoupling IS NOT present since it is not possible to add it realistically. It means that large ADC current fluctuations are not filtered in these simulations. For this reason results of transient simulations may be treated as the worst case.

SALT3 simulation results – ext RC Transient, pre out v3_1



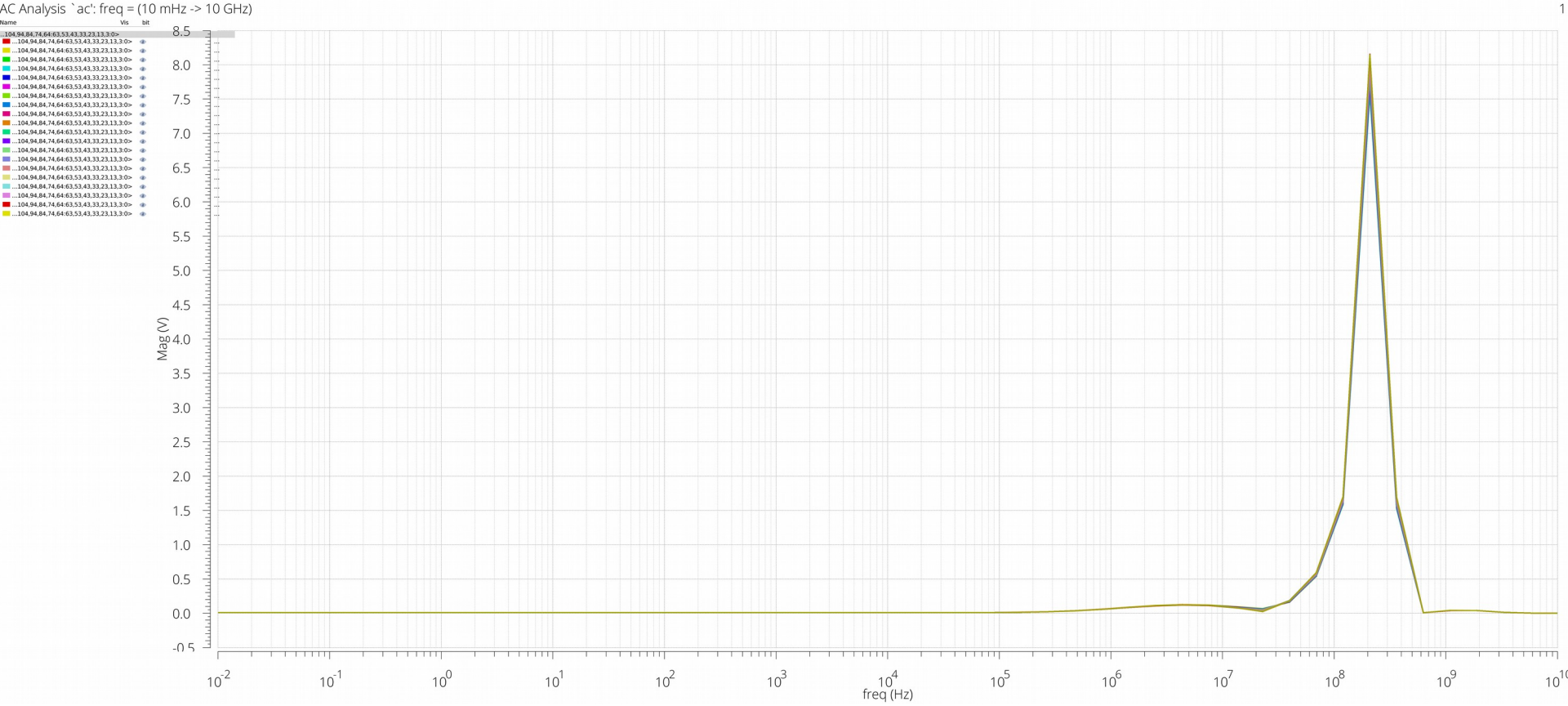
- ADC delay=4, No internal inductances, Cchan_decADC=0

SALT3 simulation results – ext RC Transient, S2Diff out v3_1



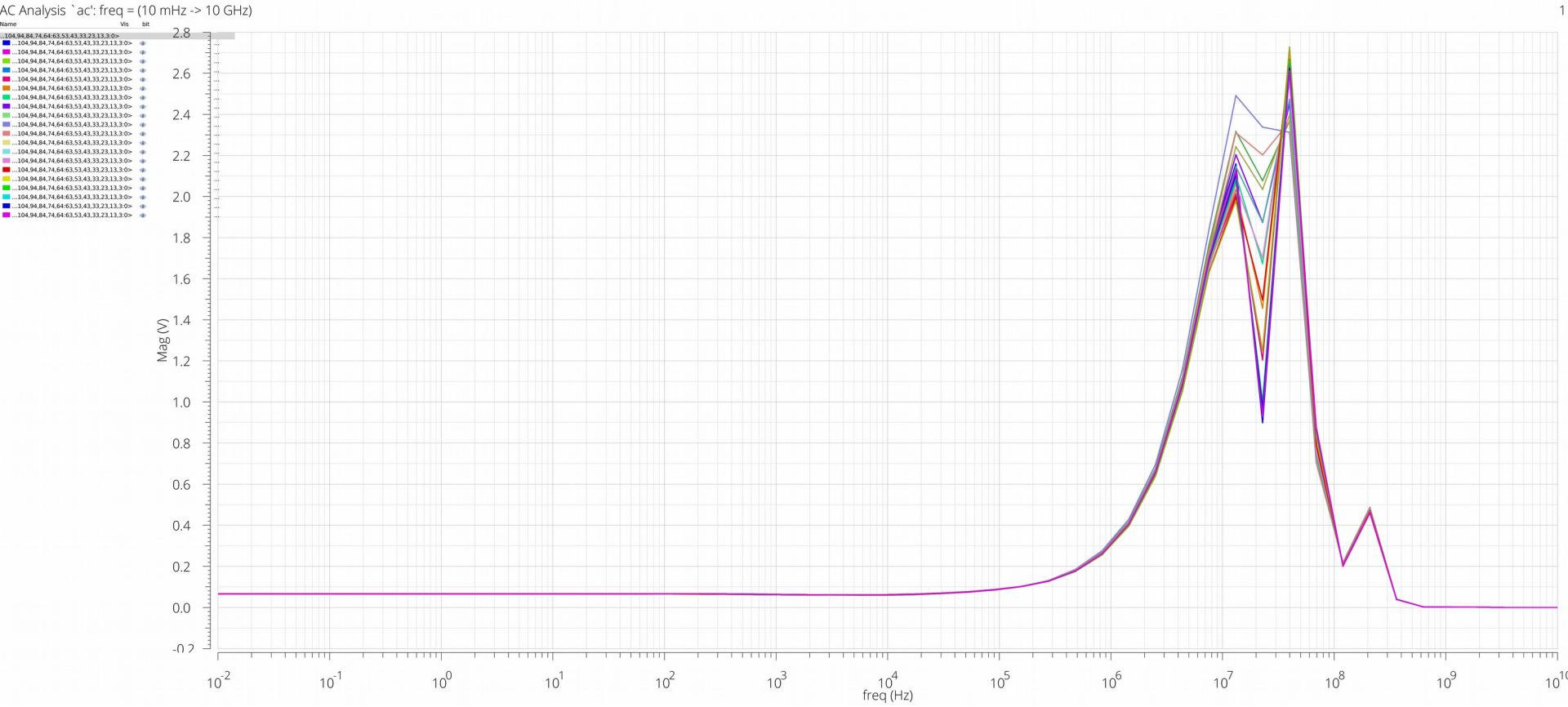
- ADC delay=4, No internal inductances, Cchan_decADC=0

SALT3 simulation results – ext RC AC, pre out v3_1



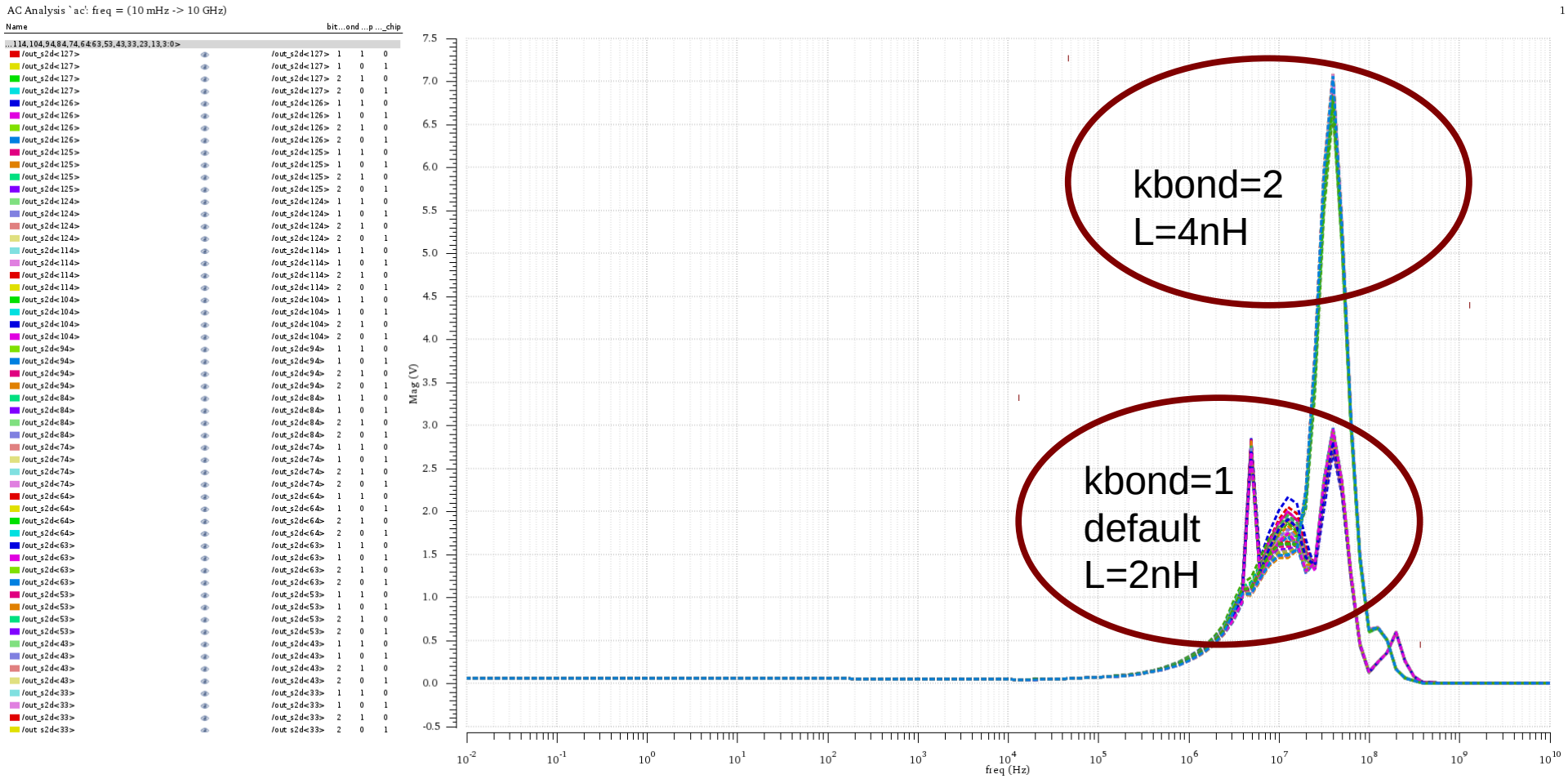
- @40MHz ~0.2, peak@200MHz

SALT3 simulation results – ext RC AC, S2Diff out v3_1



- Peak of about 2.7 @40MHz

SALT3 simulation results – ext C
AC, S2Diff out v3_1 versus bond inductance



- Power supply bonds should be shortest possible!
- Effect was much smaller for sims of 128 channels with LR power distr.