GEM Detector and Its Readout System

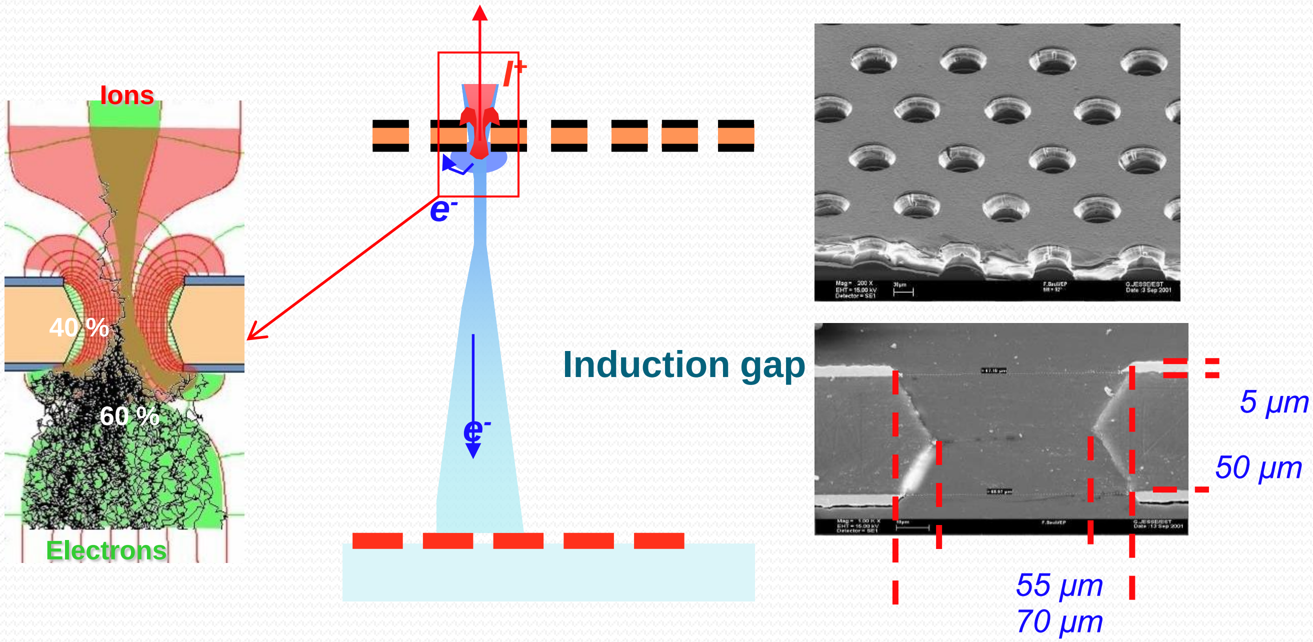
Bartosz Mindur

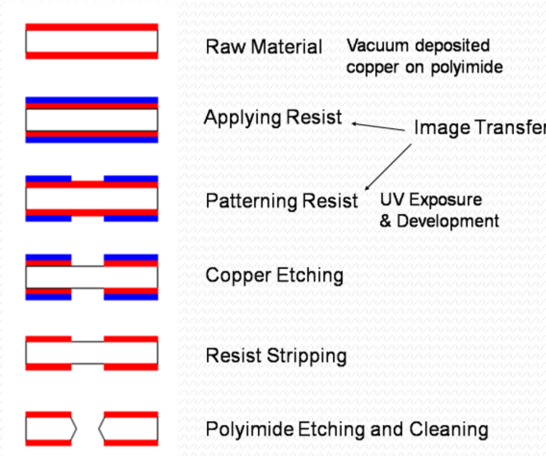
Faculty of Physics and Applied Computer Science
AGH University of Science and Technology, 30-059 Krakow, Poland

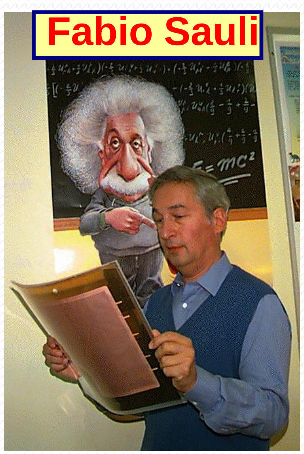
Outlook

- GEM Detectors
- Our Setup
- MSGCROC Chip
- “Juelich” readout
- DAQ Software
- Detector test results
- Ethernet readout
- Conclusions
- Online Ethernet readout presentation

Gas Electron Multiplier



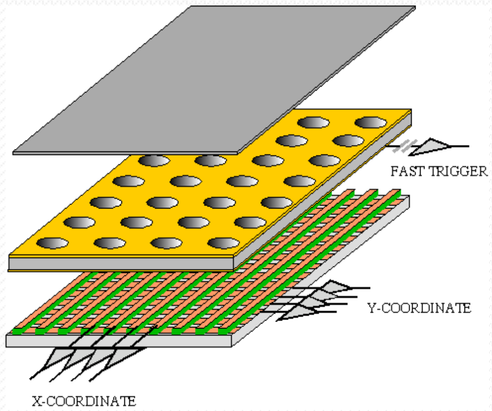




- Invented in 1997 by Fabio Sauli
- GEM is a thin, metal coated polyimide foil perforated with high density holes
    - Holes are typically 70μm in diameter, 140μm apart in triangular pattern

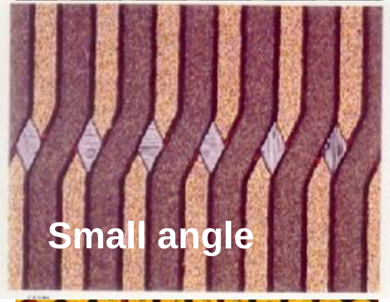
- Electrons are collected on patterned readout board
- A fast signal can be detected on the lower GEM electrode
- All readout electrodes are at ground potential

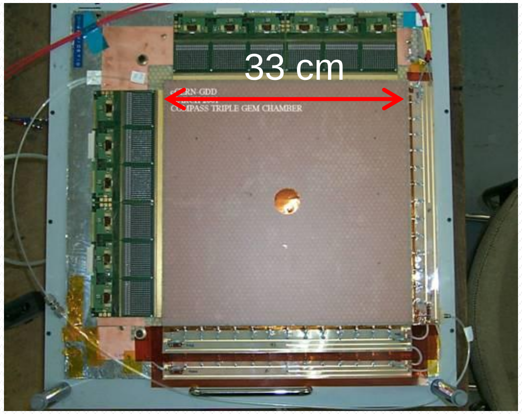
GEM – many types



A. Bressan et al, Nucl. Instr. and Meth. A425(1999)254

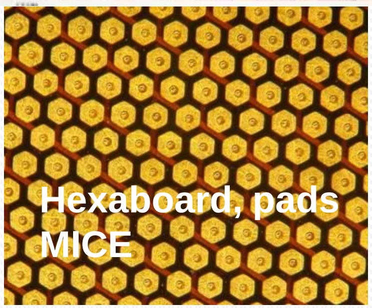
- Full decoupling of the charge amplification structure from the charge collection and readout structure
- Both structures can be optimized independently

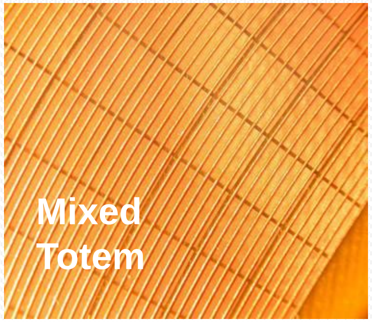




Compass

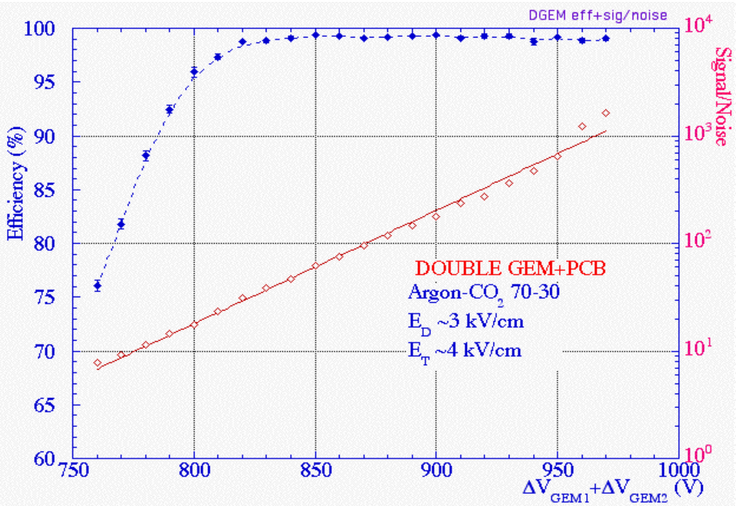
Totem



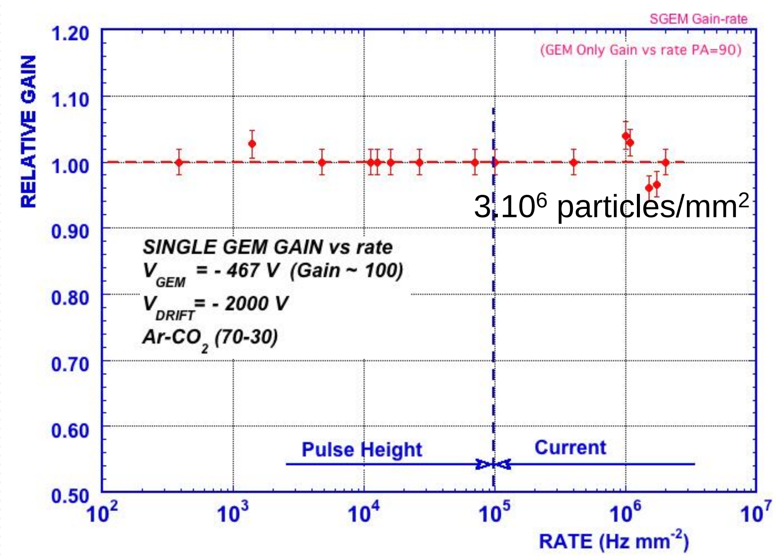


- Both detectors use three GEM foils in cascade for amplification to reduce discharge probability by reducing field strength.

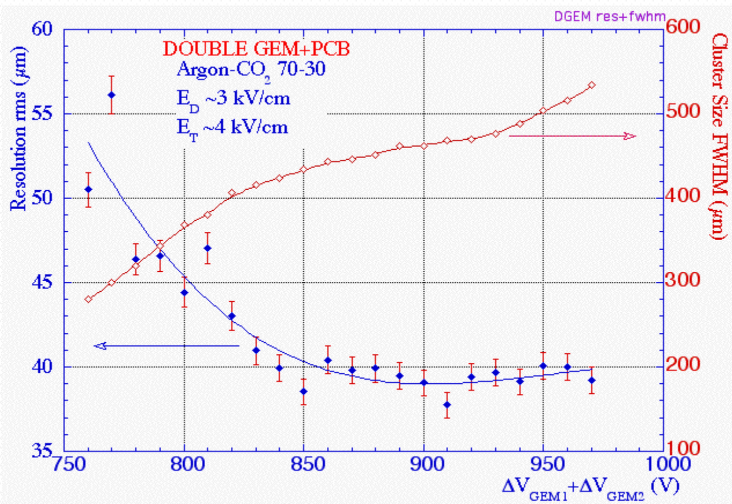
GEM Performance

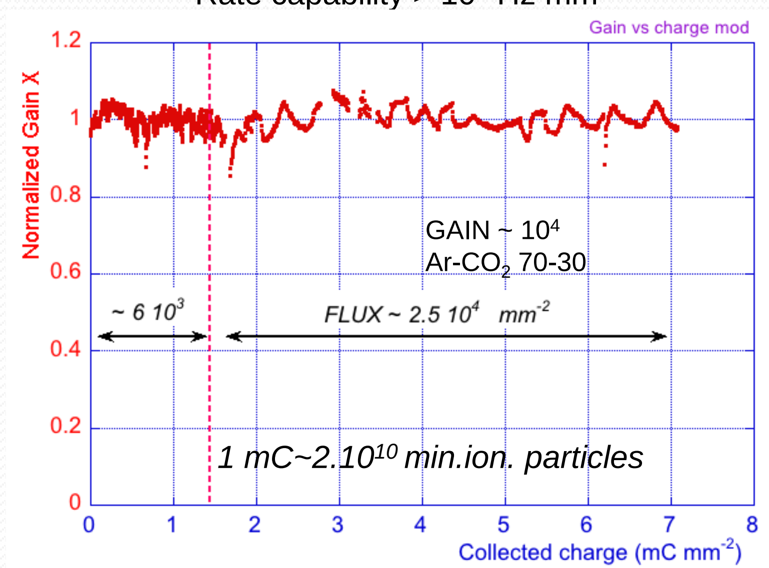


Efficiency for minimum ionizing particles with 3 mm gap



Rate capability > 10^6 Hz mm^{-2}



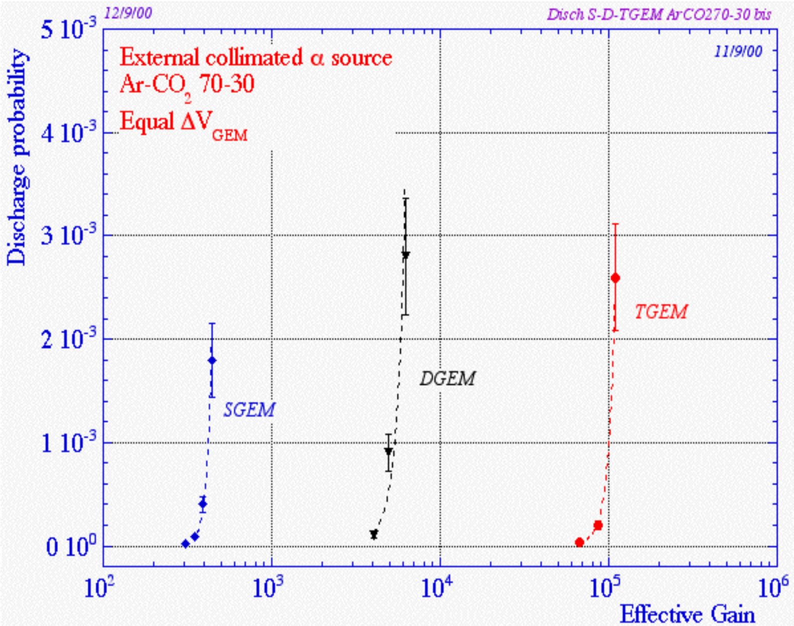


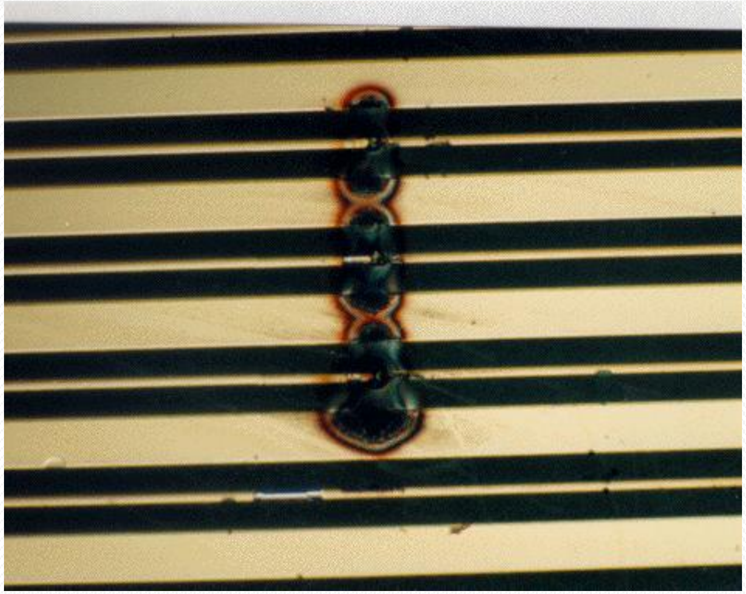
Space resolution ~ 40 μm rms
Cluster size ~ 500 μm FWHM

C. Altunbas et al, DESY Aging Workshop (Nov. 2001) Nucl. Instr. and Meth. A
A. Bressan et al, Nucl. Instr. And Meth. A425(1999)262

GEM Limitations

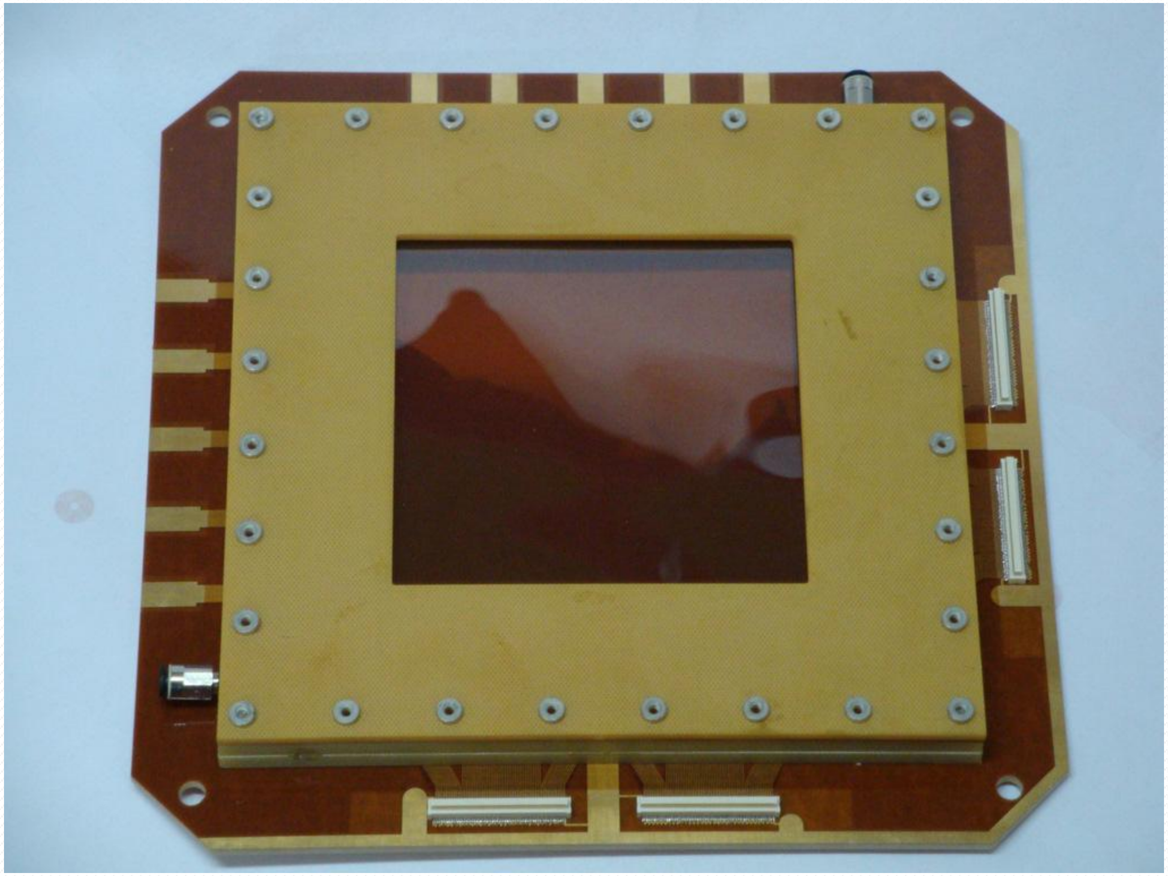
- Discharges
  - Caused by field and charge density
    - Can destroy the detector
    - Can destroy front-end
    - Solution
      - Multistep amplification
- Insulator charging up
  - Gain variation with time and rate
  - Solution
    - Slightly conductive materials





Our detector

- Standard CERN GEM
  - 10 x 10 cm
  - Kapton window
  - Three GEM foils
  - X & Y readout strips
    - 256 per plane
  - Drift space of 3 mm
  - Transition and Induction gaps of 2 mm

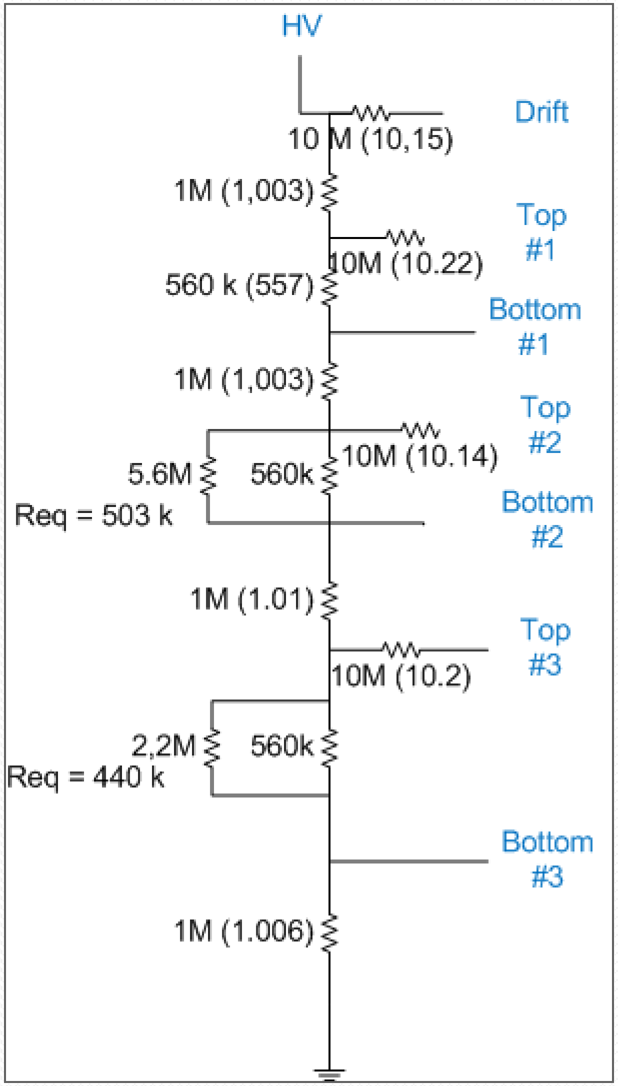


- Readout of the strips
  - Via four Panasonic 130 pin connectors
    - Part no. AXK6SA3677YG
    - 128 signal
    - 2 ground lines
- Gas inlet and outlet
- Pads for HV soldering

HV Distribution

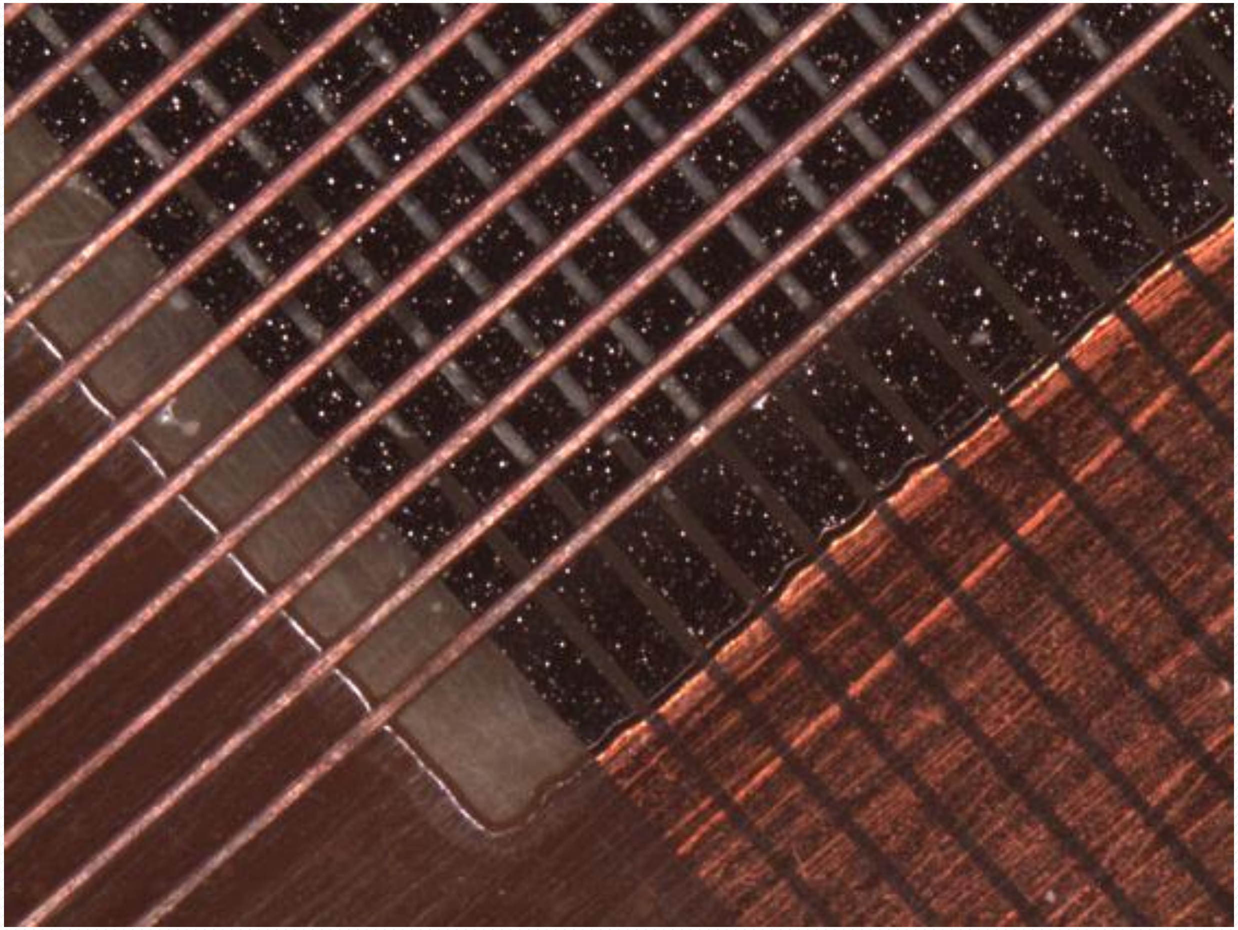
- Asymmetric HV divider
  - Pros
    - One HV power supply needed
    - Slightly different voltage on each GEM foil
  - Cons
    - No flexibility
    - Relatively high current needed (0.8 mA)

V	GEM 1 (V)	GEM 2 (V)	GEM 3 (V)
3800.0	383.3	346.1	302.8
3900.0	393.4	355.3	310.8
4000.0	403.5	364.4	318.7
4100.0	413.6	373.5	326.7
4200.0	423.7	382.6	334.7
4300.0	433.7	391.7	342.6
4400.0	443.8	400.8	350.6
4500.0	453.9	409.9	358.6



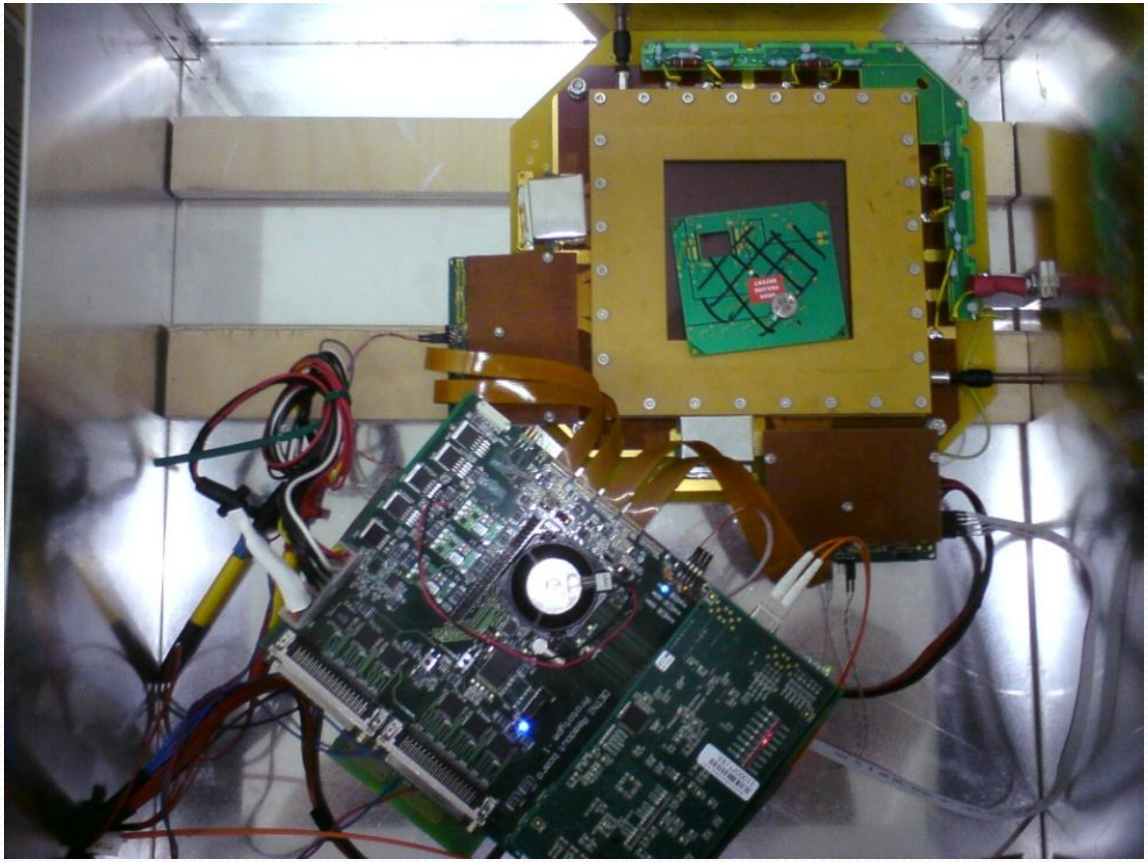
Readout structure

- 256 x 256 strips
  - One strip plane on top of the other
  - Only negative signals
  - Different strip widths to get the same number on electrons collected on both planes

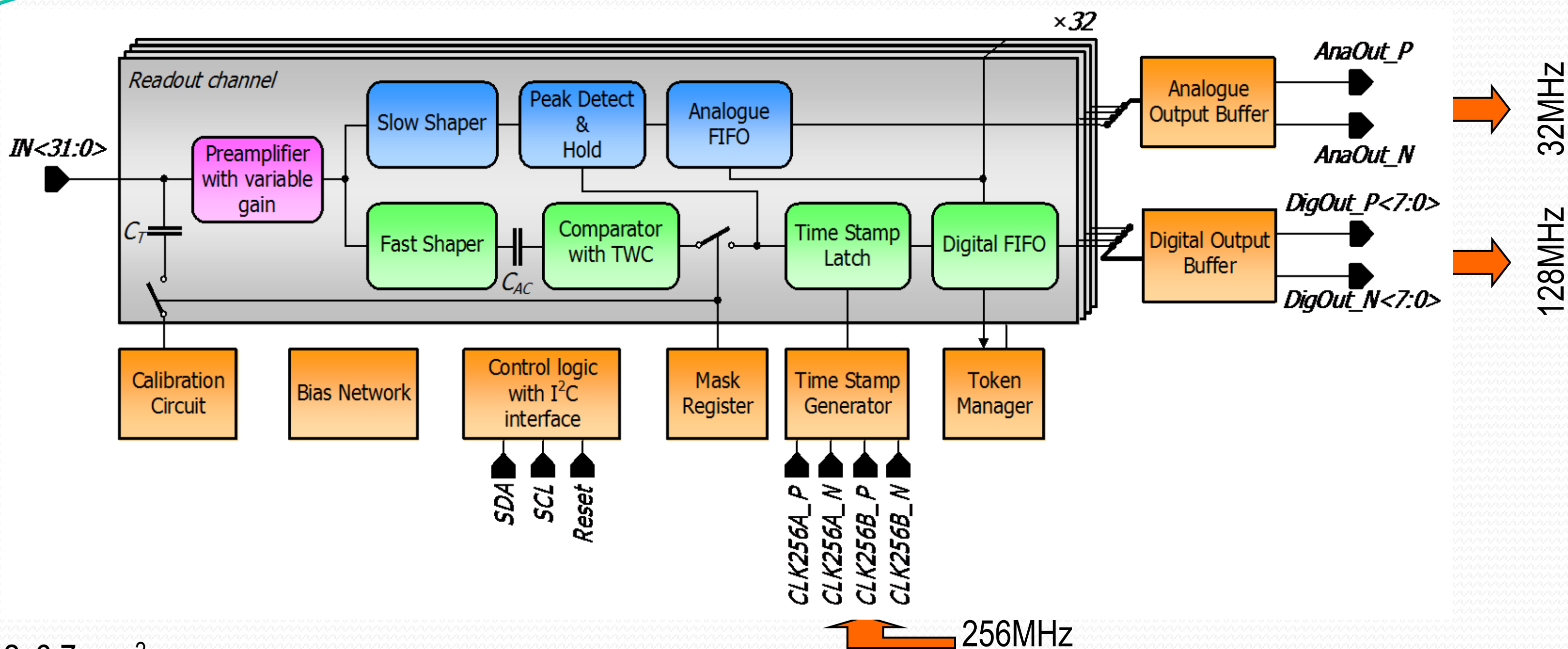


Our setup

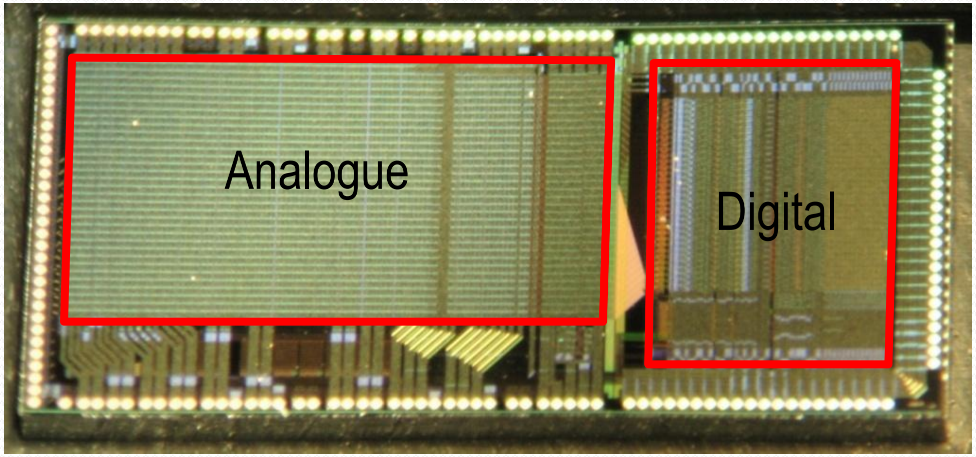
- Standard CERN triple GEM
- Ar/CO_2 80/20 gas mixture
- HV power supply
- Two ASICs' boards
  - Each has two ASICs
- FPGA board
- Time distribution board
- SiSLink optical connection to PC
- Dedicated readout software



MSGCROC

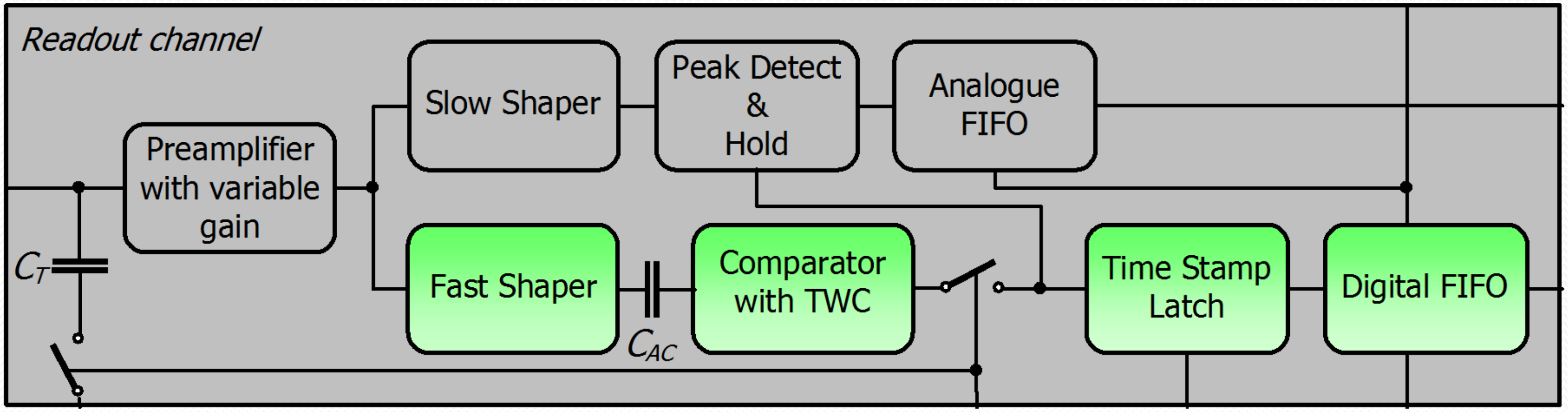


3.2x6.7 mm²



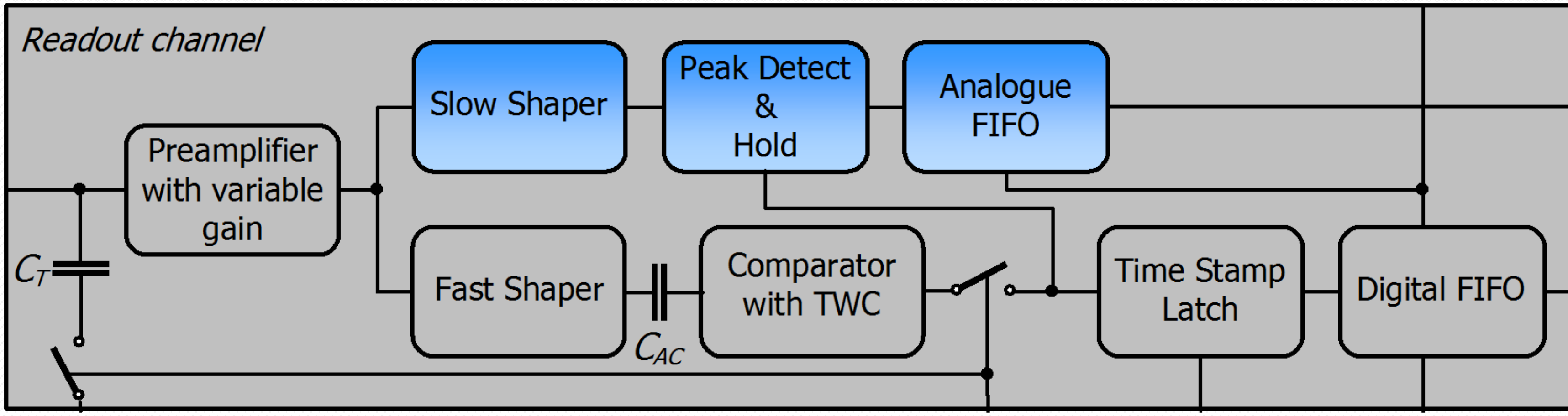
- 0.35 mm CMOS process from Austria Microsystems
- Input device: PMOS 2368µm/0.4 µm
- Bias current of the input transistor: 2.36mA (nominal)
- Power consumption ~25 mW/channel (@ 3.3 V)
- Separated analogue and digital power supply

Timing channel



- Fast Shaper - T_{peak} = 25 ns
- Comparator with TWC - T_{walk} < 2 ns
- The output signal from the timing channel is used to latch a 14-bit time stamp of 1 ns resolution and to enable the peak detector and hold (PDH) circuit in the energy channel
- Each comparator is equipped with a 5-bit trimming DAC, which allows to correct the threshold offset on the channel basis with a precision better than 1 LSB in the threshold DAC (8-bit) common for all channels

Energy channel



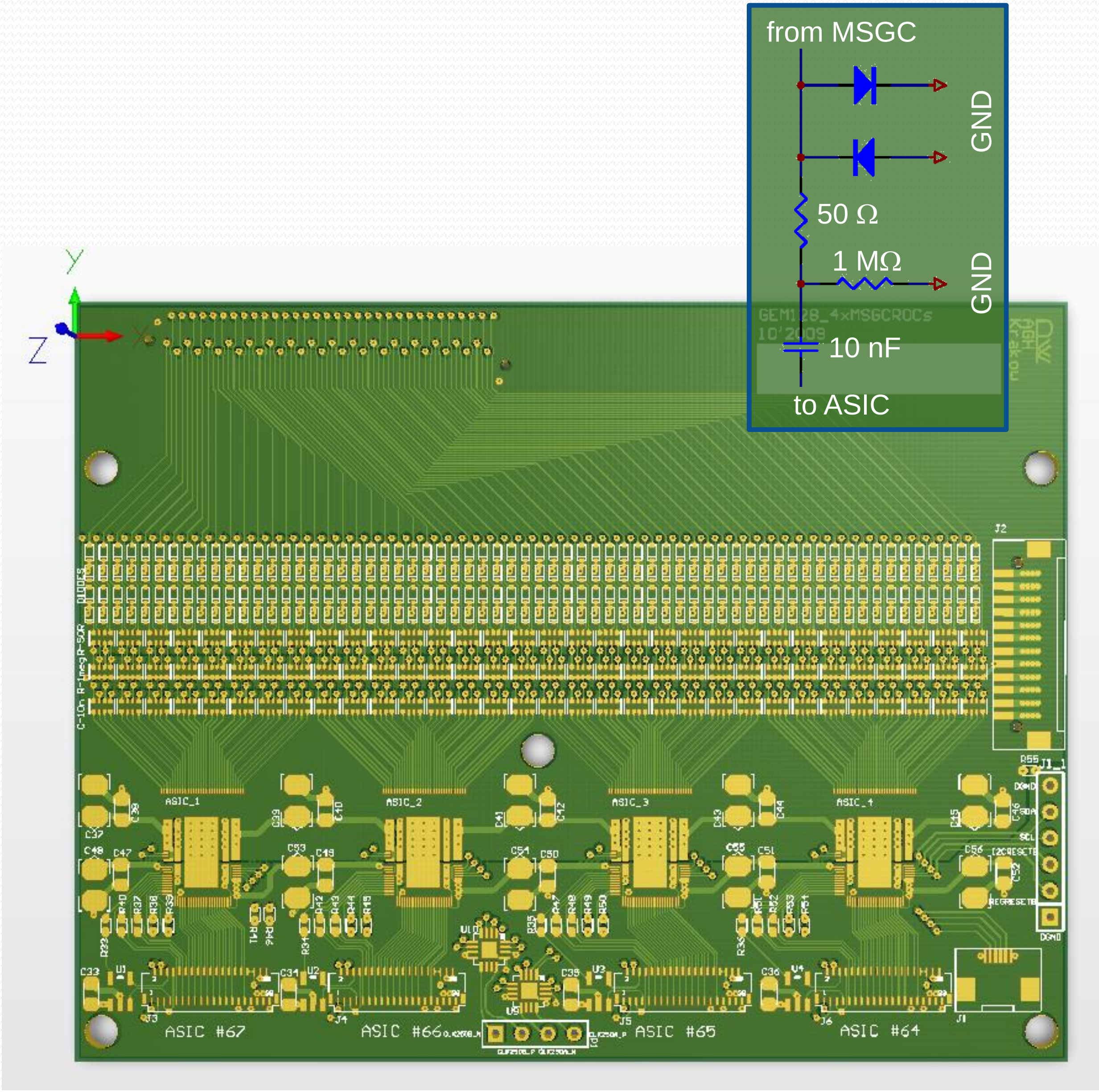
- Slow Shaper - T_{peak} = 85 ns
- The PDH circuit detects peaks of incoming pulses and holds their values for a given time period controlled with respect to the response of the comparator in the fast timing channel

MSGCROC Characteristics

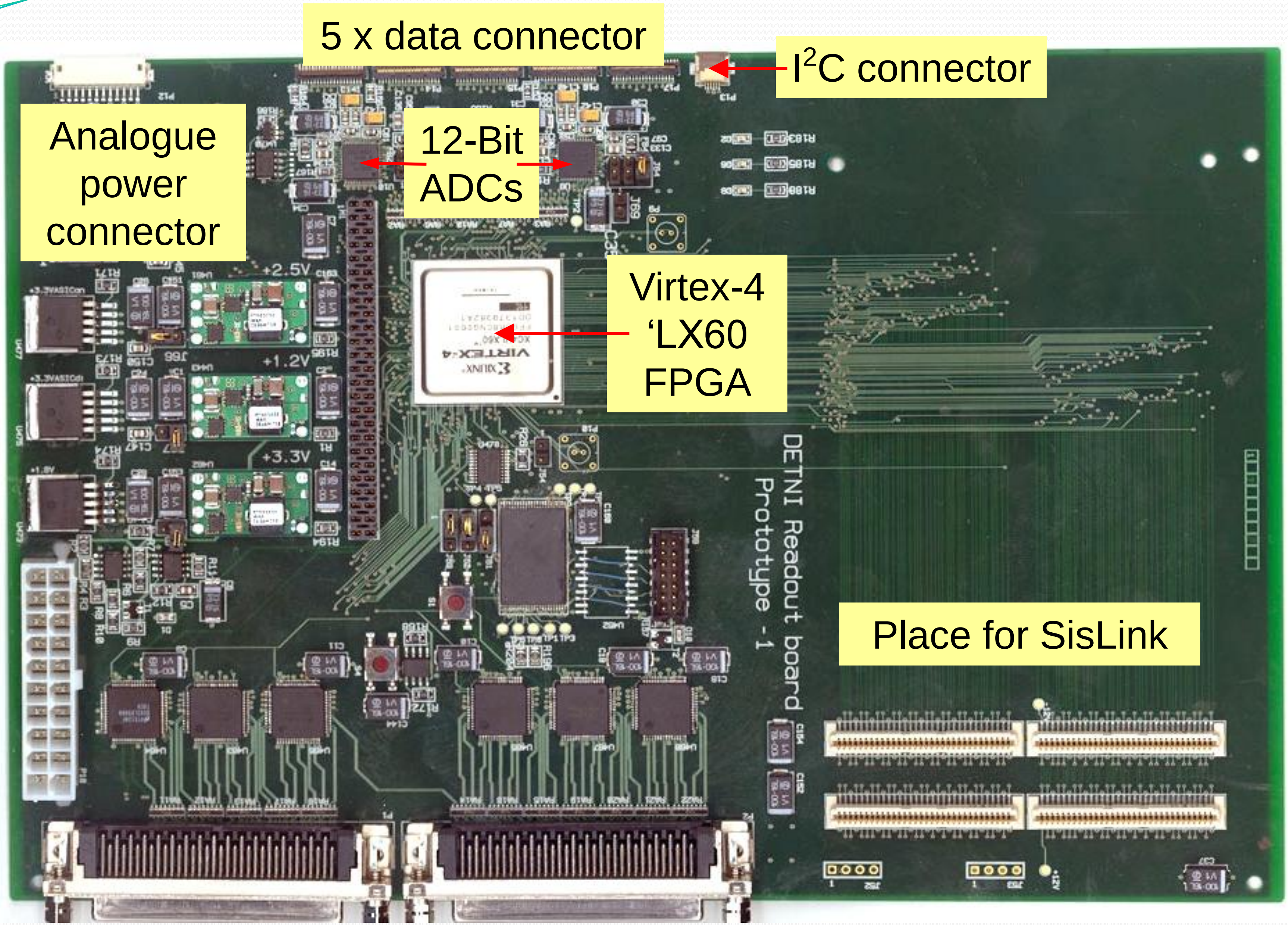
- Signal parameters to be measured:
  - position X/Y, time T, energy (amplitude) EX/EY
- Detector strip capacitance: ~ 23 pF
- The preamp-shaper circuit must be compatible with positive and negative signal polarities
- Input signal charge: $2 \cdot 10^5$ e- (32fC) - $5 \cdot 10^6$ e- (800fC) (depending on the detector gas amplification)
- Variable gain in a range 1 - 20 to cope with different detector gas amplification factors
  - Gain factors: ×1, ×2, ×4, ×8, and ×16
- Hit rate per strip: ~ $9 \cdot 10^5$ /s (global count rate: 10^8 /s)
- X/Y coincidence window 2 ns + (EX = EY)
- Discriminator: time walk < 2 ns, jitter < 2 ns FWHM
- The data must be buffered and derandomized on the ASIC
  - 4 - bit FIFO analogue and digital
- Zero suppression must be performed on the ASIC
- The ASIC must generate a self trigger for each event

GEM ASICs' Board

- Two boards
  - Each with two ASICs
- 1MΩ termination resistors solder to all input lines
- 64 channels per board fully operational

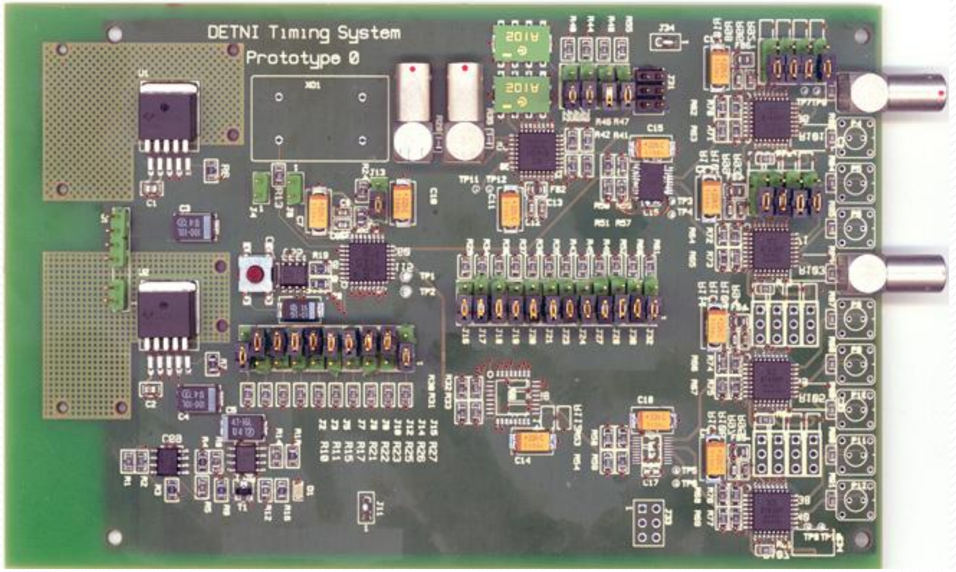


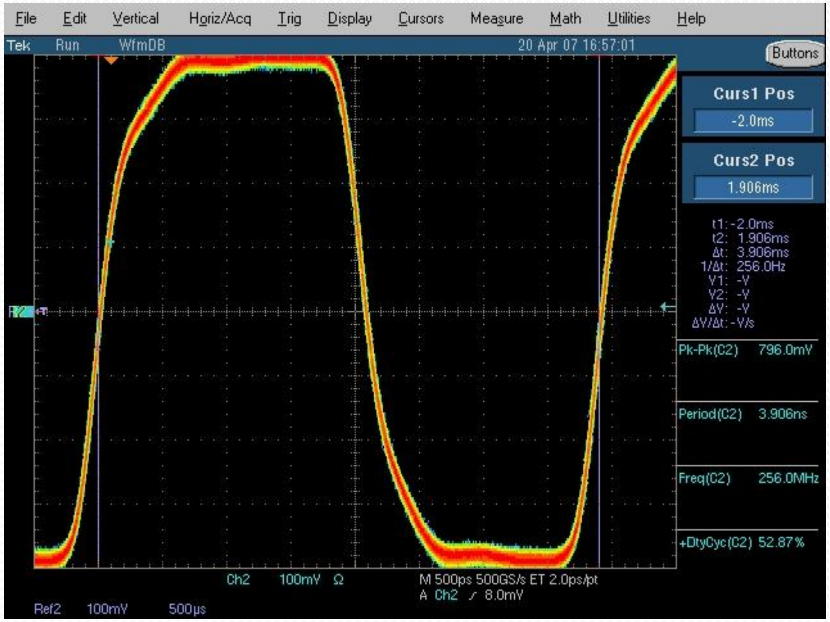
ADC-FPGA prototype board

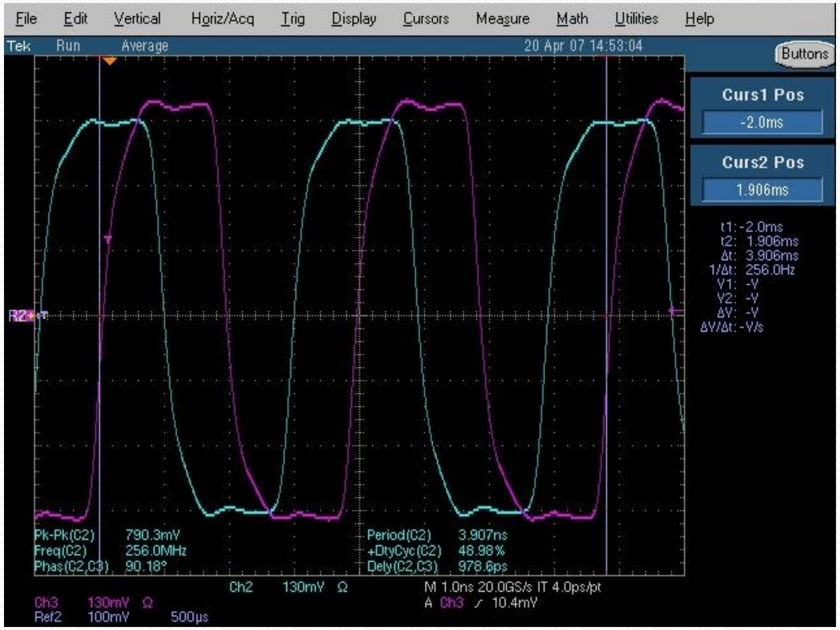


Clock distribution board

- Master reference frequency 32 MHz
- Clock outputs:
  - 5 x 256 MHz
  - 5 x 256 MHz 90° phase shifted
- 30 ps max. cycle-to-cycle Jitter





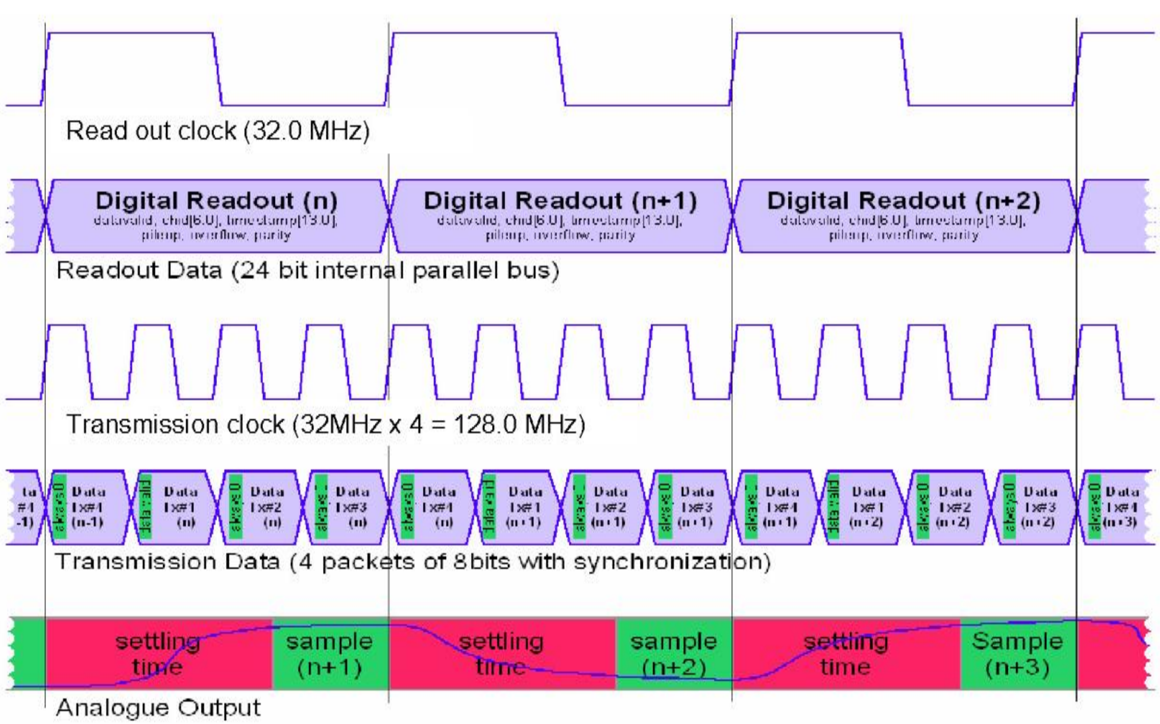


Data format and timing diagram

ASIC output:
25 bits
+
analogue information

	7	6	5	4	3	2	1	0
0	DV	TS13	TS12	TS11	TS10	TS9	TS8	TS7
1	0	TS6	TS5	TS4	TS3	TS2	TS1	TS0
2	0	ID6	ID5	ID4	ID3	ID2	ID1	ID0
3	0	0	0	0	0	PileUp	OverF	Parity

data valid TimeStamp channel id



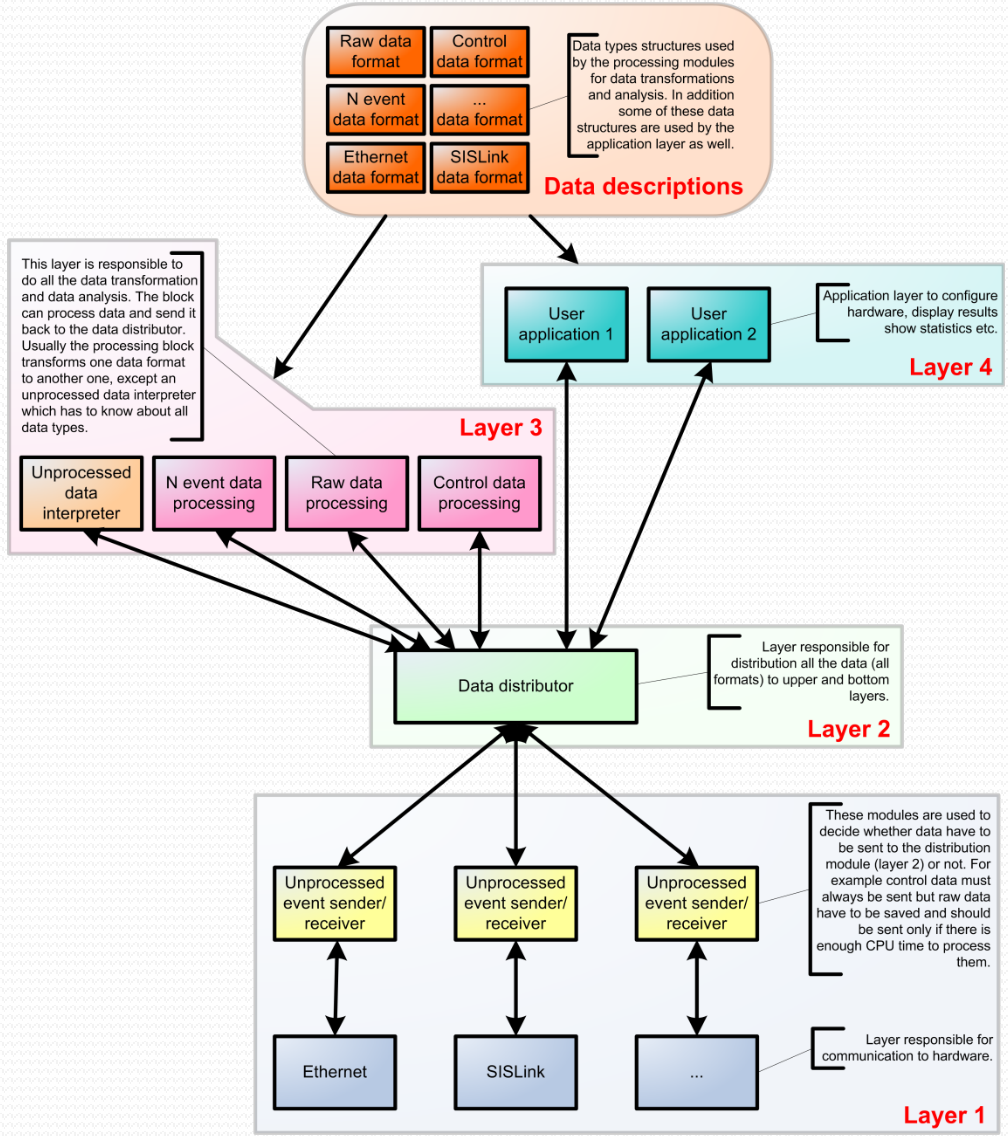
multiplexed readout

digital output

analog output

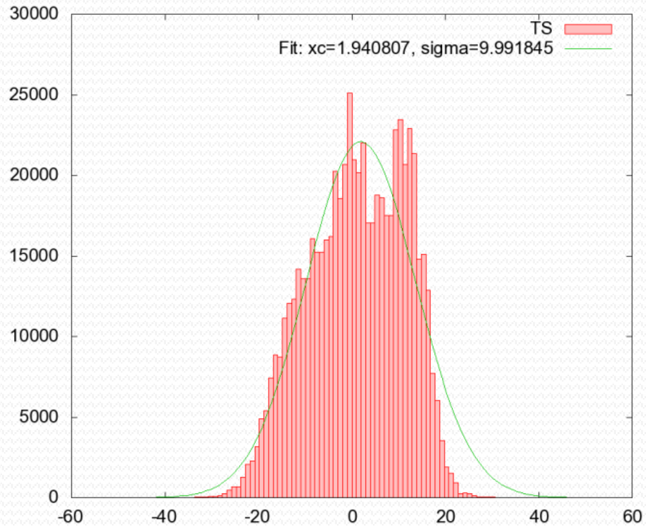
DAQ Software – layered concept

- DAQ Software is structured in four layers:
  - Layer 1 - connection to the hardware (possible different types)
  - Layer 2 - data distribution to the processing modules
  - Layer 3 – includes data processing modules
  - Layer 4 - data visualization and overall system configuration (application level)

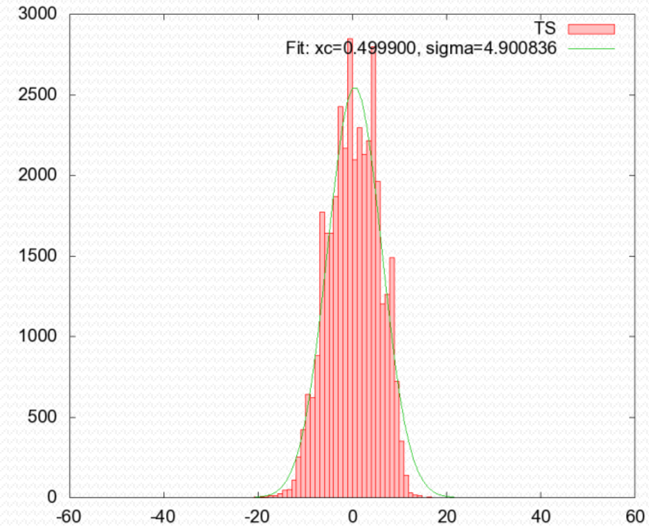


GEM Test Results

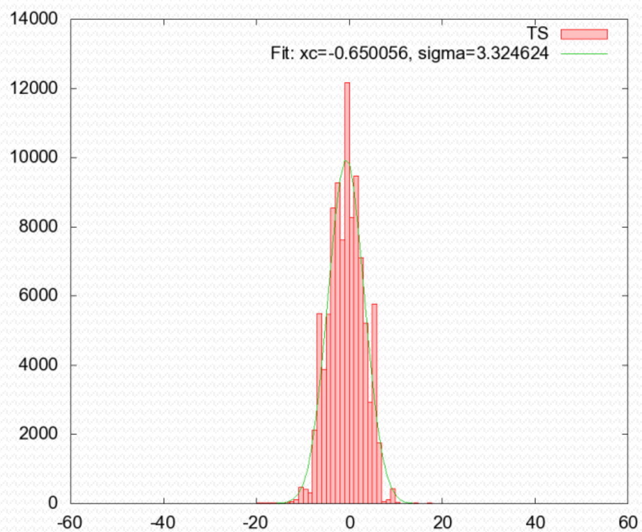
Timing measurement



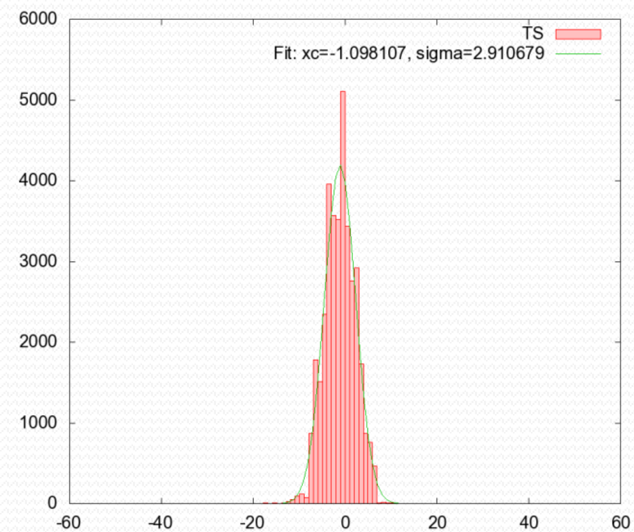
ASIC gain 4, threshold 23 (~315 eV), GEM voltage 3900 V



ASIC gain 4, threshold 40 (~550 eV), GEM voltage 3900 V

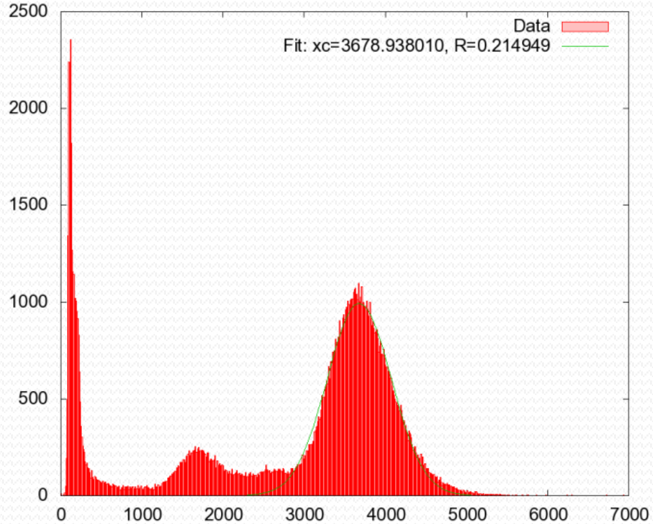


ASIC gain 4, threshold 60 (~820 eV), GEM voltage 3900 V

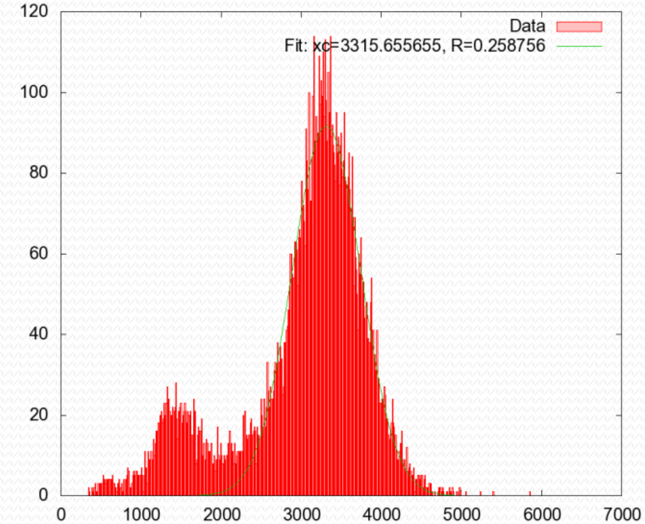


ASIC gain 4, threshold 80 (~1.1 keV), GEM voltage 3900 V

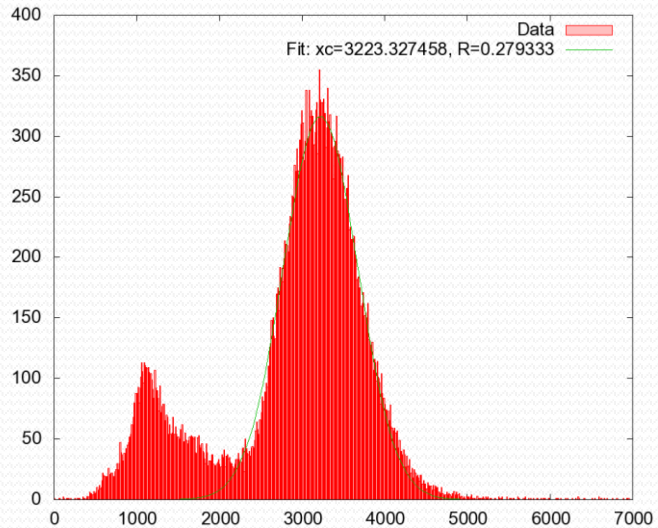
Fe-55 Energy Spectra



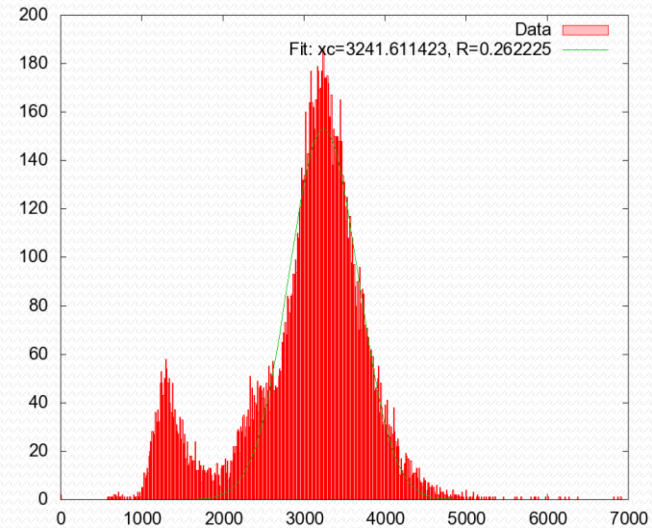
ASIC gain 4, threshold 23, GEM voltage 3900 V



ASIC gain 4, threshold 40, GEM voltage 3900 V

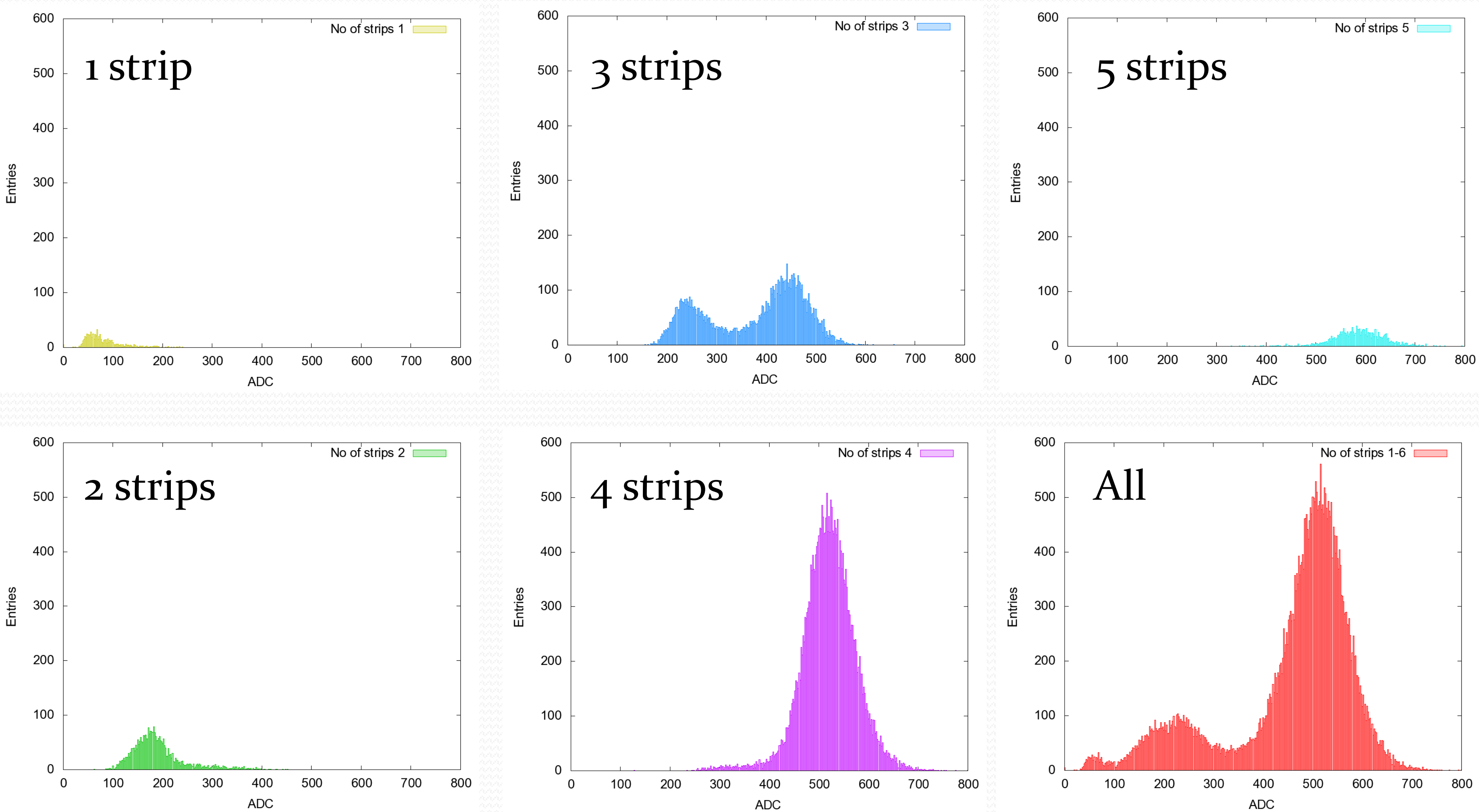


ASIC gain 4, threshold 60, GEM voltage 3900 V

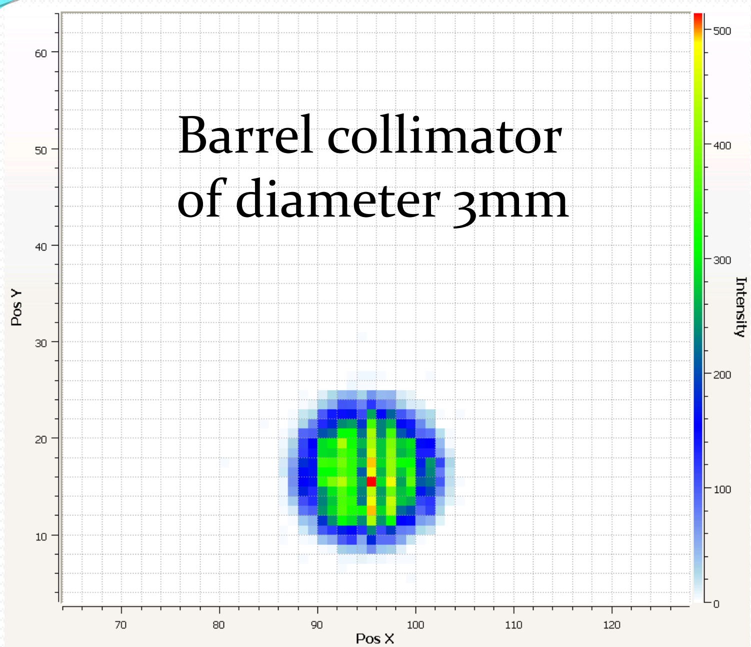


ASIC gain 4, threshold 80, GEM voltage 3900 V

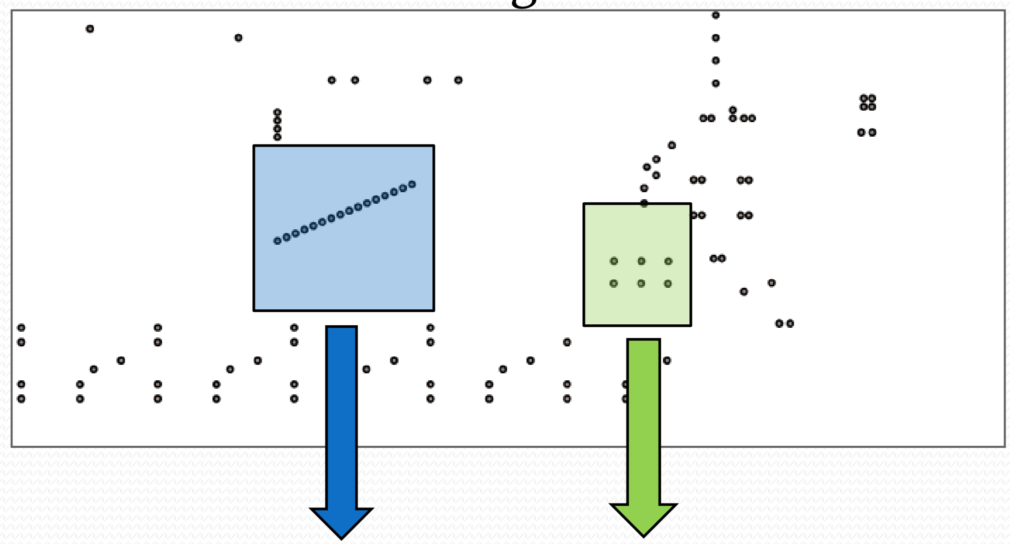
Amplitude distribution for strip clusters

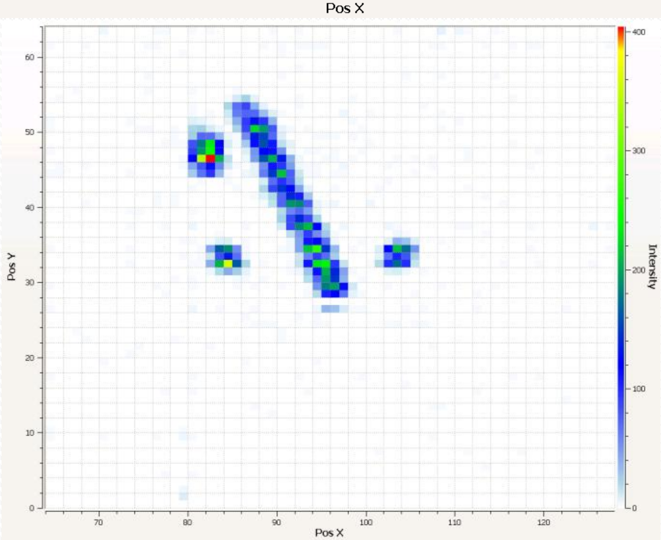


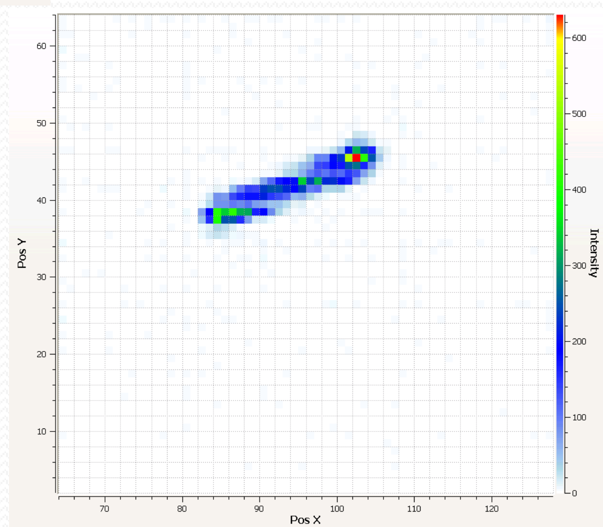
2D Imaging with Fe55

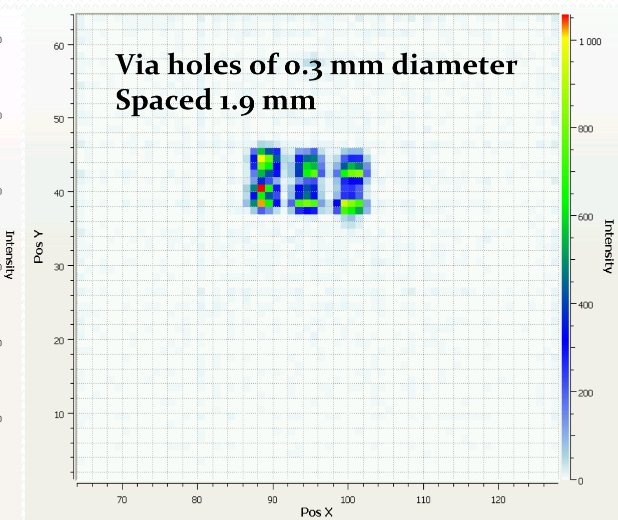


Pattern scans trough PCB holes









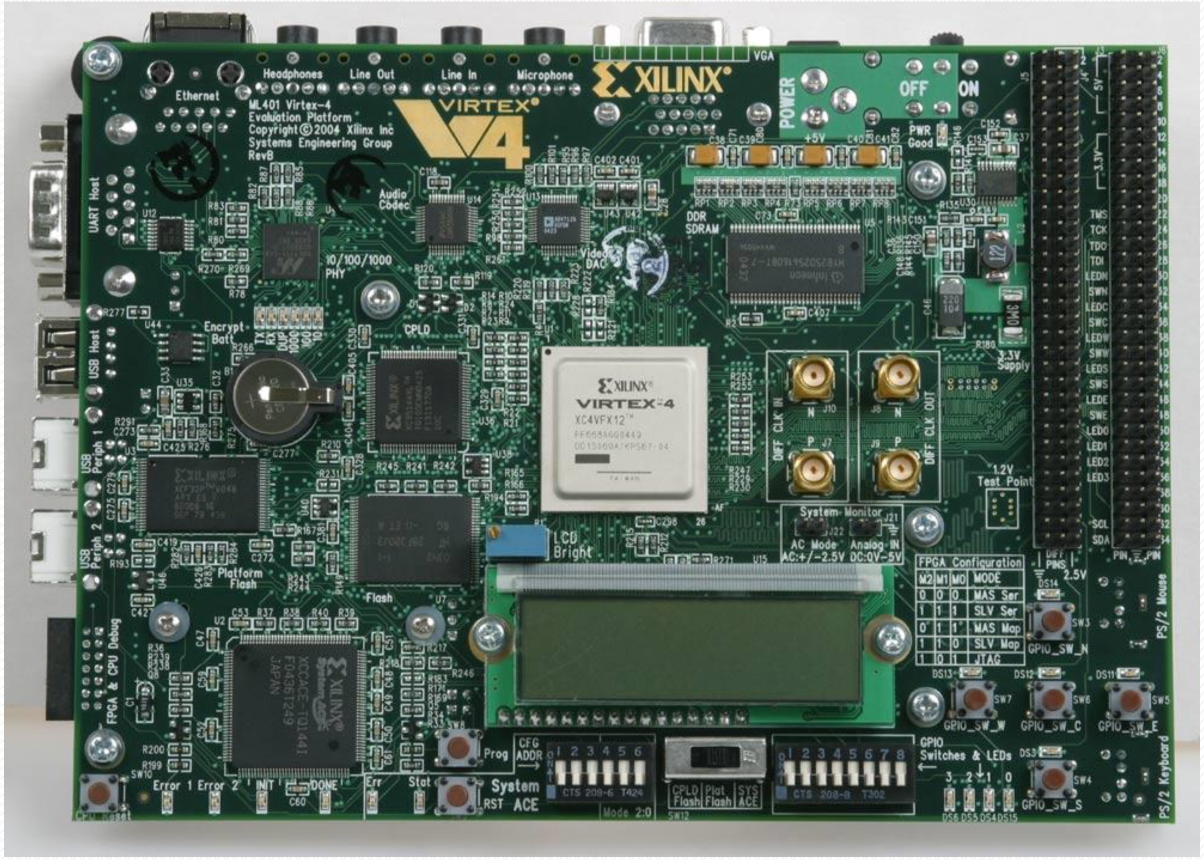
Results - conclusions

- Show very good time resolution
  - Only slightly worse then expected value
  - Still some place for improvement (TWC optimization)
- Energy channel characteristic
  - "Nice" collective energy spectrums
    - Energy resolution of about 21 – 26 %
      - Depends on threshold
- 2D Position resolution
  - "No so good"
    - Because the source type (Fe-55)
- Further studies are ongoing

Ethernet Readout System

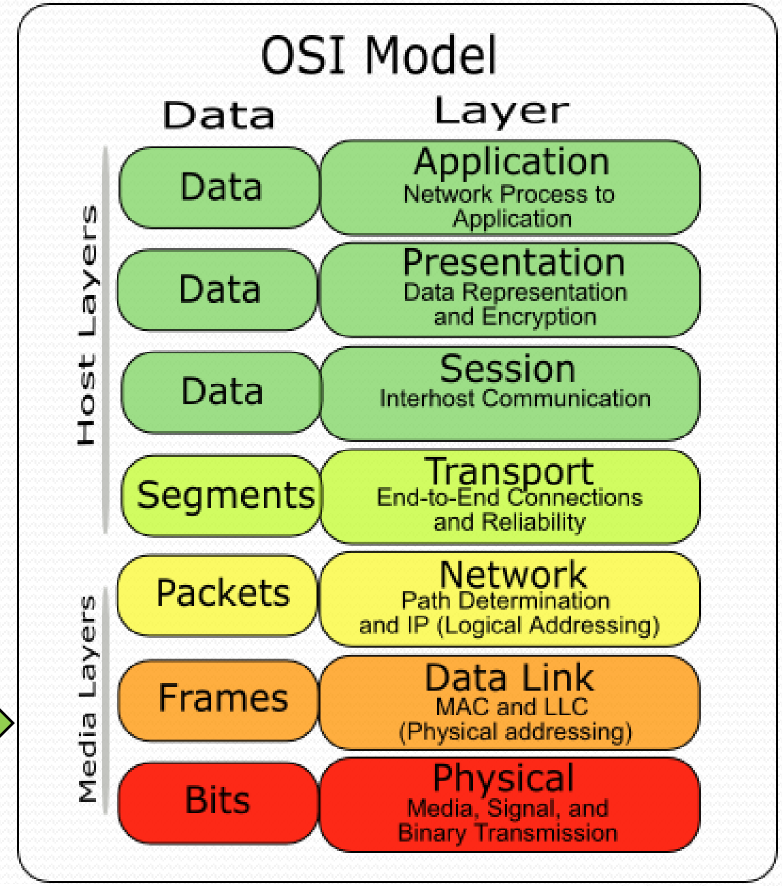
Ethernet Readout

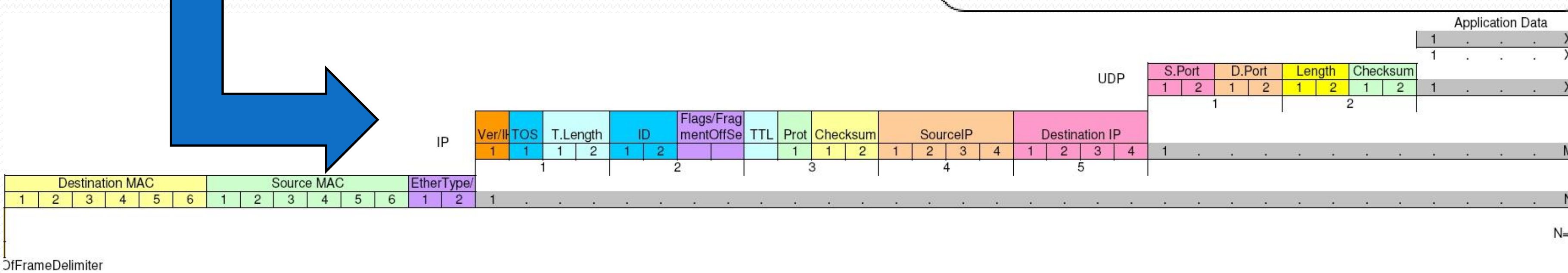
- Xilinx ML 403 Evaluation Board
- Virtex-4 FX 12
  - Build-in Hard Ethernet MAC
- Using Ethernet
  - Raw frames can be sent relatively easily
  - Or custom made protocol



Ethernet Layers

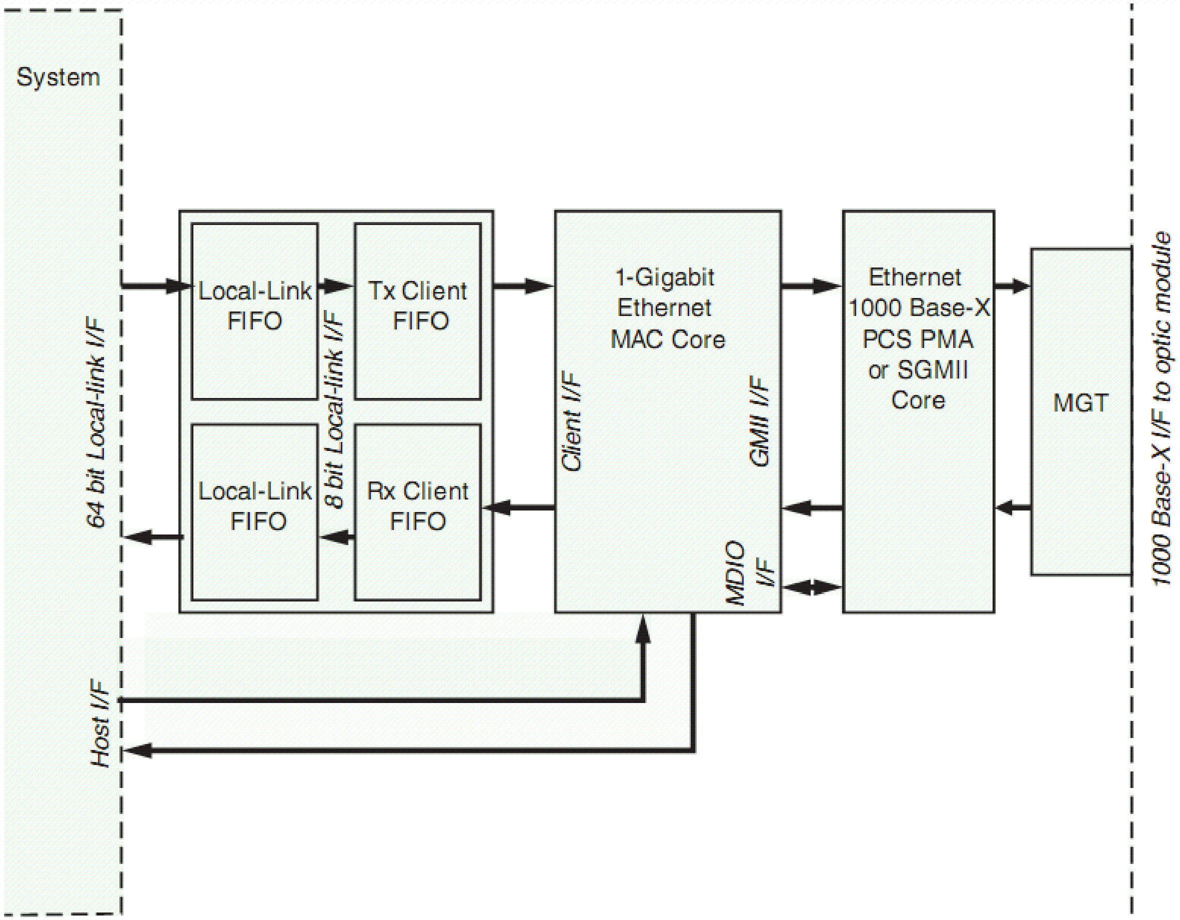
- Open System Interconnection Model
  - Two/three bottom layers
- UDP Packet
  - Raw frame
    - IP header
      - UDP header
        - Data





Core Components for Ethernet readout

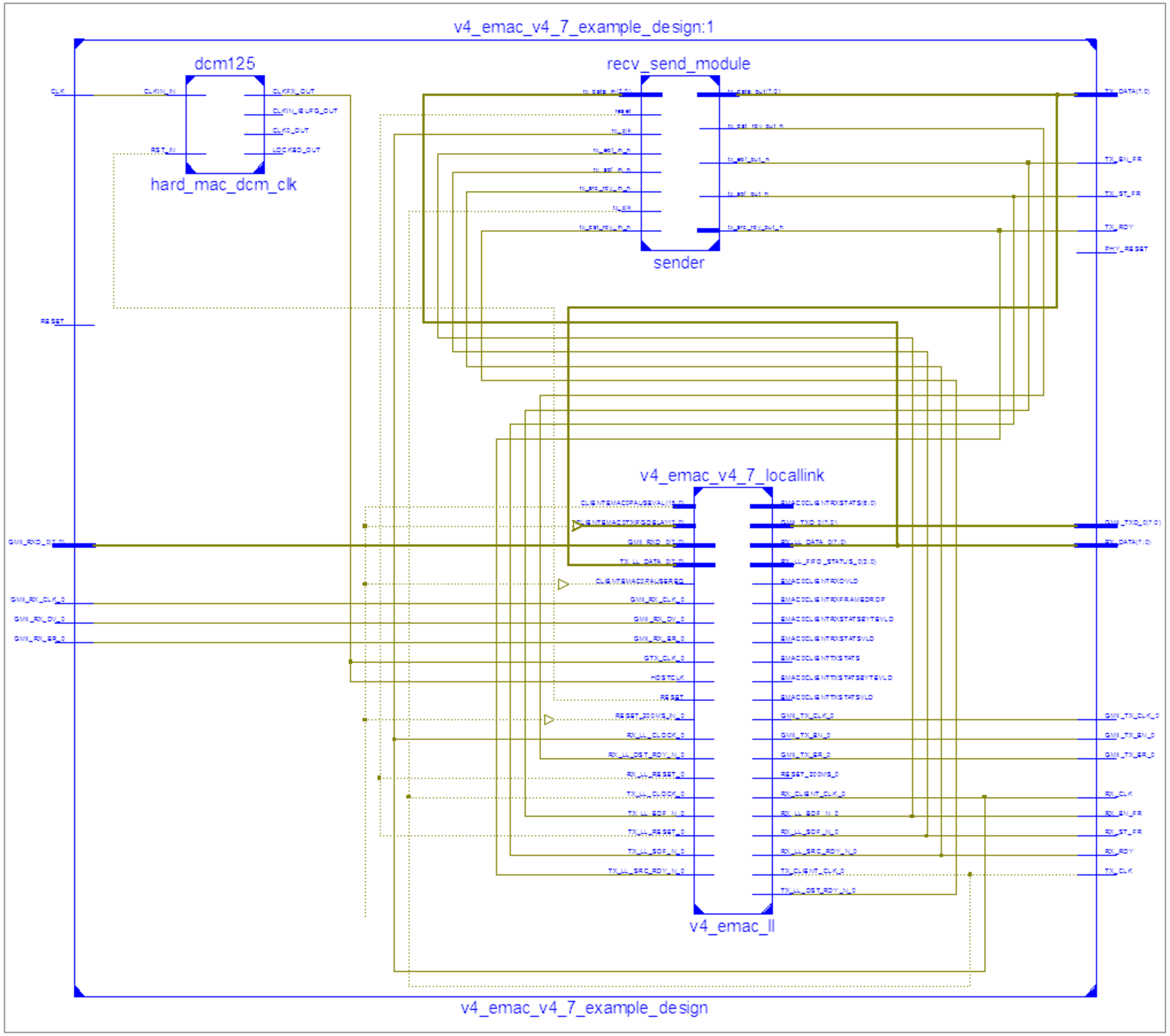
- Hard Ethernet Mac
- Xlinx Virtex4/5/6 FX
- Ethernet MAC Wrapper IP core
  - LL FIFO 4kB each
- Custom protocol
  - Implemented on top of the LL FIFOs
- Driver for Linux ready working with full speed
- Driver for Windows under the development



Current functionality (FPGA)

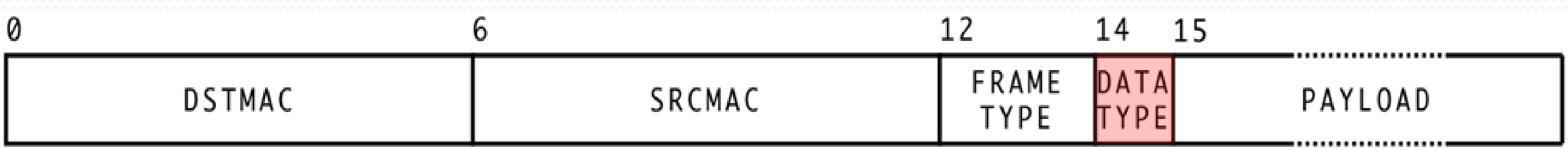
- Receiving control frames
  - Start
  - Stop
  - Reset
- Sending data with different types
  - "Raw data"
  - "Control data"
  - Each packet is filled with 64bit counter contains frame no. and fake data up to 1500 bytes
- Rather "proof of concept" design
  - Needs further development

Design Schematic



Custom protocol - EPPRO frames

- Frame format is compliant with commonly used Ethernet II (DIX) standard
  - Receiver MAC address
    - 6 bytes
  - Sender MAC address
    - 6 bytes
  - Frame type
    - 2 bytes
- Frame types used by EPPRO
  - 0x0823 – default type
  - 0x0824 – EPPRO RAW type
    - frame does not contain DATATYPE field
    - Payload starts at byte 14
- EPPRO-specific field on 15-th byte describes data type that frame carries in it's payload
  - Payload starts at byte 15
  - Payload can be
    - 45 to 1500 bytes
      - Regular frames
    - Up to 9000 bytes long
      - Jumbo frames



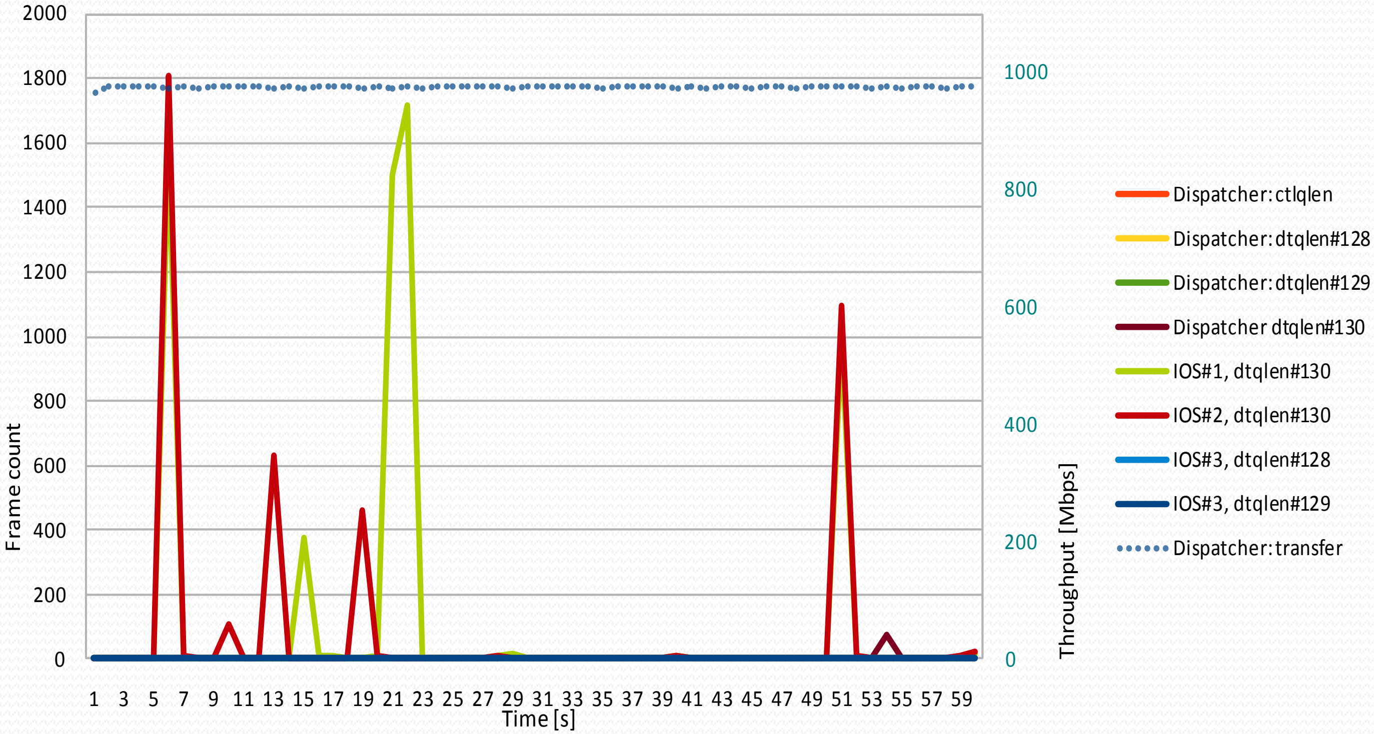
EPPRO, LIBEPPRO – design ideas

- EPPRO – Linux kernel module
  - As opposed to regular Ethernet driver, EPPRO module is independent from actual hardware
    - It works on top of hardware specific drivers
  - Features
    - Buffers, queues frames and passes them to their destination
    - Maximum efficiency
    - Handles queues' overflow in a smart way
    - Frames are passed to
      - User-space
      - Written directly to disk (for efficiency)

- LIBEPPRO: API+library+SDK
  - C-language API defines set of functions and structures enabling user to manage the module
  - Contains ready-to-use tools (i.e. eppconfig)

Test Case: Two Files

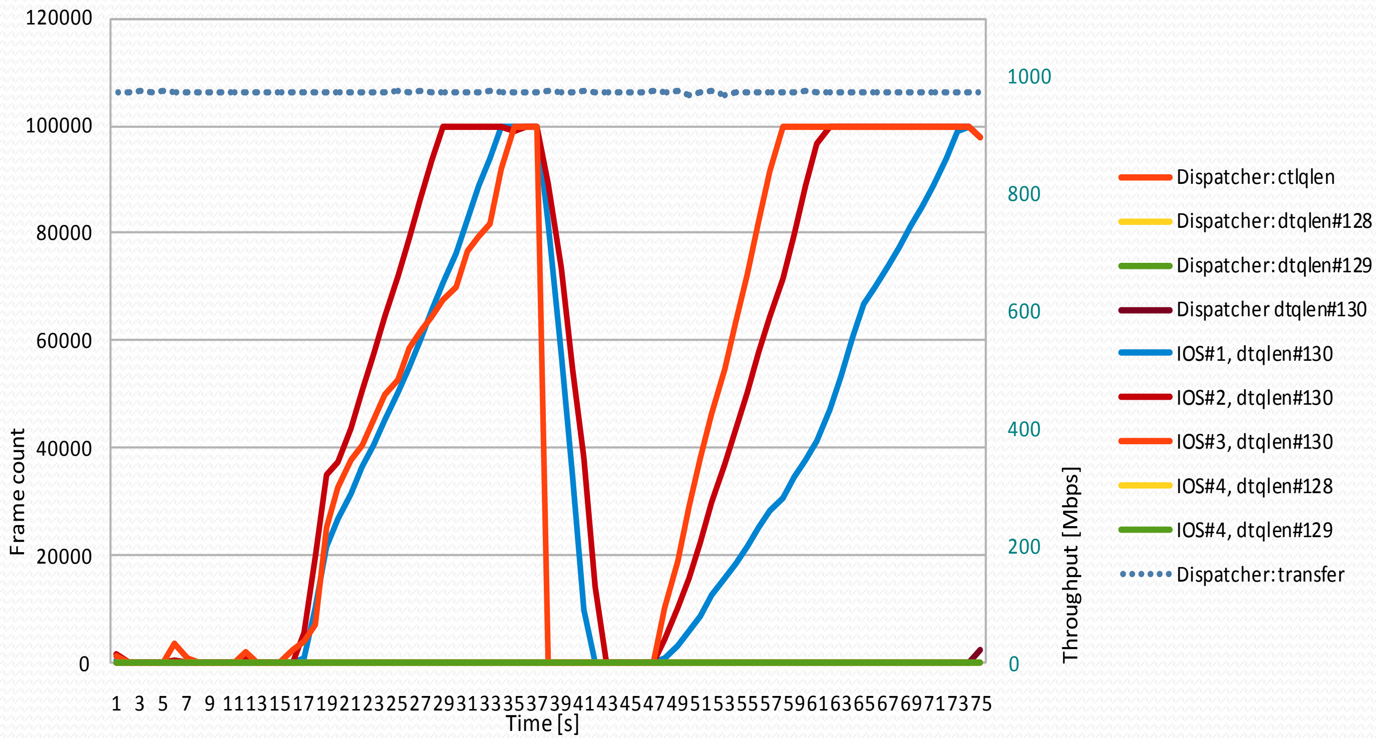
- Three data types
  - 128, 129 – control data, small amount, high priority
  - 130 – actual data, high throughput
- Three IOSes
  - 1,2 – files, subscribing DT#130
  - 4 – user-space app, subscribing DT#128,129



Conclusion: **NO DATA LOSS!** Transfer close to 1Gbps

Test Case: Three Files

- Three data types
  - 128, 129 – control data, small amount, high priority
  - 130 – actual data, high throughput
- Four IOSes
  - 1,2,3 – files, subscribing DT#130
  - 4 – user-space app, subscribing DT#128,129



On 38th second IOS#3 is removed. On 48th – added back.

Conclusion: Data loss on IOS level. Dispatcher queues still OK.

Slow control (very preliminary)

- I2C master model
  - Verilog synthesizable model
- I2C slave
  - Behaviour simulation model
  - Verilog synthesizable model
- Shall be integrated with Ethernet Readout
  - Easy compact solution for data readout and ASICs setup
- May also be used as RS232 to I2C interface
  - For any kind of FPGA

Conclusion

- Detection system
  - GEM detector
  - Full readout chain ready to use
  - Software to manage configuration and analyze data
  - Preliminary results show proper operation of the system
- New FPGA readout
  - Ethernet base
  - Up to 1 Gbps throughput
  - Can possibly have more then one connection
  - No special hardware on PC side needed
  - Can easily electrically decouple two readout domains
    - By using optical transceivers

Thank you

But wait for online presentation