MSGCROC - funkcjonalność układu
Wstępne testy

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MSGCROC – Micro-Strip Gas Chamber ReadOut Chip

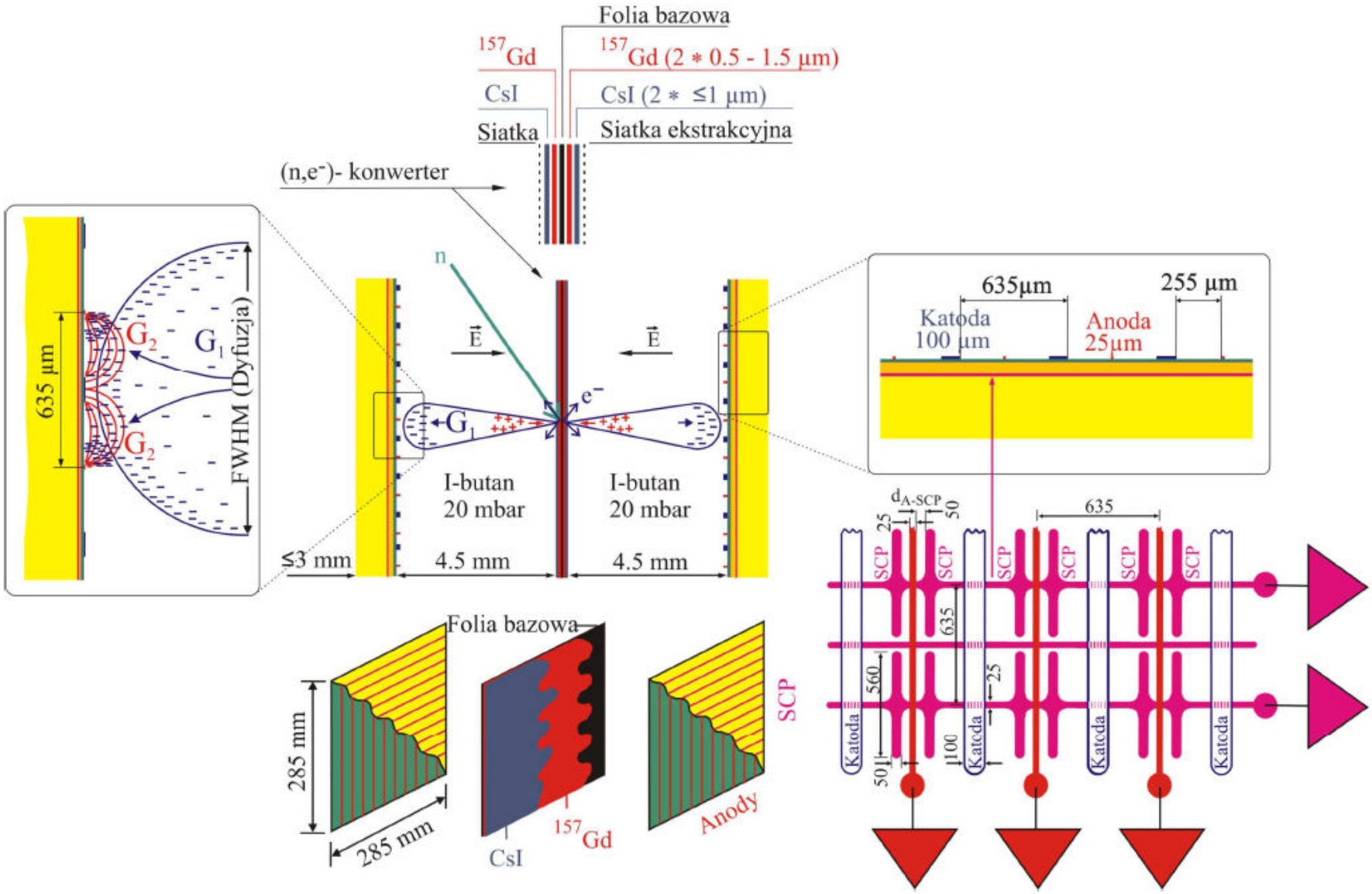
DETNI – DETectors for Neutron Instrumentation

NMI3 – Integrated Infrastructure Initiative for Neutron Scattering and Muon Spectroscopy

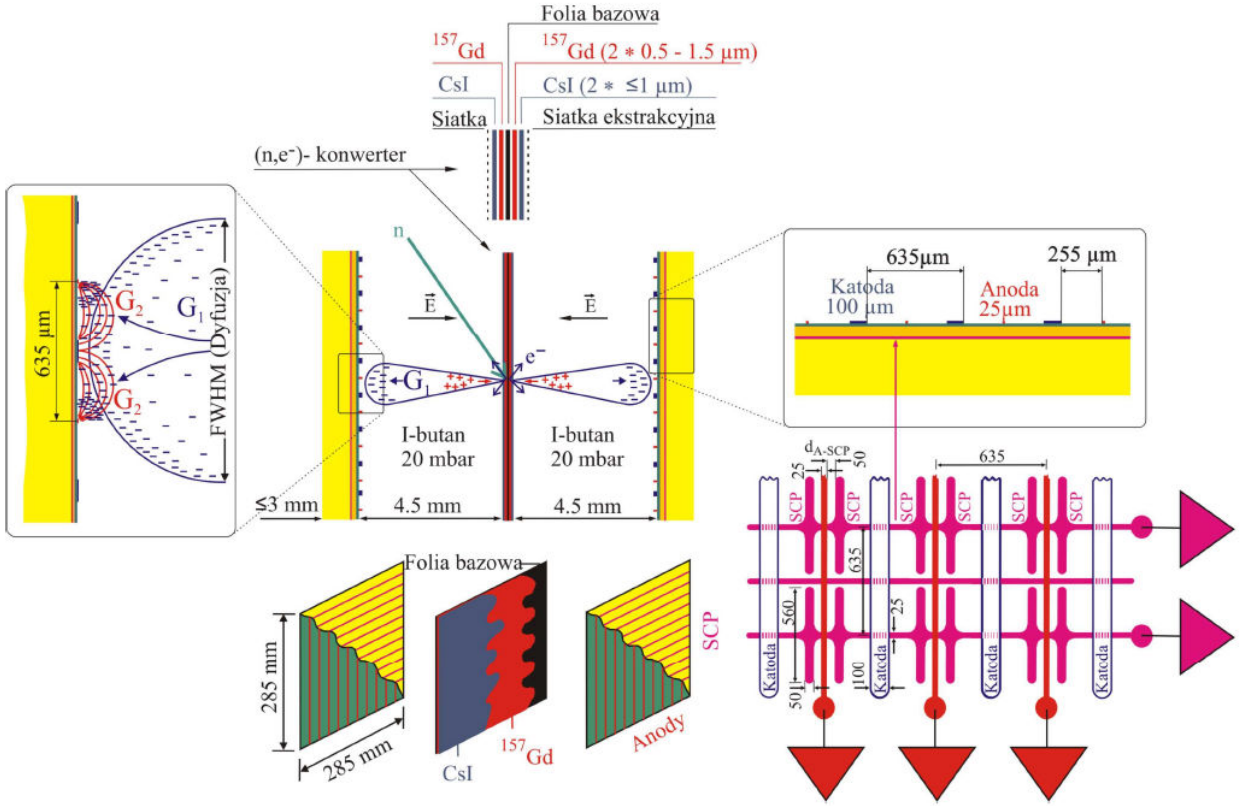
Plan

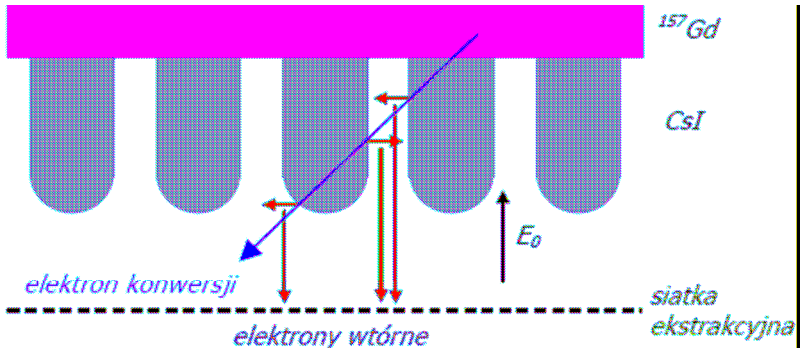
- **Przeznaczenie układu scalonego i założenia projektowe**
- **Układ pomiarowy**
- **Parametryzacja analogowa**
  - przetworniki cyfrowo-analogowe (dyskryminacja)
  - korekta offsetu (trimming)
  - kanał energetyczny (slow shaper)
  - kanał czasowy (fast shaper)
- **Parametryzacja czasowa**
- **Pomiary ze źródłem promieniowania**

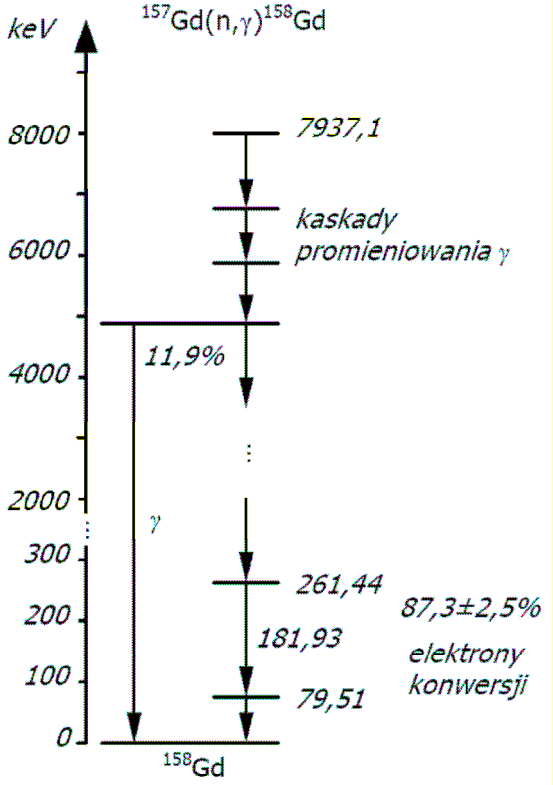
^{157}Gd/CsI MSGC - detektor neutronów



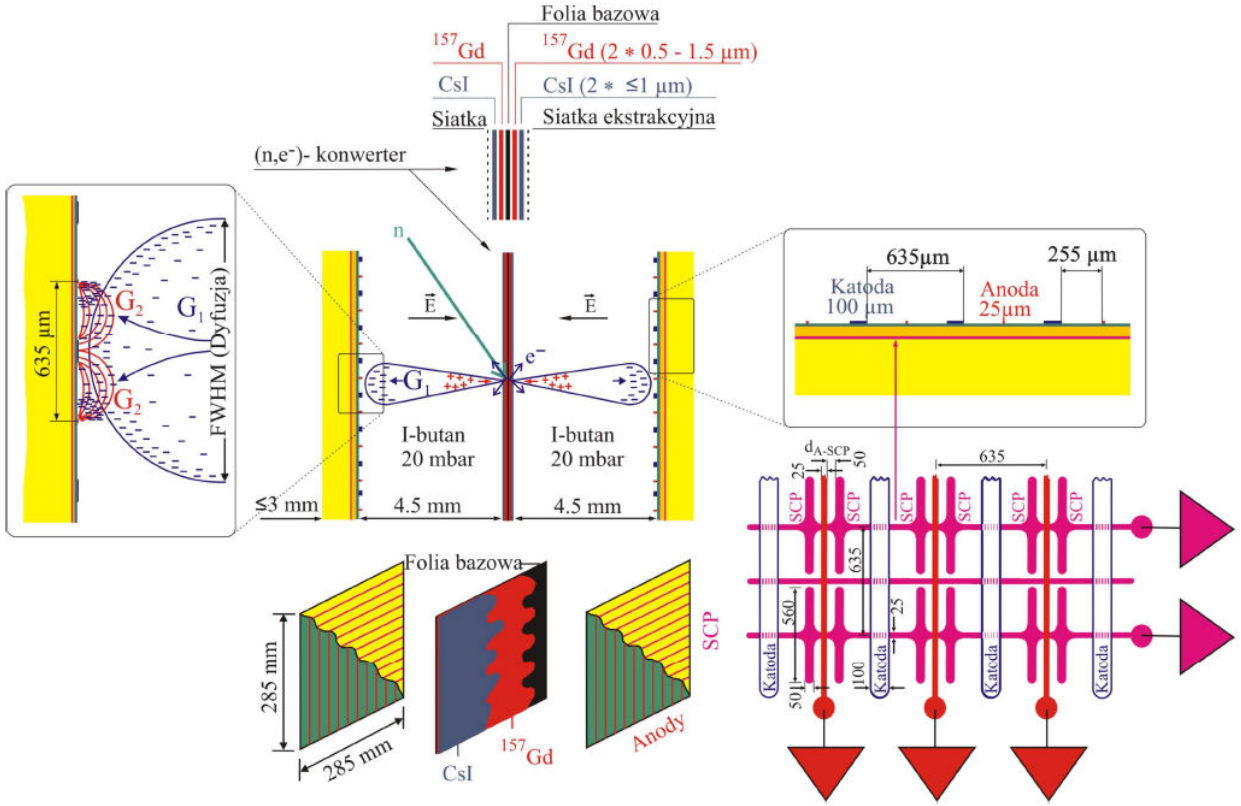
^{157}Gd/CsI MSGC - detektor neutronów





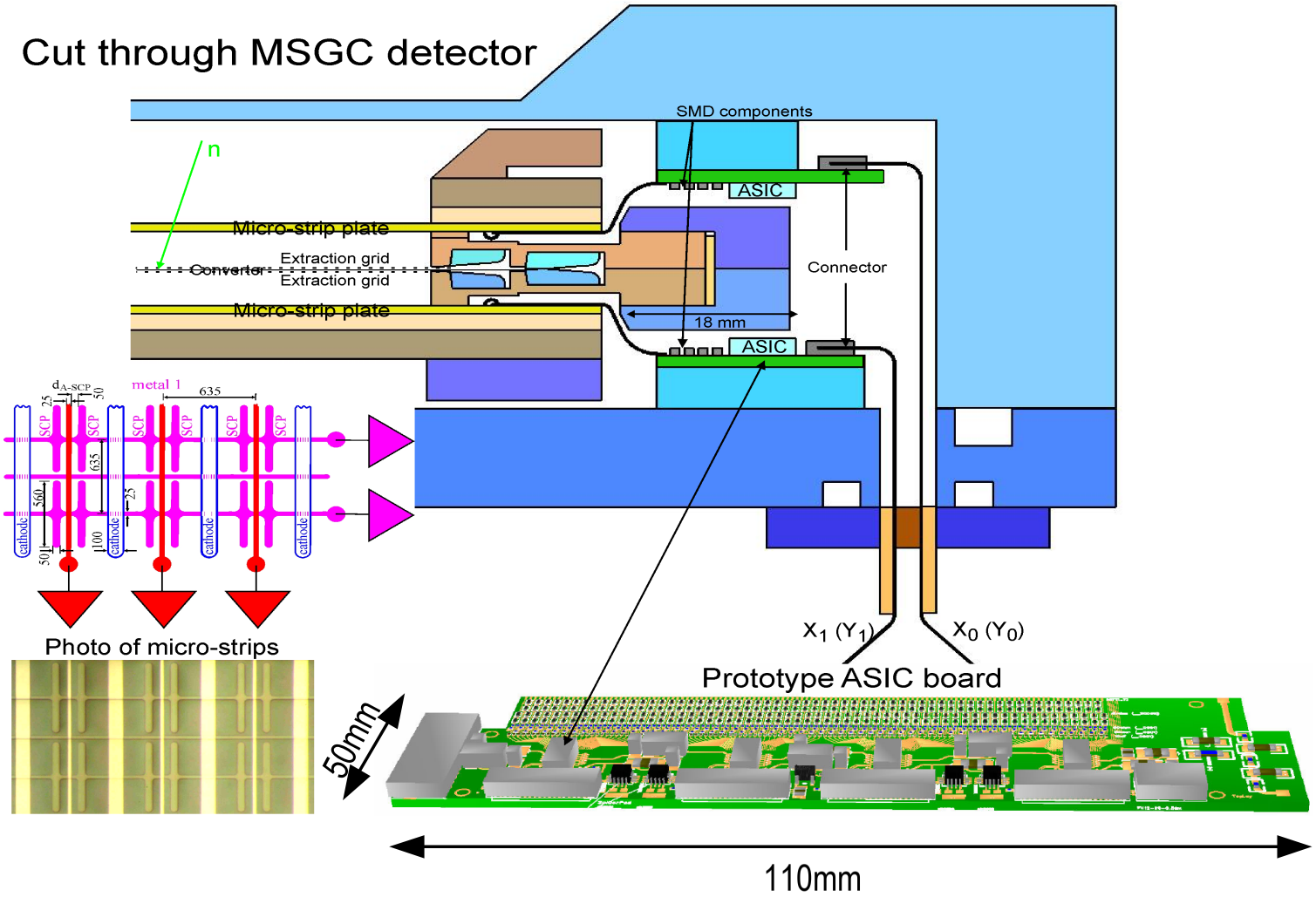


^{157}Gd/CsI MSGC - detektor neutronów



Segment size	285x285 mm^2 (active: 254x254 mm^2)
Module size	570x570 mm^2 (2x2 segments)
Micro-strip pitch	635µm
No. of micro-strip per segment	400x400 (121x121) !!!
No. of ASICs (32 ch.) per segment	13x13 (4x4) !!!

^{157}Gd/CsI MSGC – system odczytowy



^{157}Gd/CsI MSGC – system odczytowy

Cut through MSGC detector

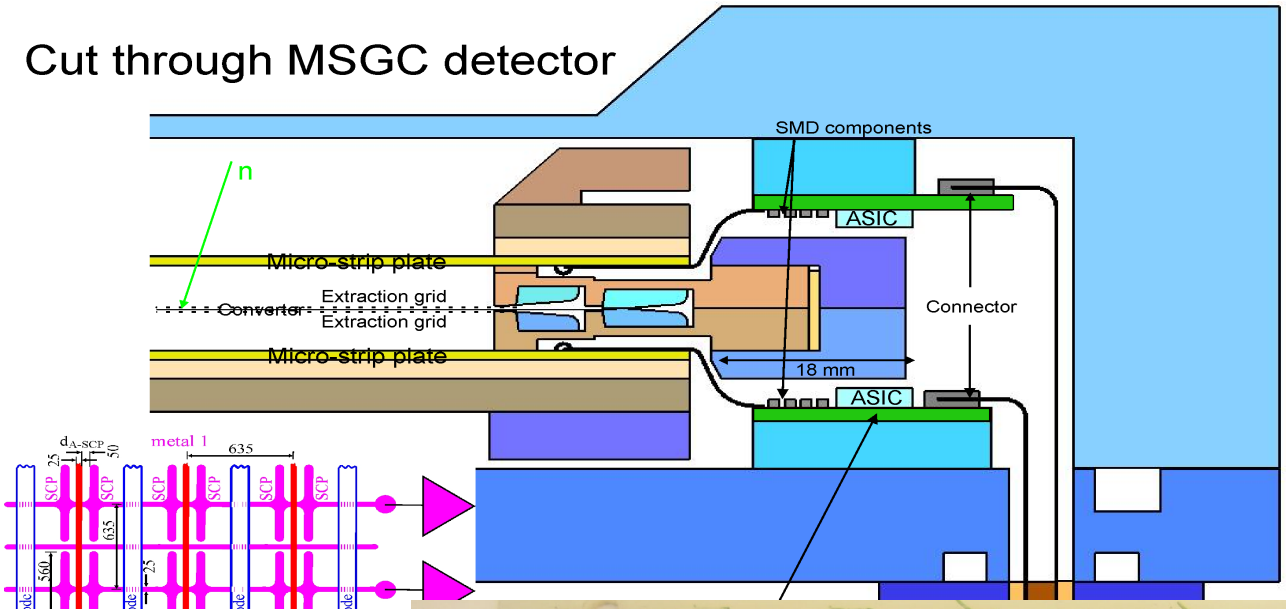
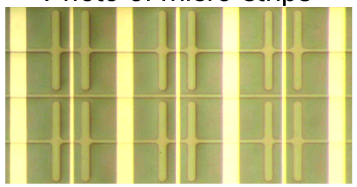
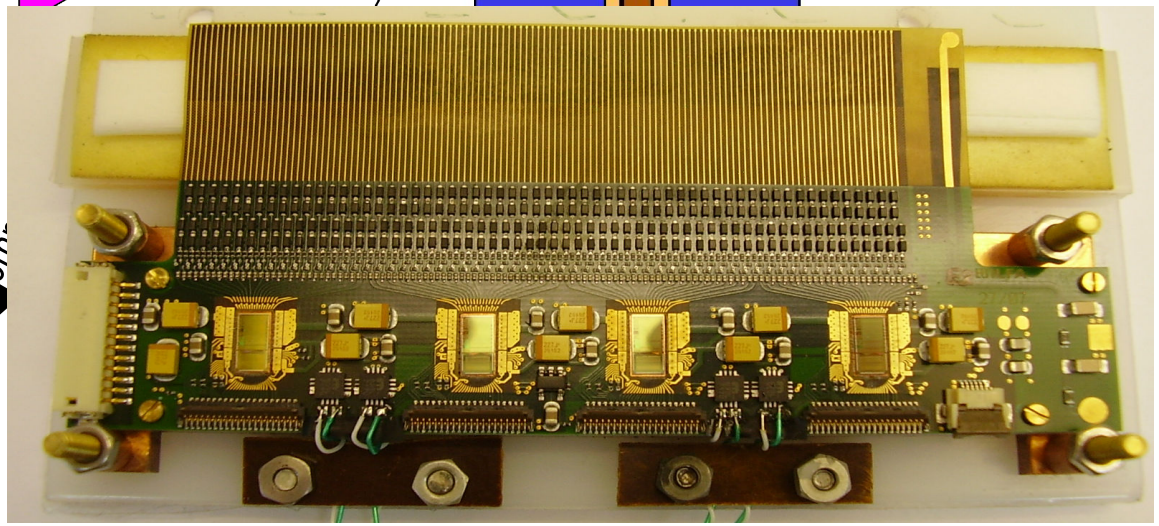
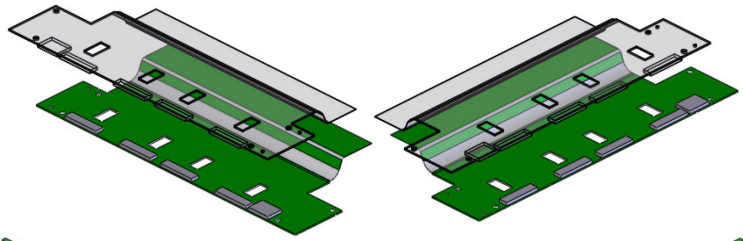


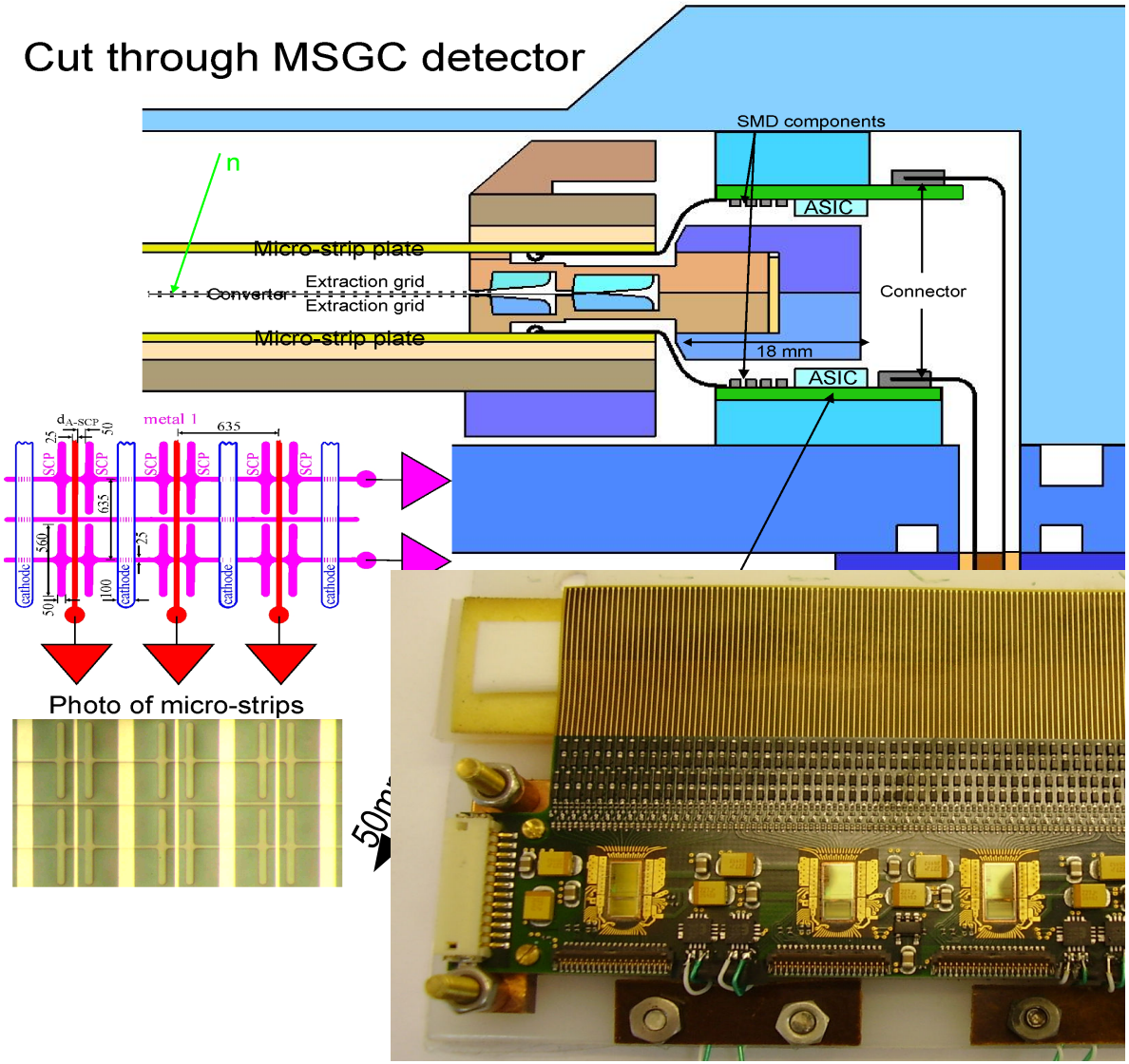
Photo of micro-strips

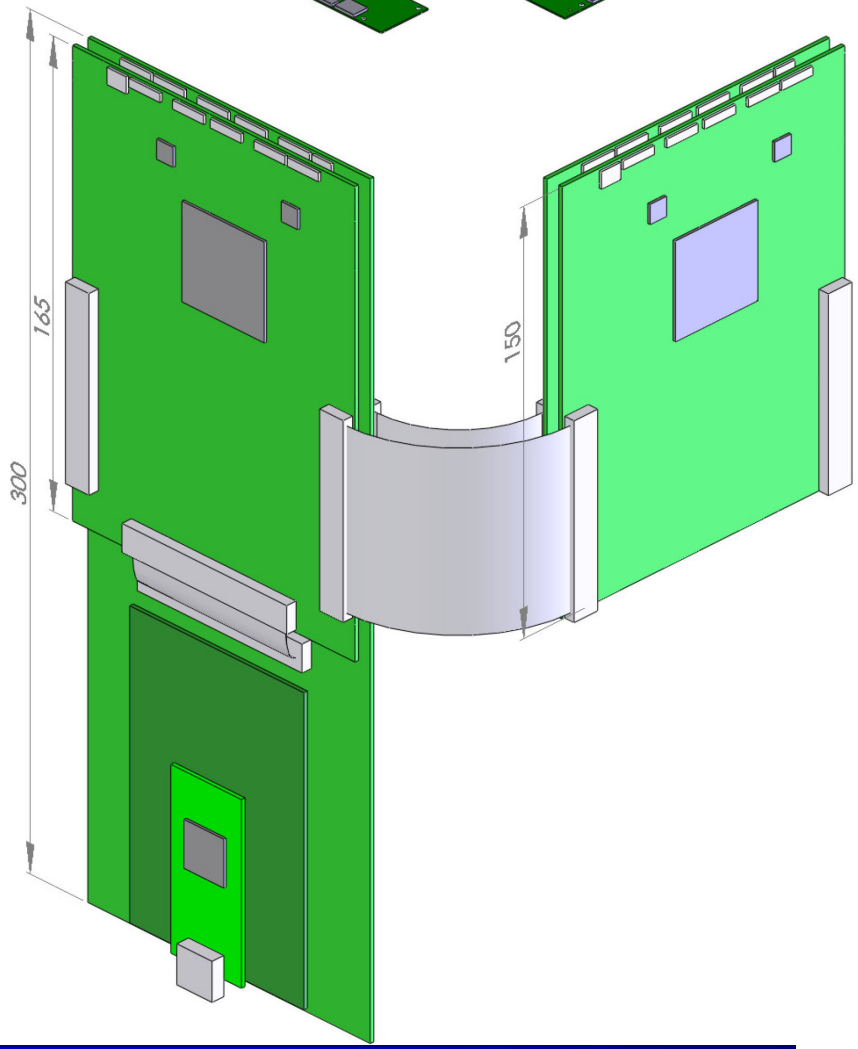




^{157}Gd/CsI MSGC – system odczytowy



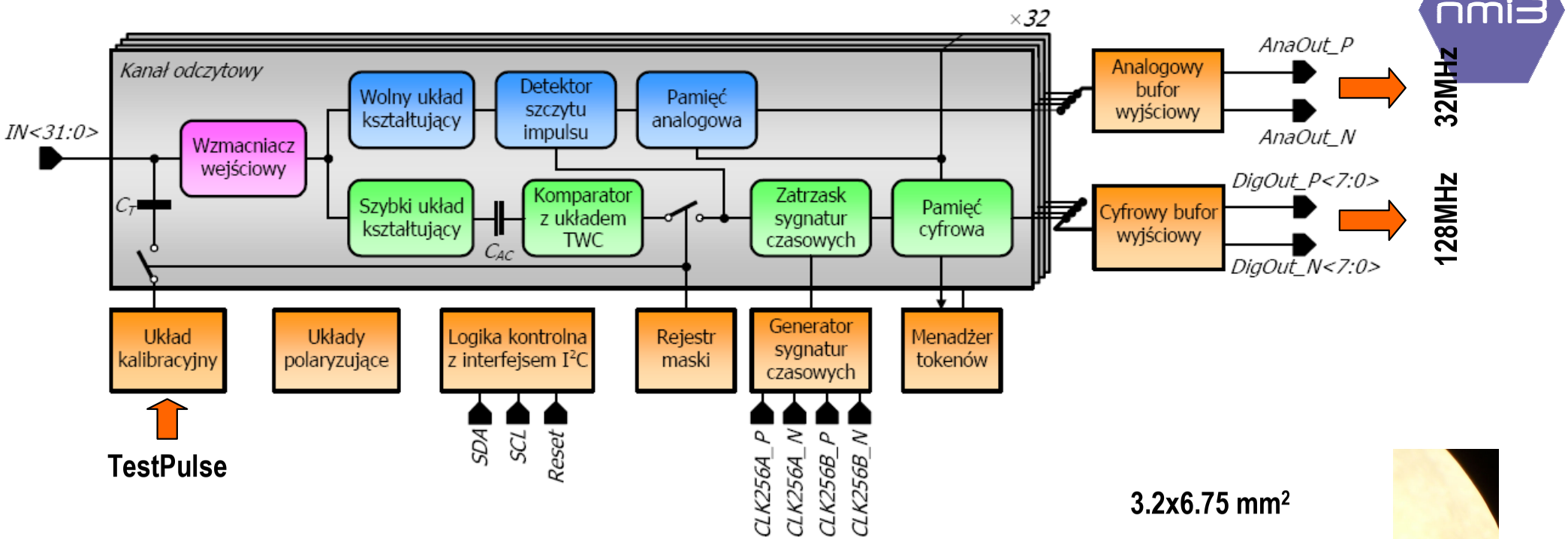




MSGCROC – założenia projektowe

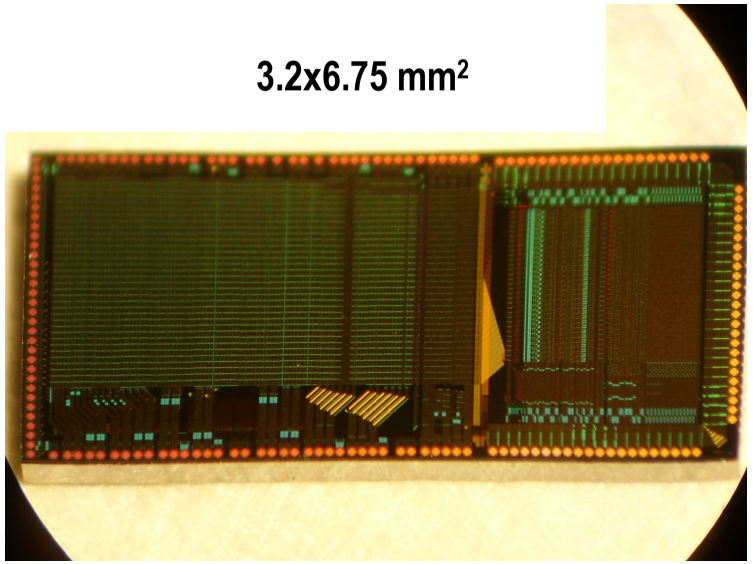
Parametry ekstrahowane z sygnału wejściowego	X/Y, T, E_X/E_Y
Liczba kanałow na jeden układ	32
Średnia częstość zliczeń na jeden kanał [1/s]	$9 \cdot 10^5$
Średnia częstość zliczeń na segment [1/s]	~ 10^8
Ładunek na wejściu [e-]	$2 \cdot 10^5$ (32fC) ÷ $5 \cdot 10^6$ (800fC)
Prog dyskryminacji	$5\sigma = 10^4$ e- (3.2fC)
Przedział czasowy dla koincydencji zdarzeń X/Y [ns]	2
Czas kształtowania w torze czasowym [ns]	25
Czas martwy [ns]	~ 120
ENC (σ rms) [e-] @ C_{det}=30pF	~ 2000 (0.32fC)

MSGCROC – architektura układu scalonego

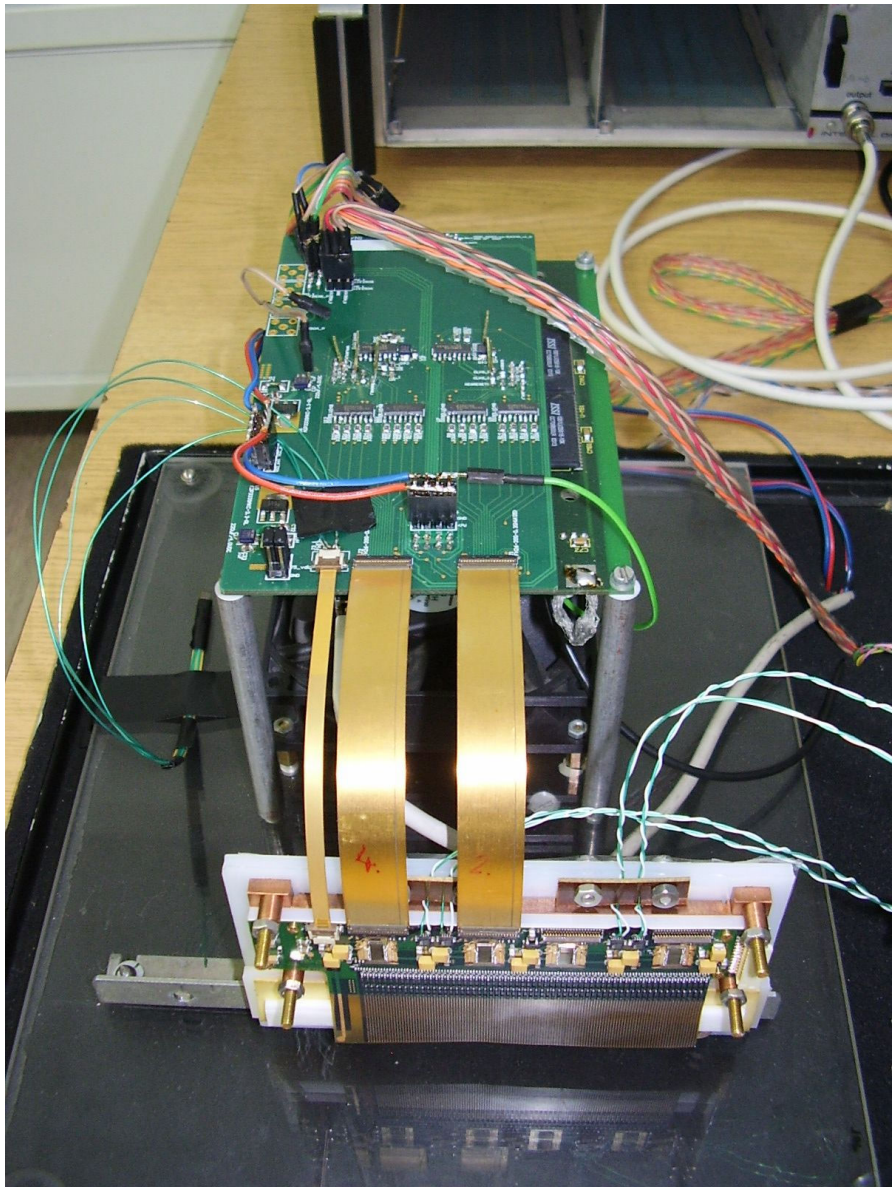


- **obie polarności** (pos. & neg.)
- **T_{peak}=25ns (fast shaper), T_{peak}=85ns (slow shaper)**
- **pamięć analogowa (4 – FIFO)**
- **pamięć cyfrowa (4 – FIFO)**
- **dyskryminator: time walk < 2 ns, jitter < 1 ns FWHM**
- **5-bit trimming DAC**

3.2x6.75 mm²



Układ pomiarowy



SUCIMA - VIRTEX II XC2V1000 4FG456CES (324 I/O)

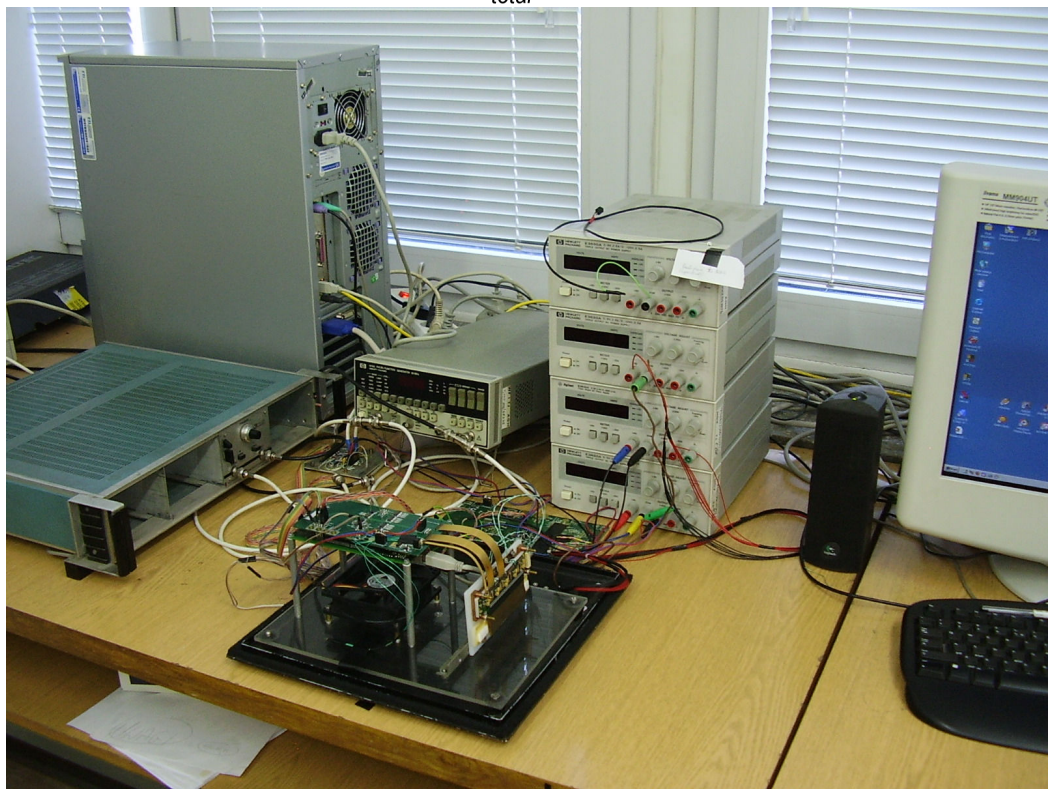
+ ADC 12-bit, 65MSPS (AD9226)

VDDA= 3.3VDC, I_{VDDA}=250mA / ASIC

VDDA_buf= 3.3VDC, I_{VDDA_buf}=2.4mA / ASIC

VDD= 3.3VDC, I_{VDD}=42mA / ASIC @ $f_{clk256AB}$=256MHz

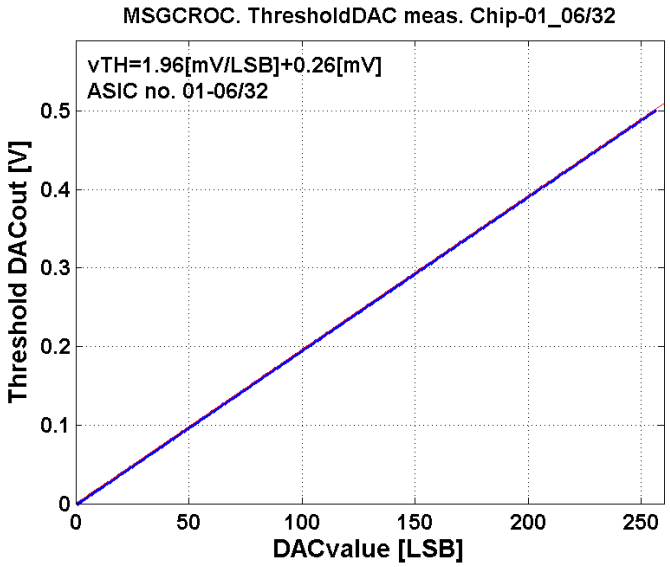
$P_{total} \approx 1W$ / ASIC

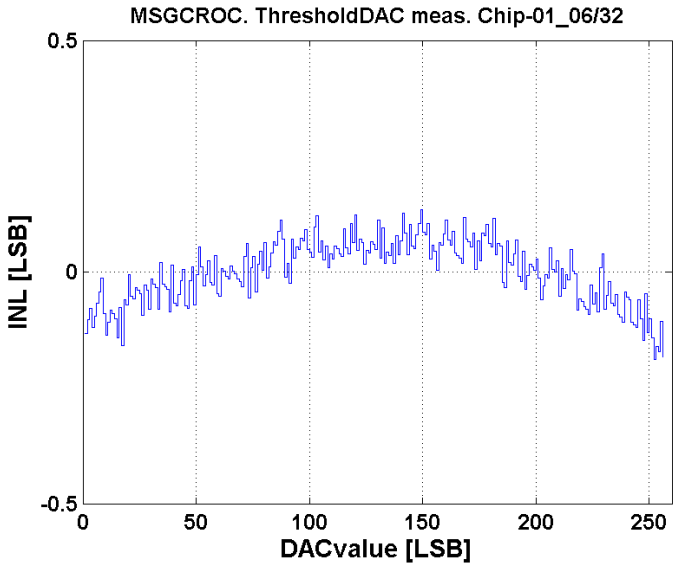


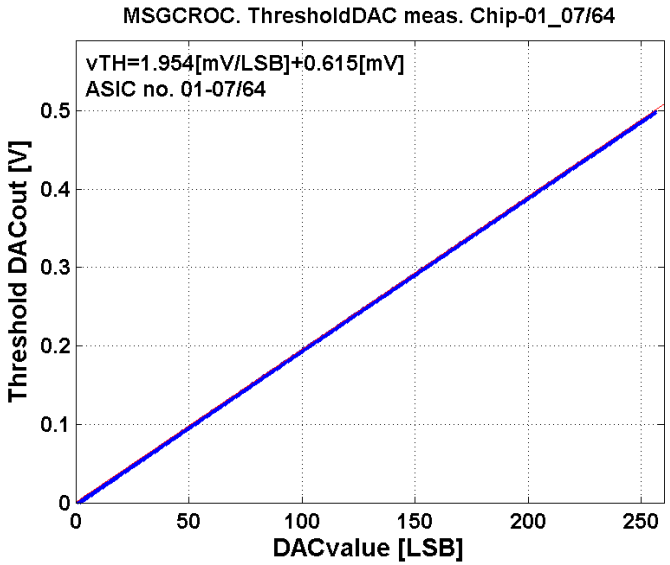
Przetworniki cyfrowo - analogowe (DACs)

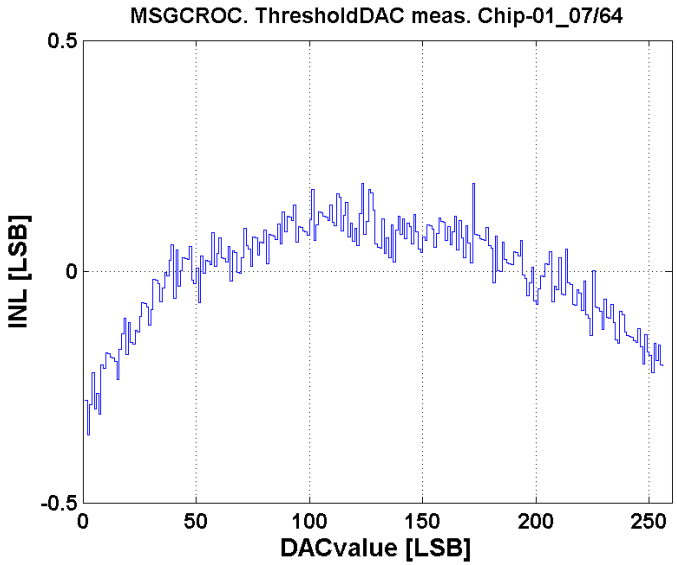
DAC Name	Type	Nominal	RealRange	Default value	DAC's LSB	Notes
iPRE	IDAC(8b)	(124LSB) 250 mA	(0; 506.9) mA	255 mA	1.9714 mA	Preamplifier current (bias)
iSH	IDAC(8b)	(122LSB) 100 mA	(0; 206.5) mA	103 mA	0.8061 mA	Shapers current (bias)
iPDH	IDAC(8b)	(98LSB) 80 mA	(0; 206.5) mA	103 mA	0.8061 mA	PDH current (bias)
vPDH	VDAC(8b)	(101LSB) 740 mV (extr.)	(0; 1.868) V	933 mV	7.3201 mV	PDH reset voltage
iCOMP	IDAC(8b)	(121LSB) 50 mA	(0; 103.7) mA	53.2 mA	0.4035 mA	Comparator current (bias)
iTWC	IDAC(8b)	(114LSB) 60 mA	(0; 133.0) mA	66.7 mA	0.5175 mA	TWC current (bias)
iINV	IDAC(8b)	(77LSB) 83 mA (extr.)	(0; 269.6) mA	134.6 mA	1.052 mA	TWC output stage current (2^{nd} TH stage)
iOUTBUF	IDAC(8b)	(117LSB) 148 mA	(0; 324.7) mA	165 mA	1.269 mA	Analog output buffer current (bias)
iDUR	IDAC(8b)	(78LSB) 50 mA	(0; 162.8) mA	81.2 mA	0.6363 mA	Monostable pulse duration time
vTH	VDAC(8b)	(14LSB) 30 mV	(0; 519.9) mV	267 mV	2.0348 mV	Threshold
cal	VDAC(8b)	(23LSB) 50fC(min)	(0; 470) fC	0 fC	1.8127 mV	C_{test}=1pF, calibration voltage step high
itrim	IDAC(5b)	(16LSB) 100 mA	(0; 188.5) mA	0 mA	6.0802 mA	Total range of IDAC divided by 49 in current mirror

DAC - dyskryminacja

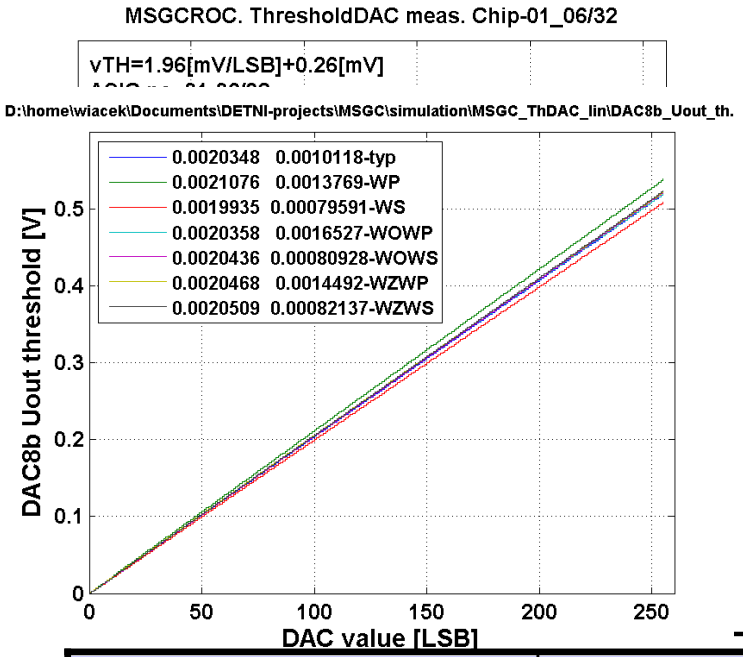


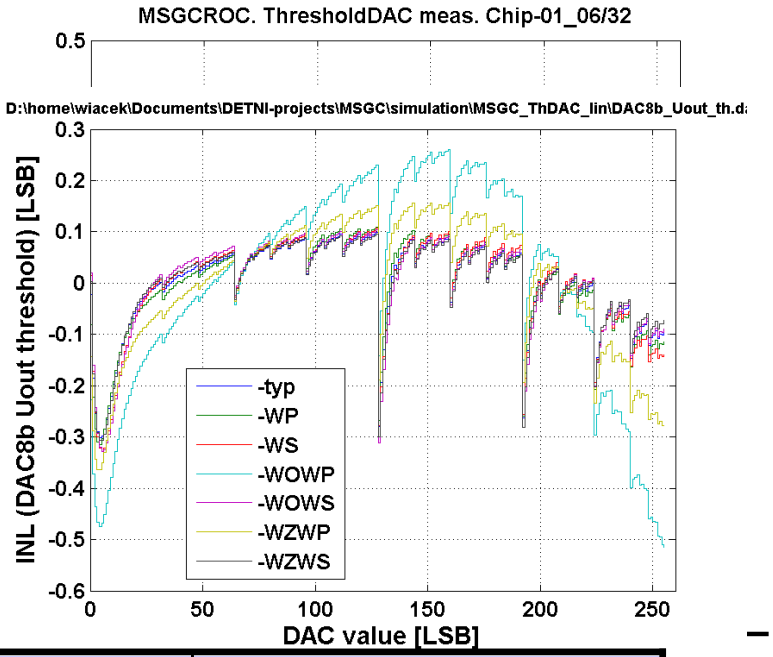




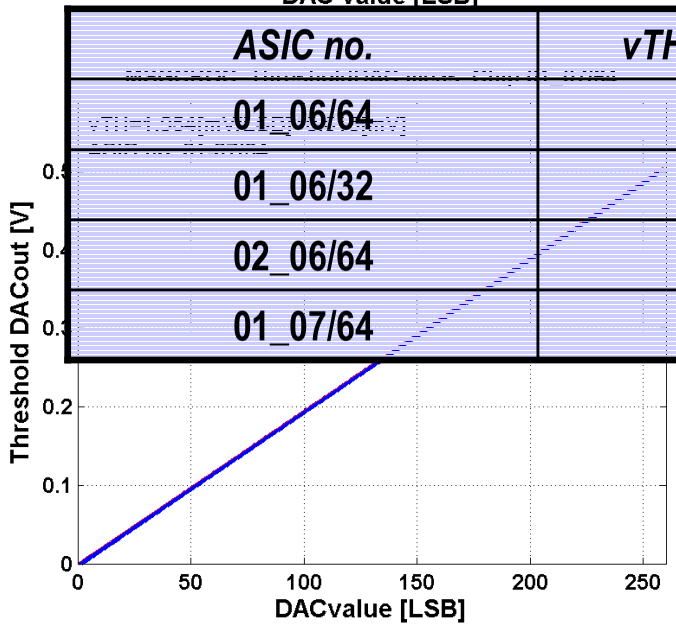


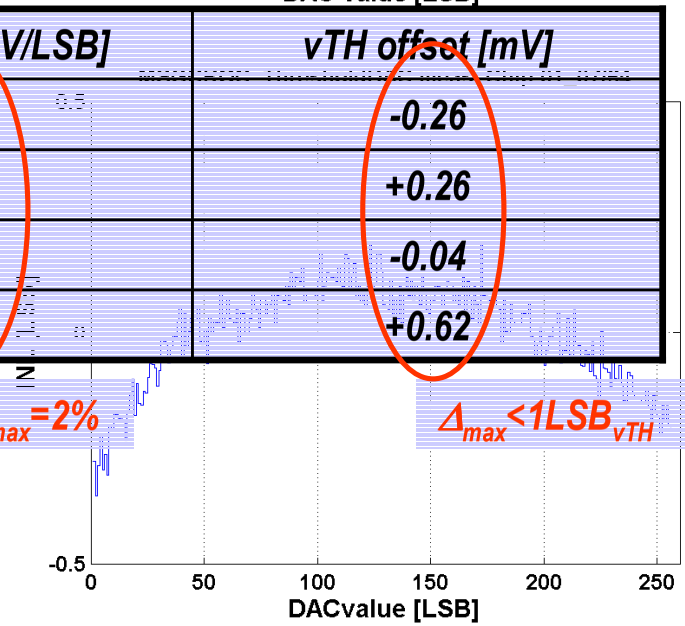
DAC - dyskryminacja





ASIC no.	vTH gain [mV/LSB]	vTH offset [mV]
01_06/64	1.98	-0.26
01_06/32	1.96	+0.26
02_06/64	1.99	-0.04
01_07/64	1.95	+0.62

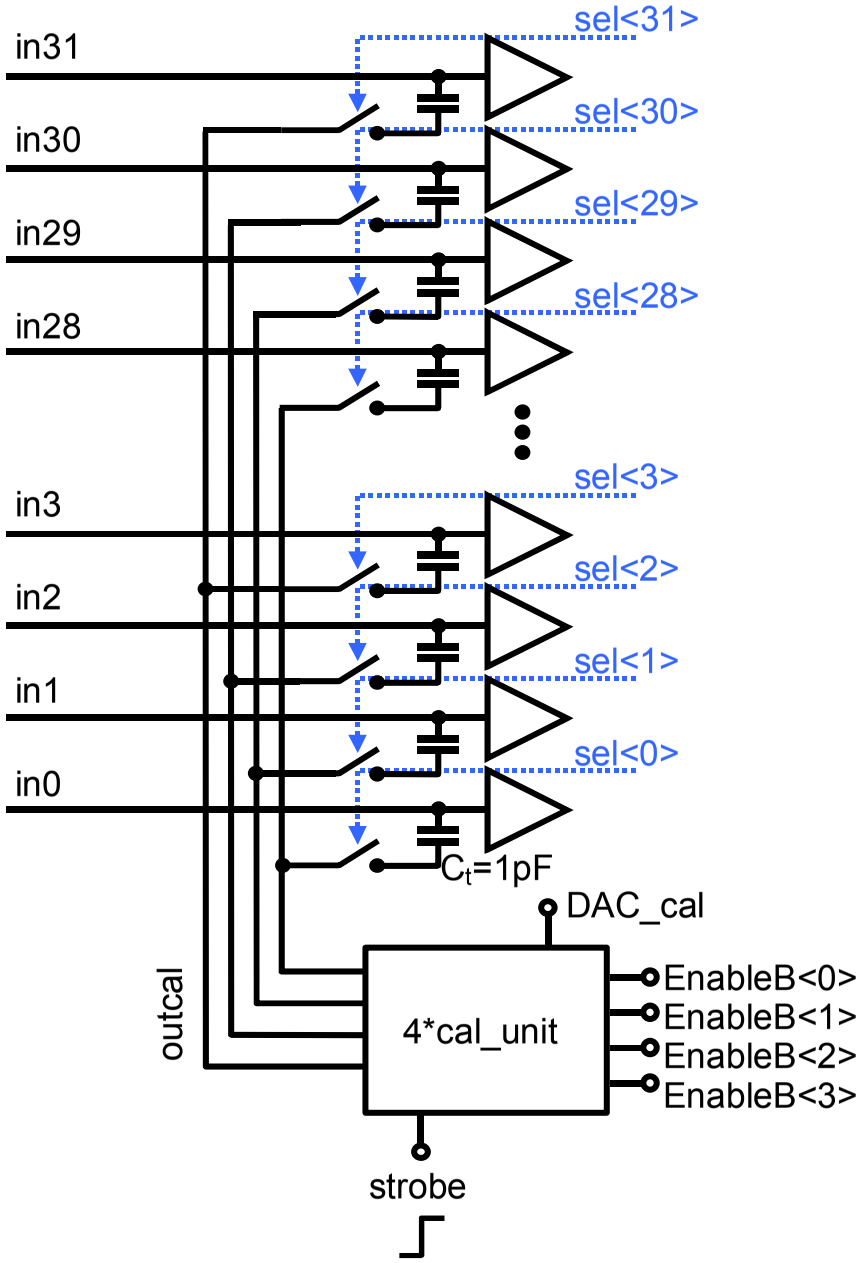




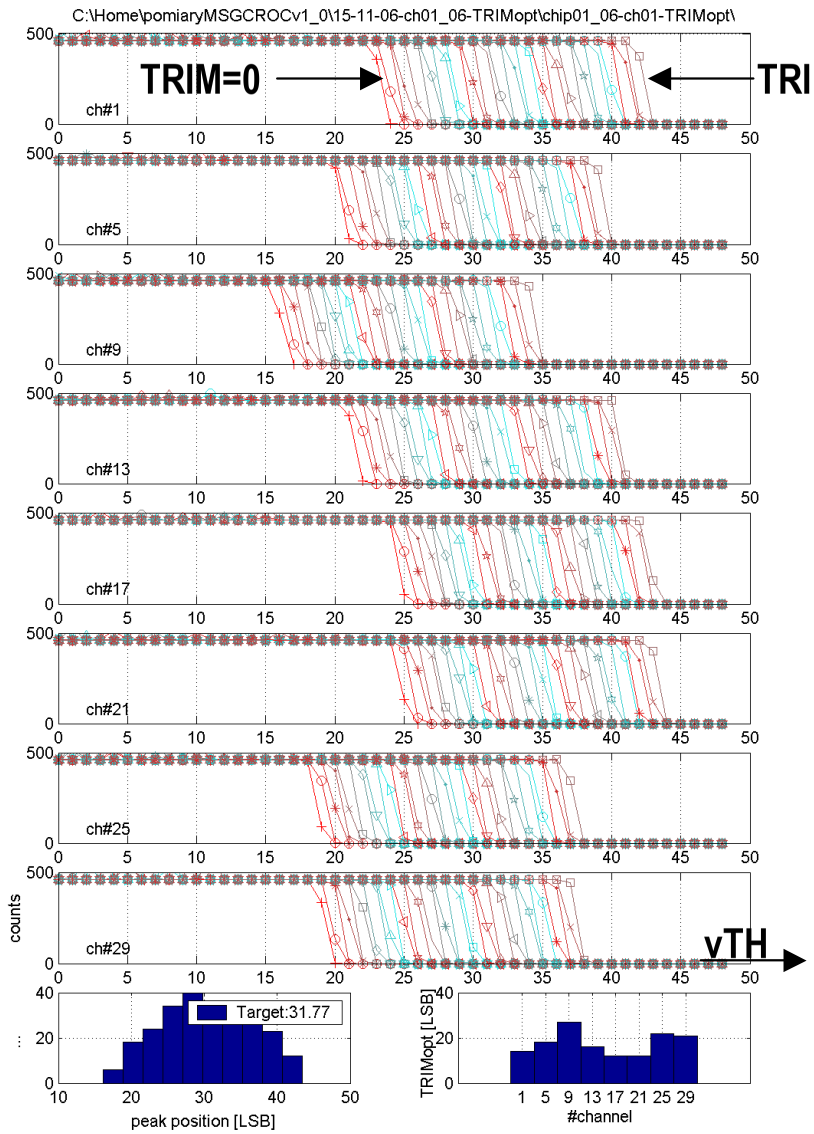
Δ_{max}=2%

Δ_{max}<1LSB$_{vTH}$

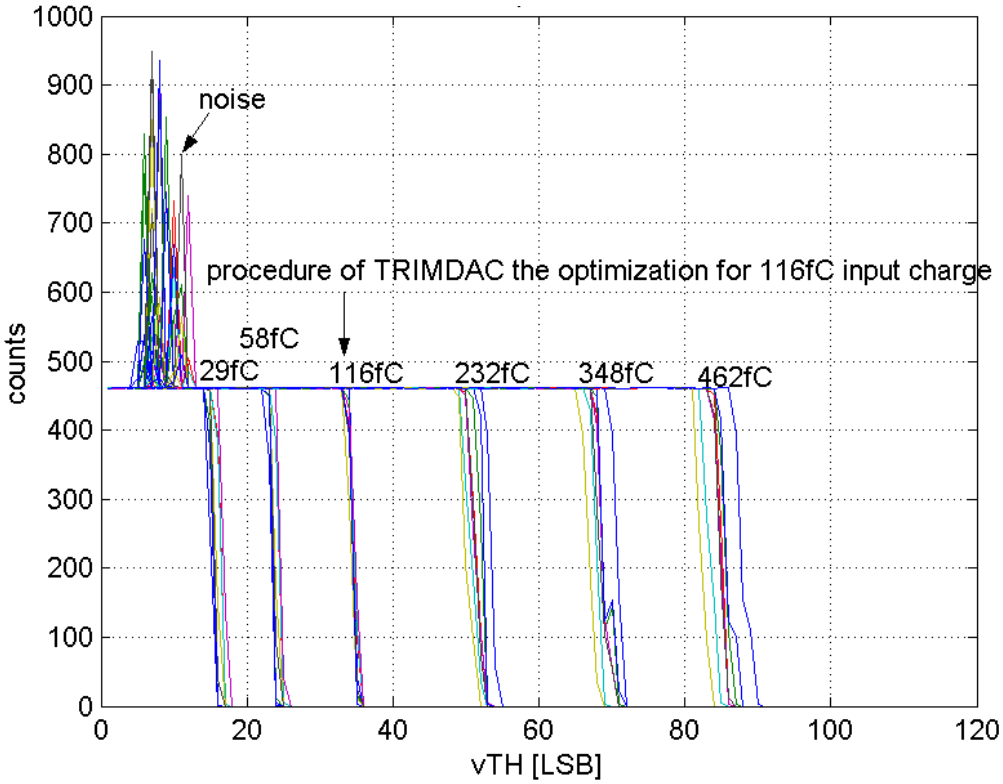
Układ kalibracyjny



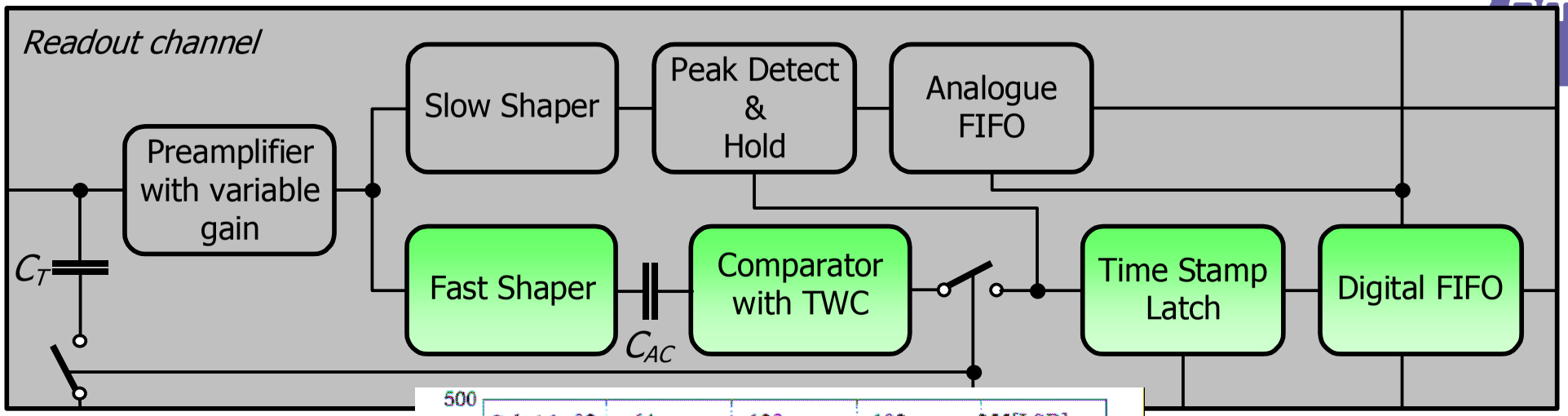
Korekta offsetu (trimming)

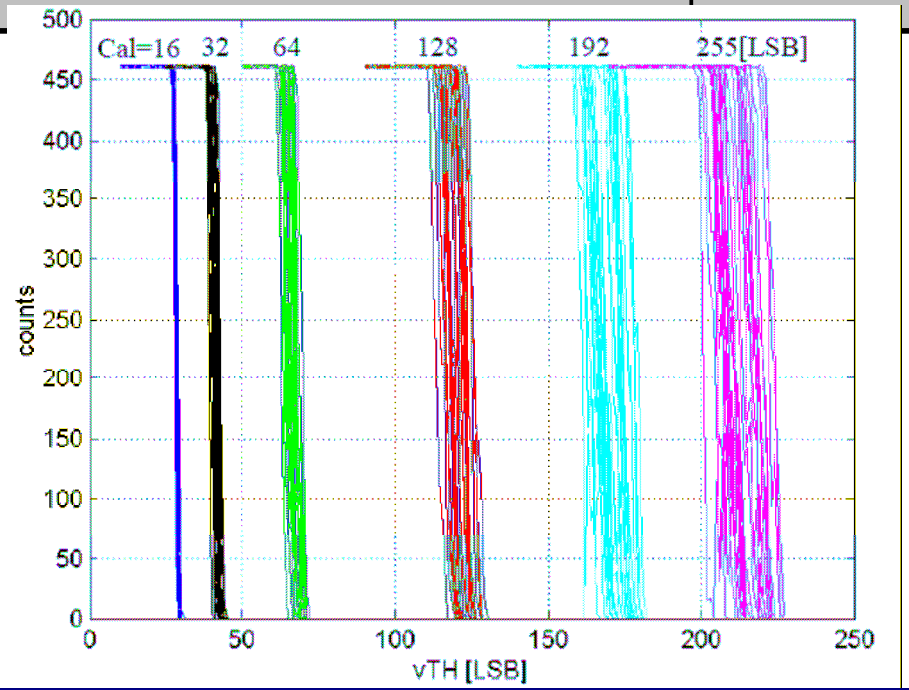


$vTRIM_{LSB} \approx 1.2$ mV ($vTH_{LSB} \approx 2$mV)

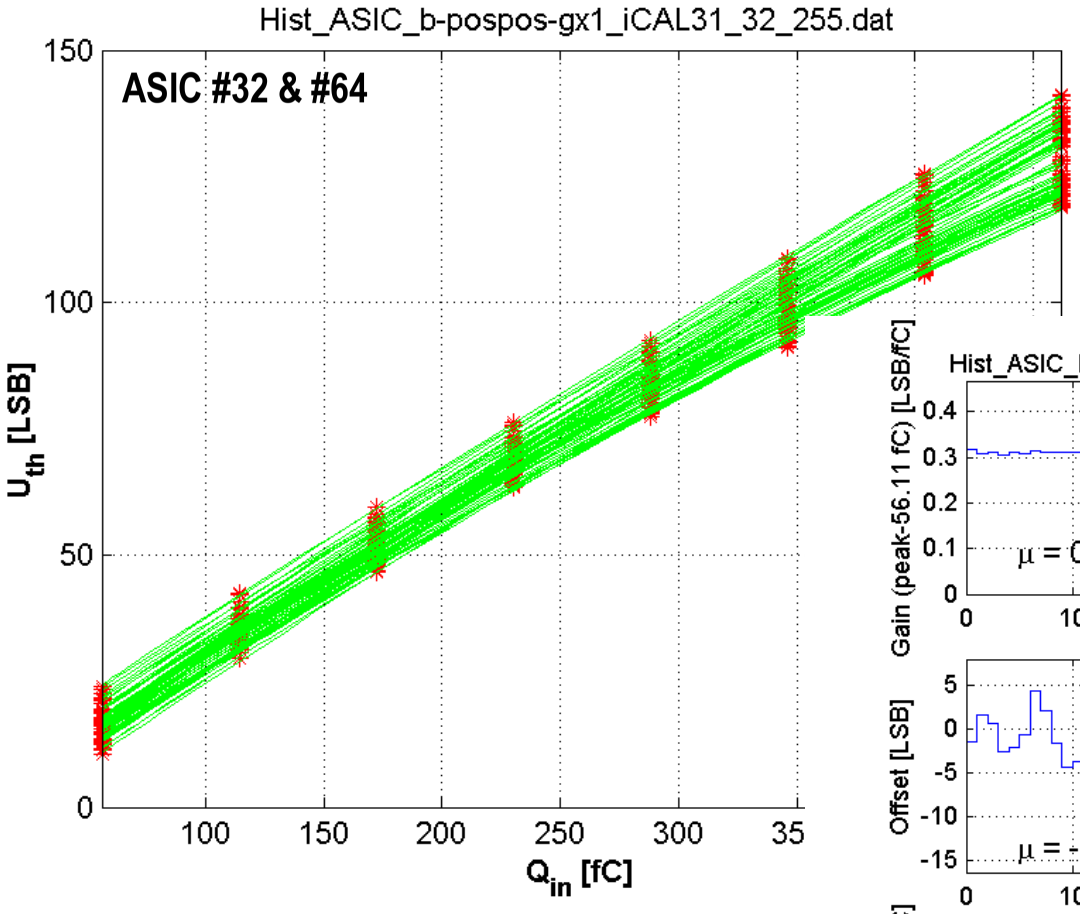


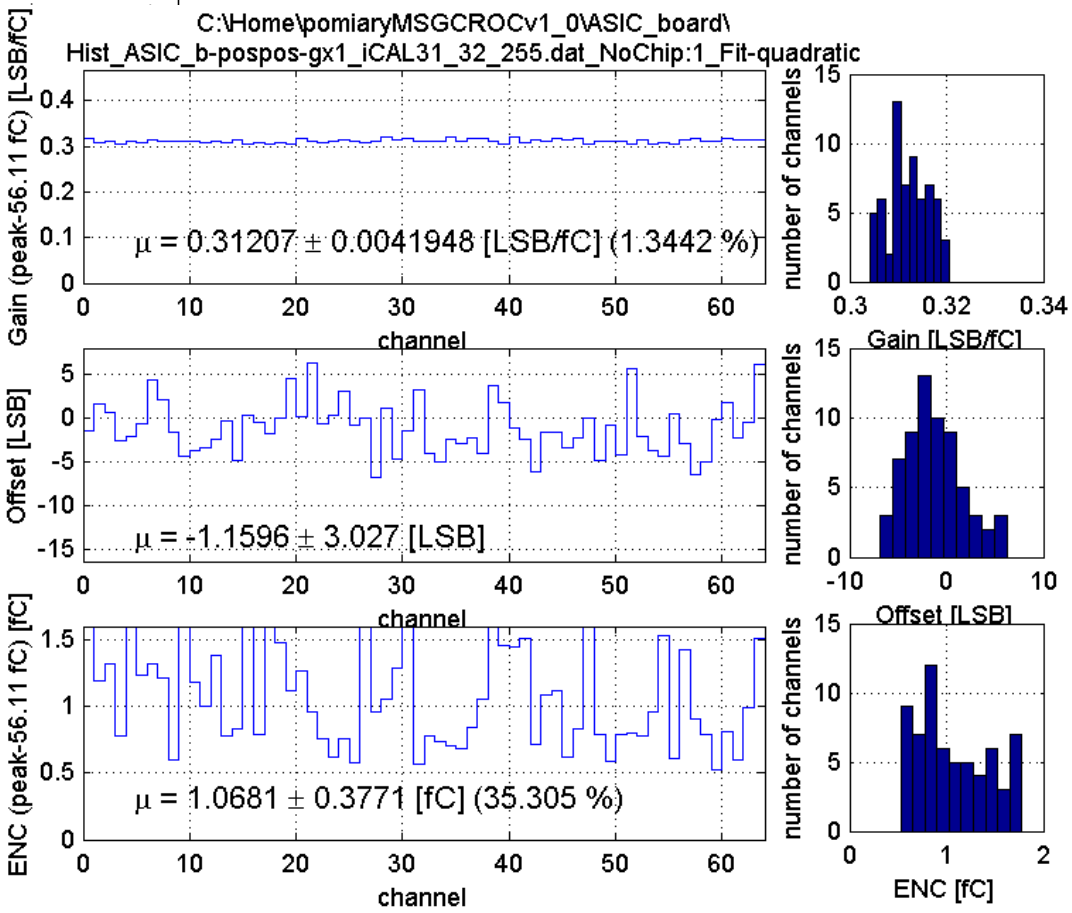
Kanał czasowy (fast shaper)



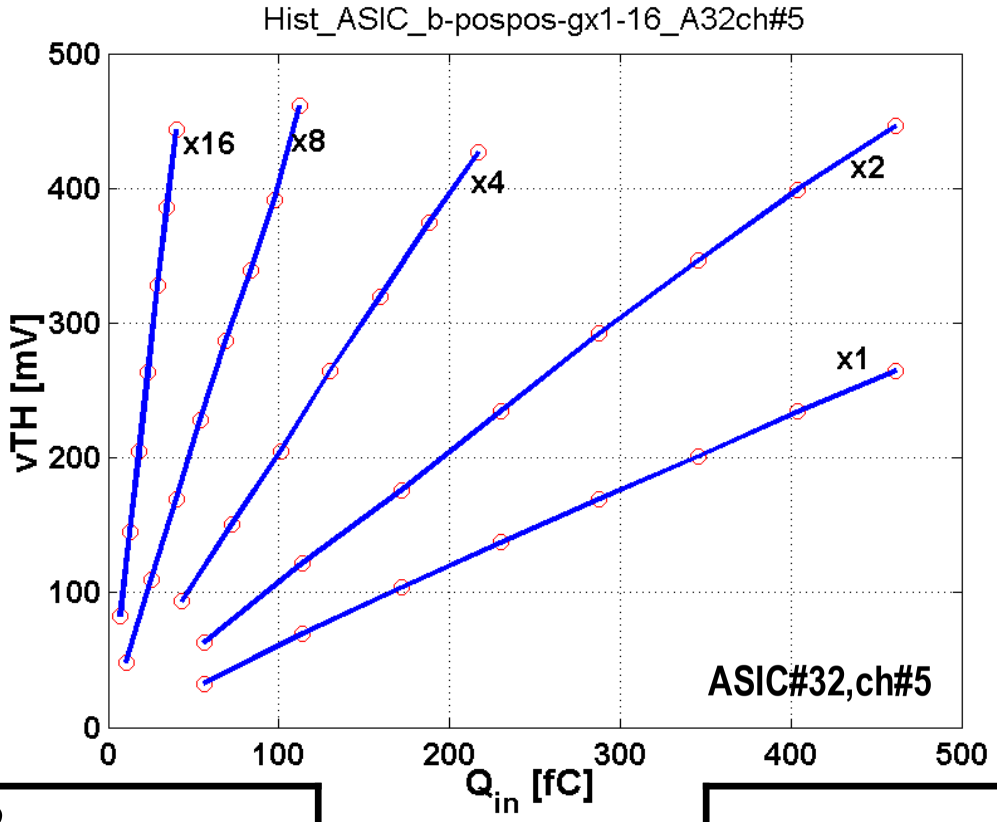


Kanał czasowy (fast shaper)



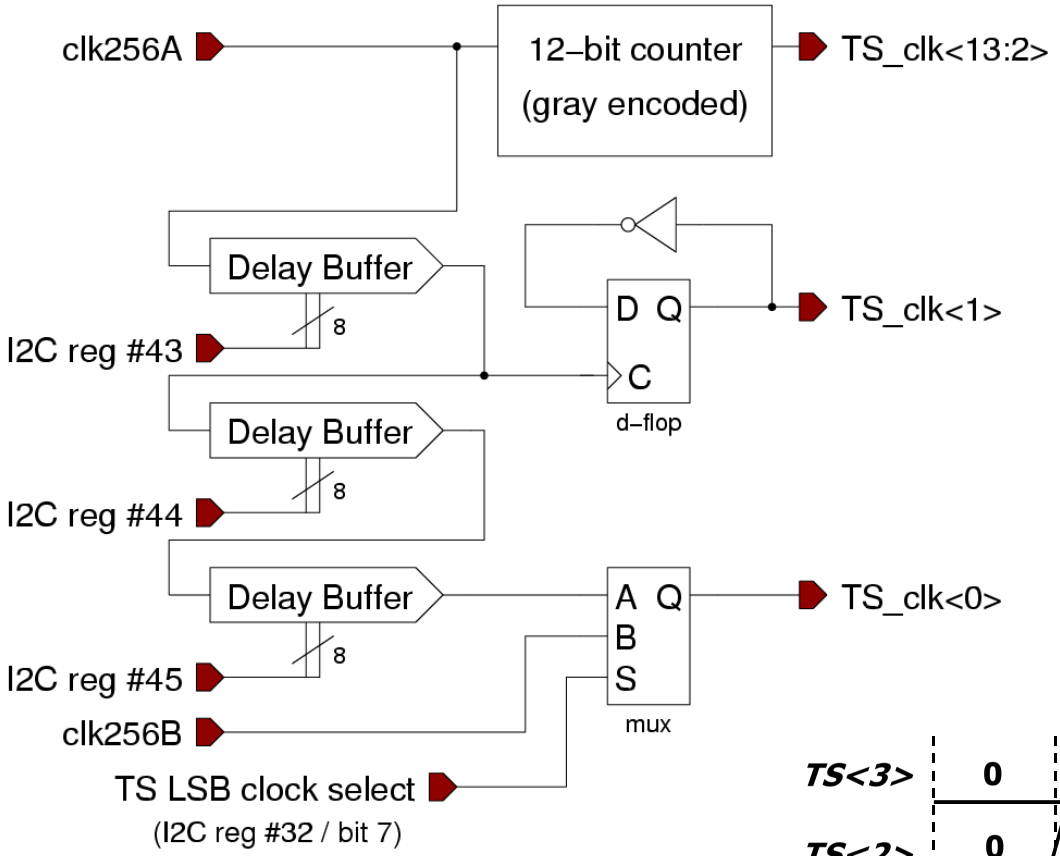


Kanał czasowy (fast shaper)



ASIC #32				ASIC #64		
Gain [mV/fC]	Offset [mV]	ENC [fC]		Gain [mV/fC]	Offset [mV]	ENC [fC]
0.6223	-1.035	1.16	x1	0.6259	-3.603	0.98
1.0613	2.423	0.69	x1.7	1.0020	5.193	0.65
2.0572	3.797	0.41	x3.3	1.8559	12.52	0.39
4.1832	5.370	0.197	x6.7	3.9216	7.380	0.22
11.609	0.025	0.082	x18.7	11.084	2.268	0.091

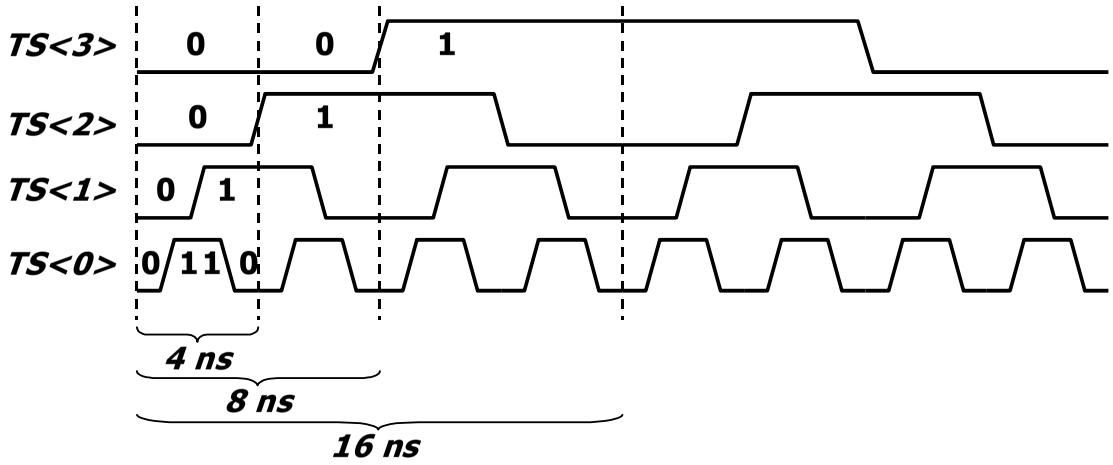
Parametryzacja czasowa



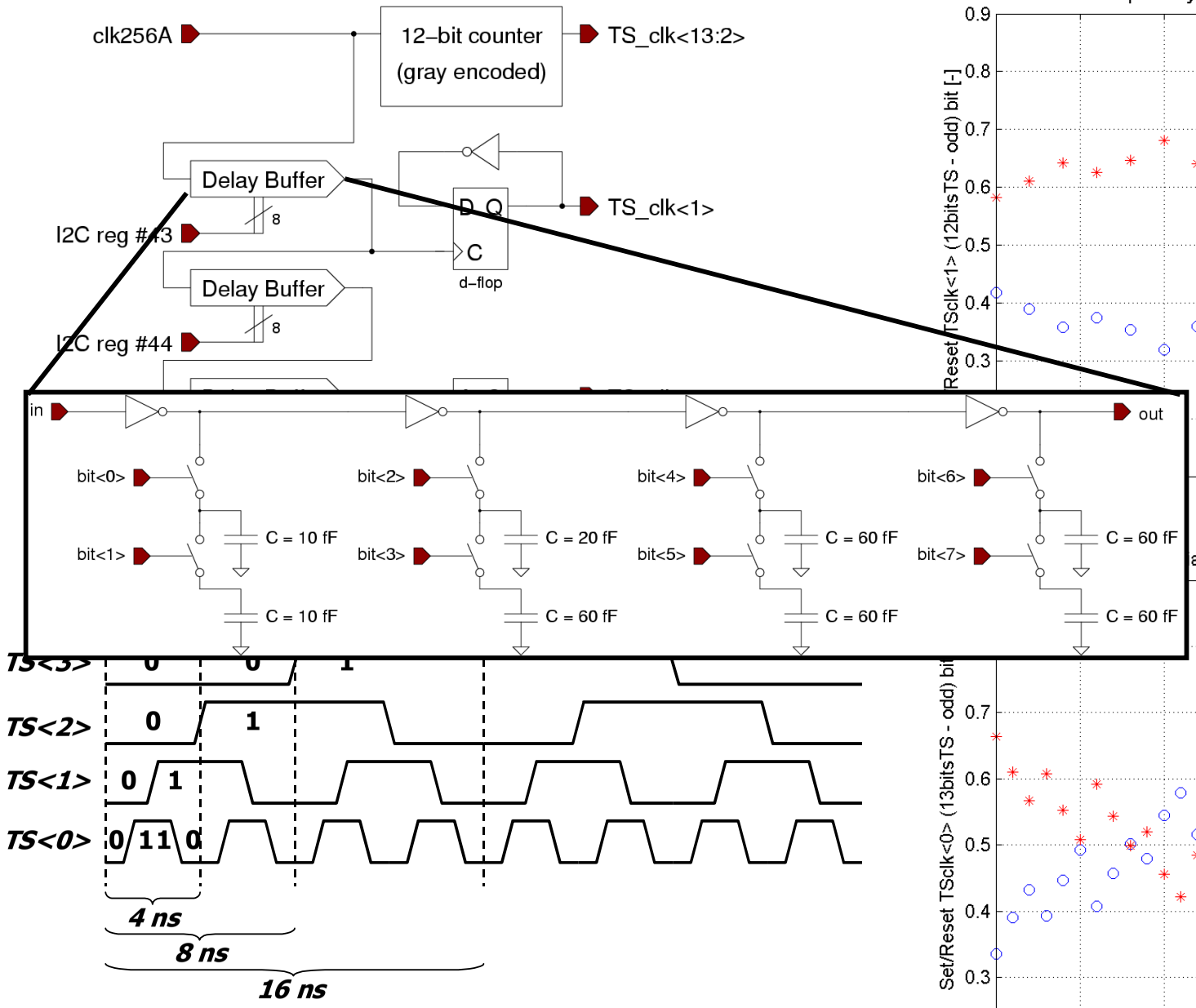
14-bit licznik sygnatur czasowych:

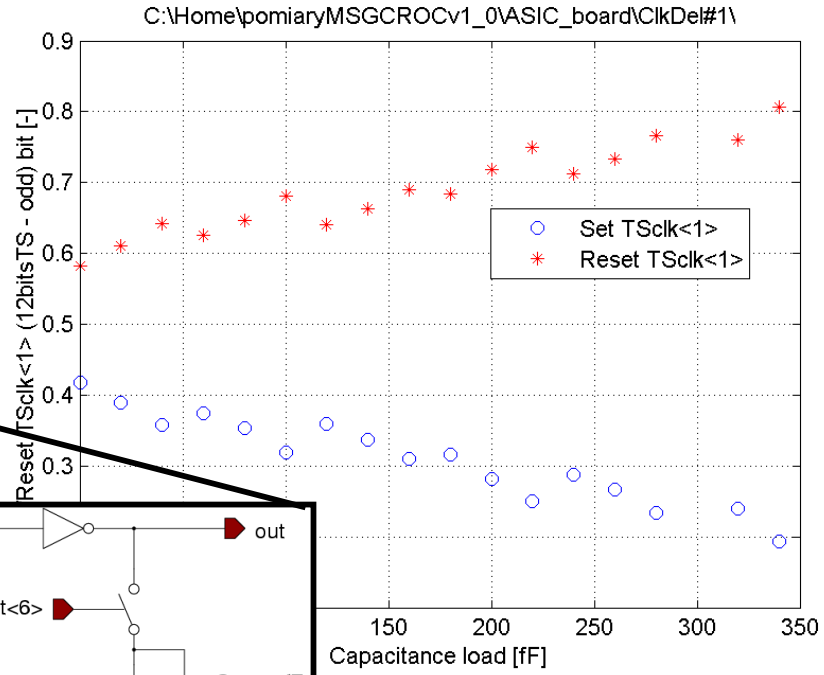
- **12-bit licznik kodu Gray'a,**
- **przerzutnik flip-flop,**
- **wejściowy zegar**

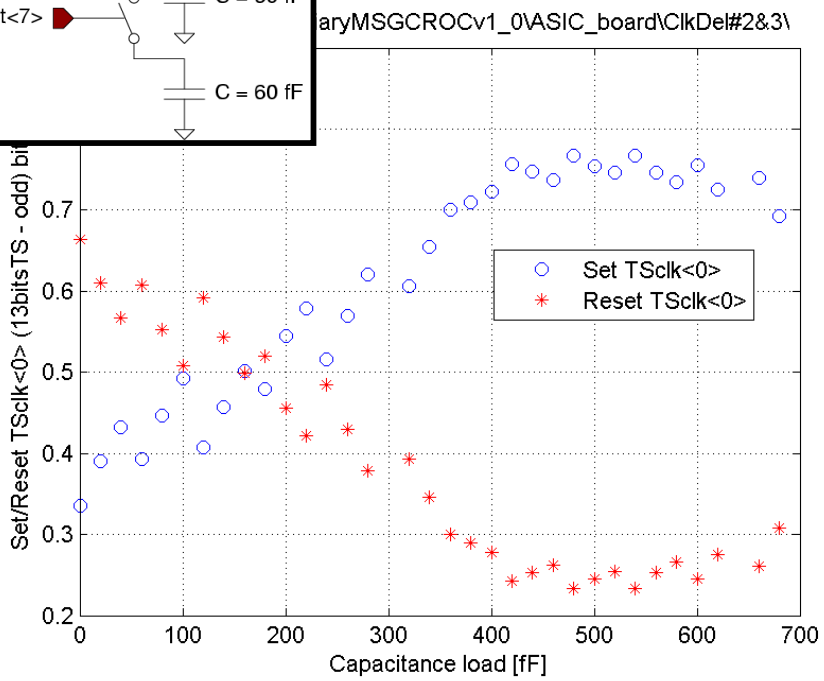
Dla wejściowego zegara 256MHz rozdzielczość czasowa: ~1ns



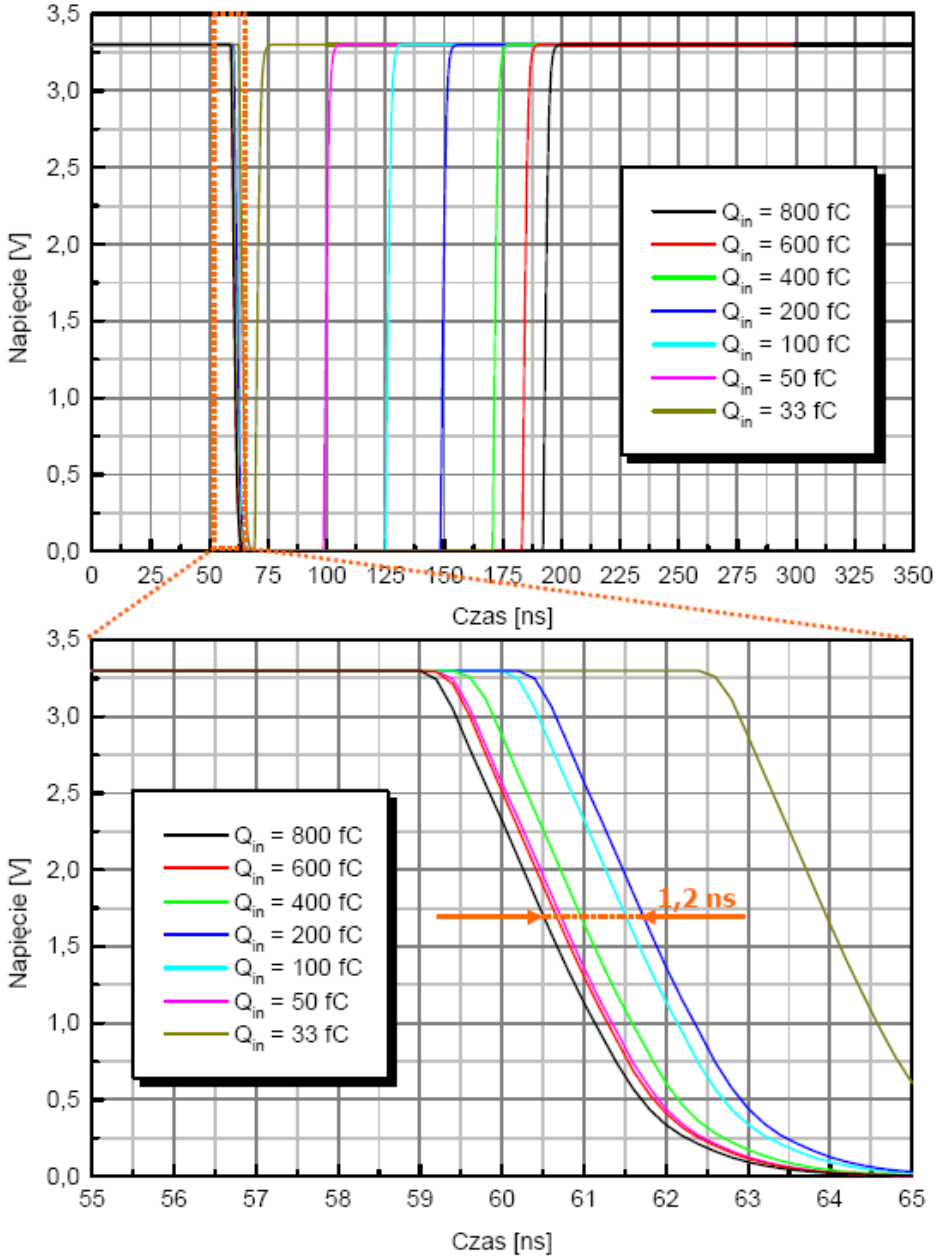
Parametryzacja czasowa



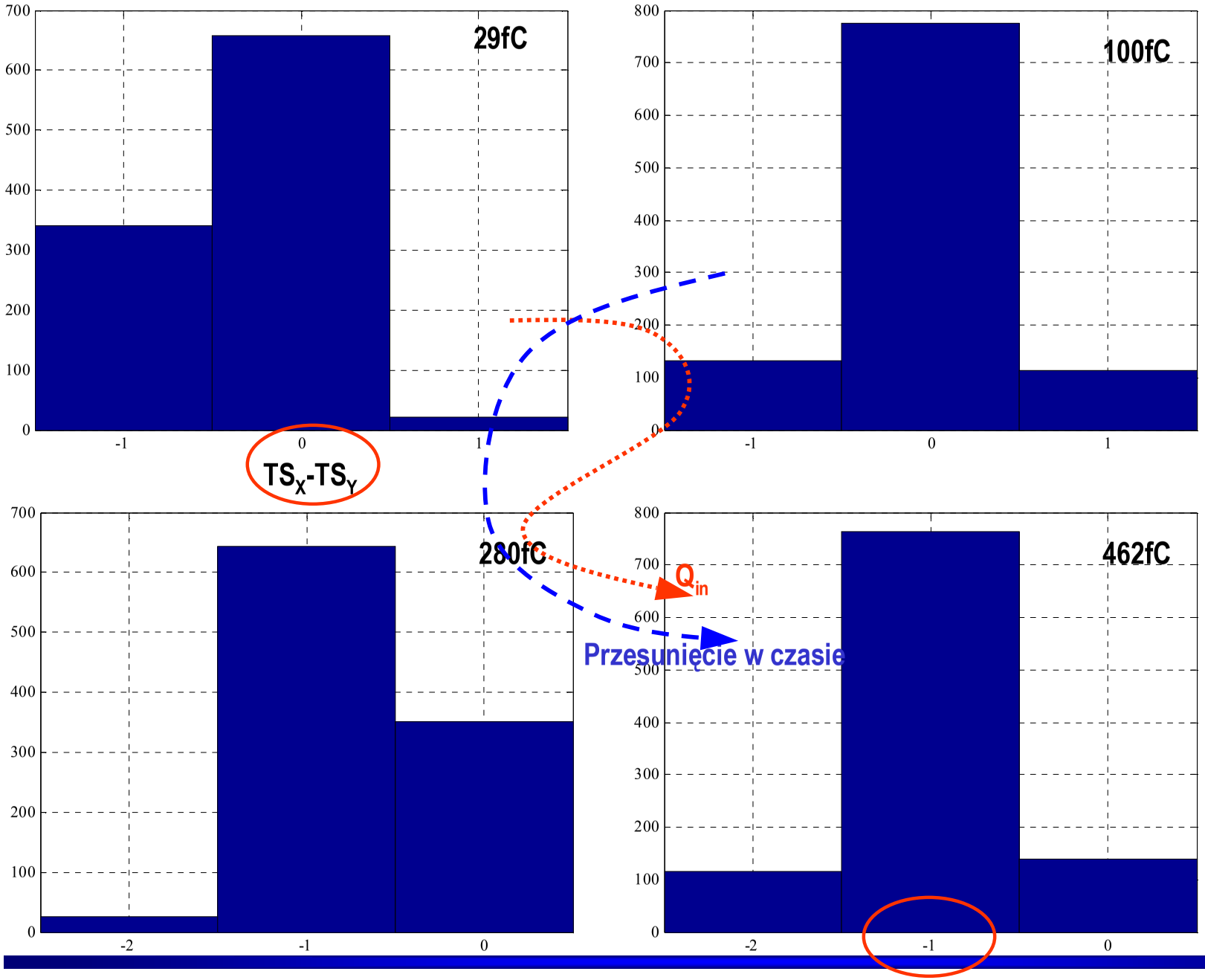




Kompensacja efektu wędrowania (time walk)



Kompensacja efektu wędrowania (time walk)



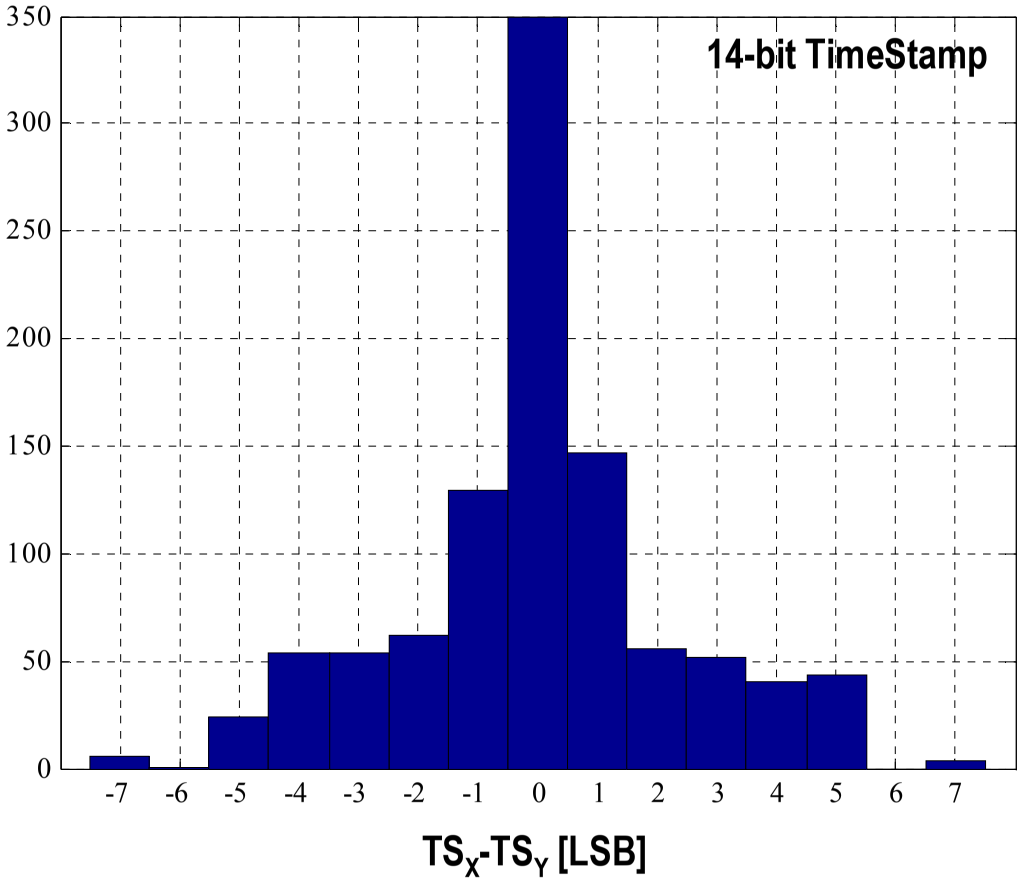
ical=10 (dyskryminacja)

Dla q_{in} od 33fC do 462fC

Time Walk ~4ns

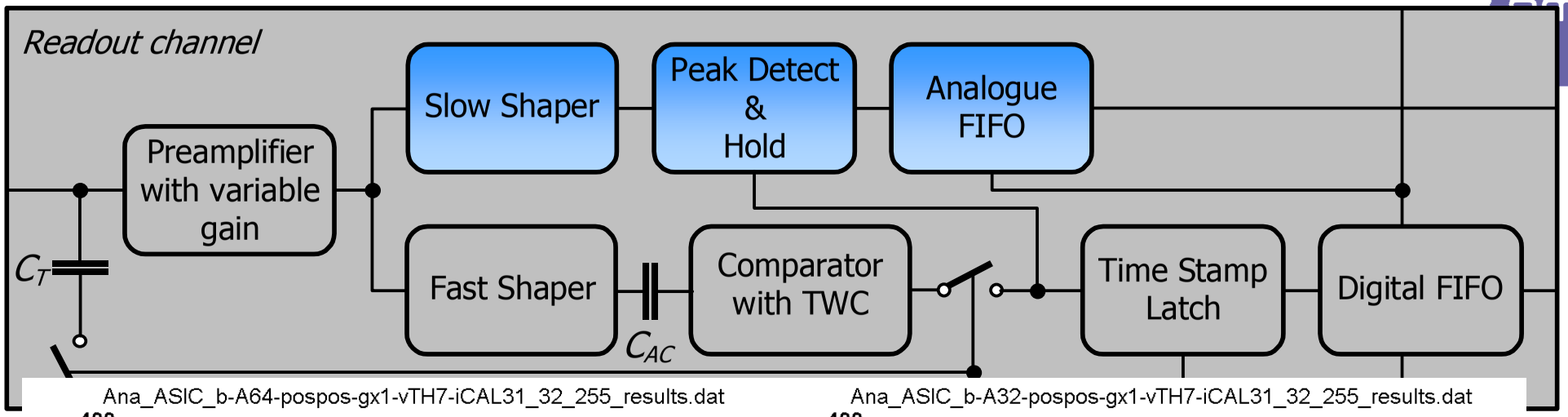
UWAGA: histogramy dla sygnatur 12-bit TS

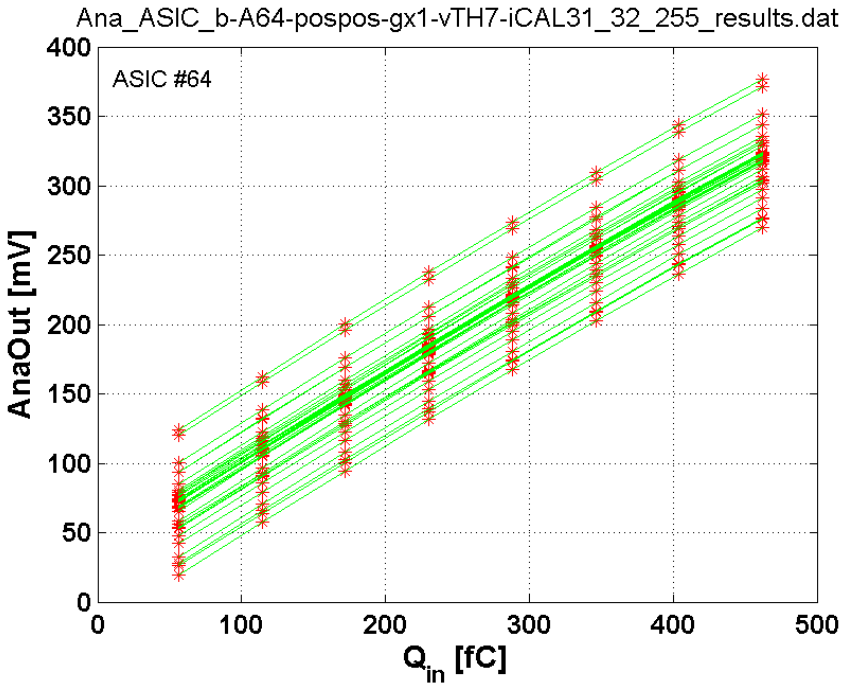
Efekt drżenia (jitter)

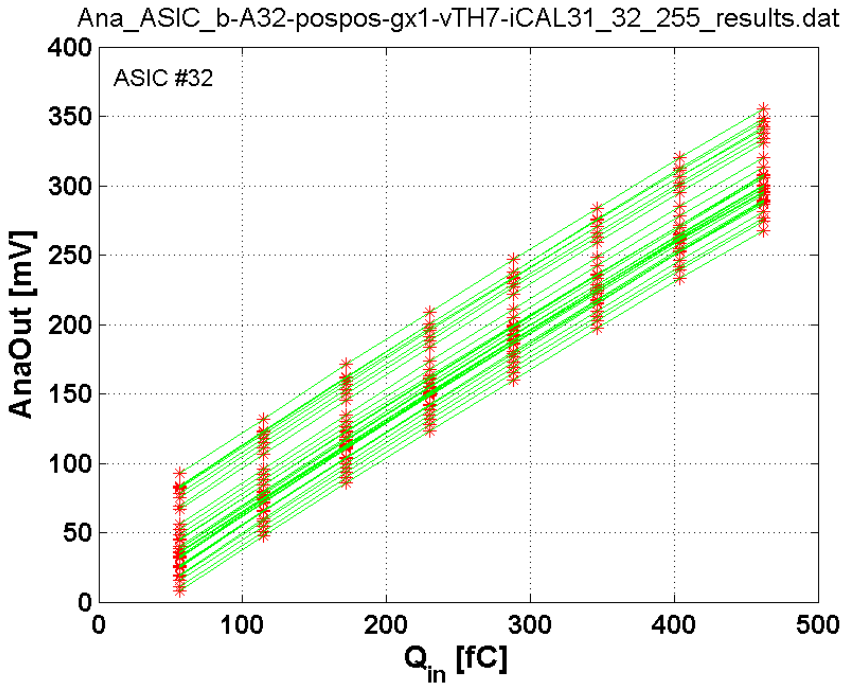


jitter ~1 [$LSB_{14\text{-}bit}$] (1ns)

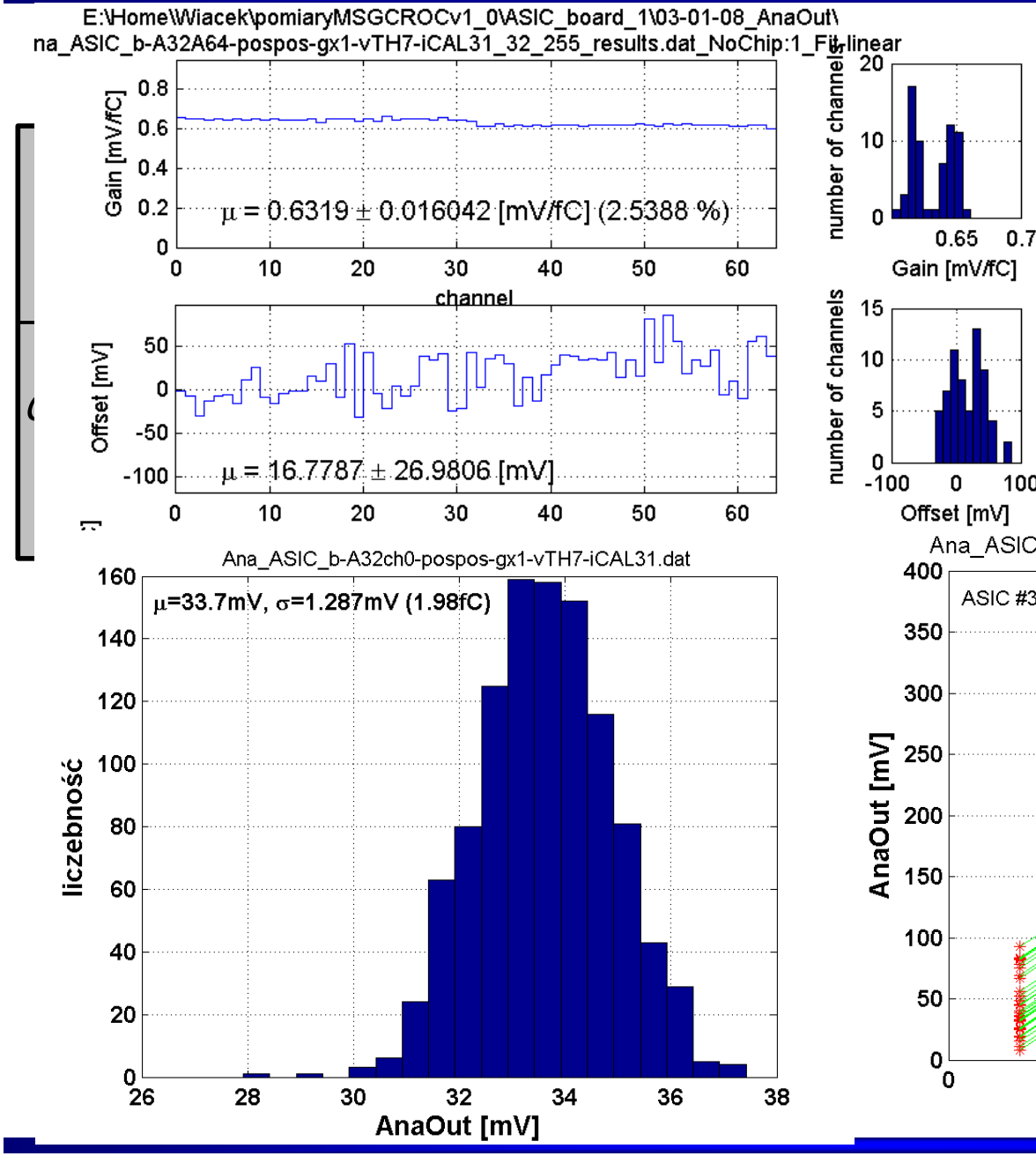
Kanał energetyczny (slow shaper)



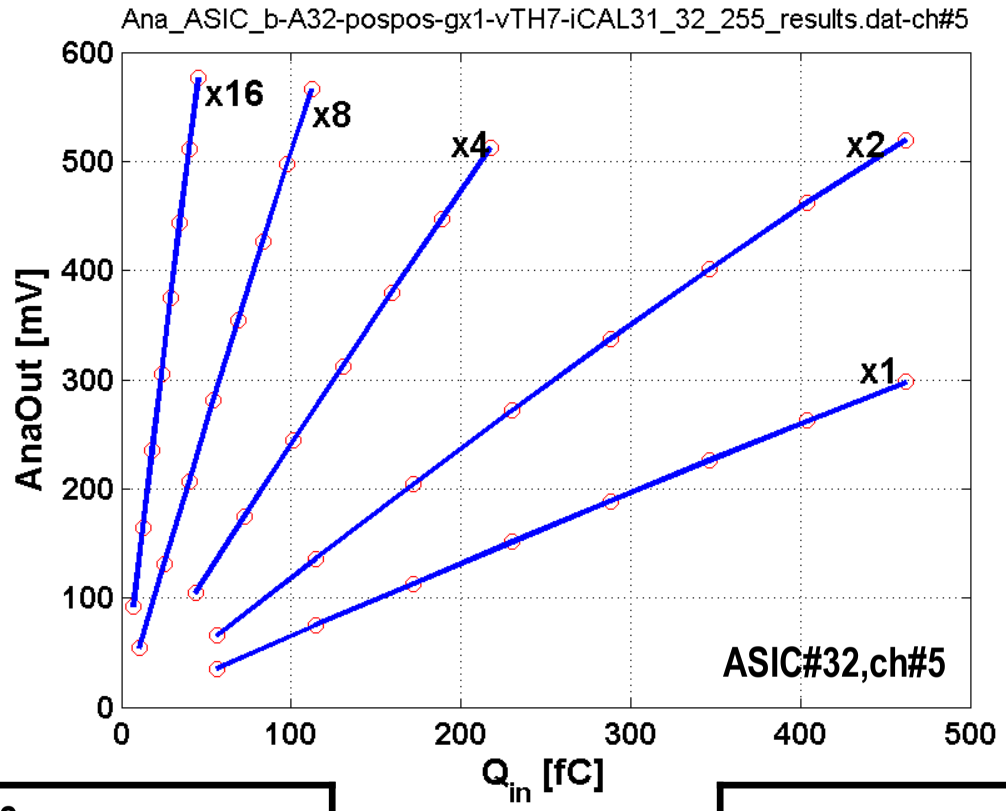




Kanał energetyczny (slow shaper)

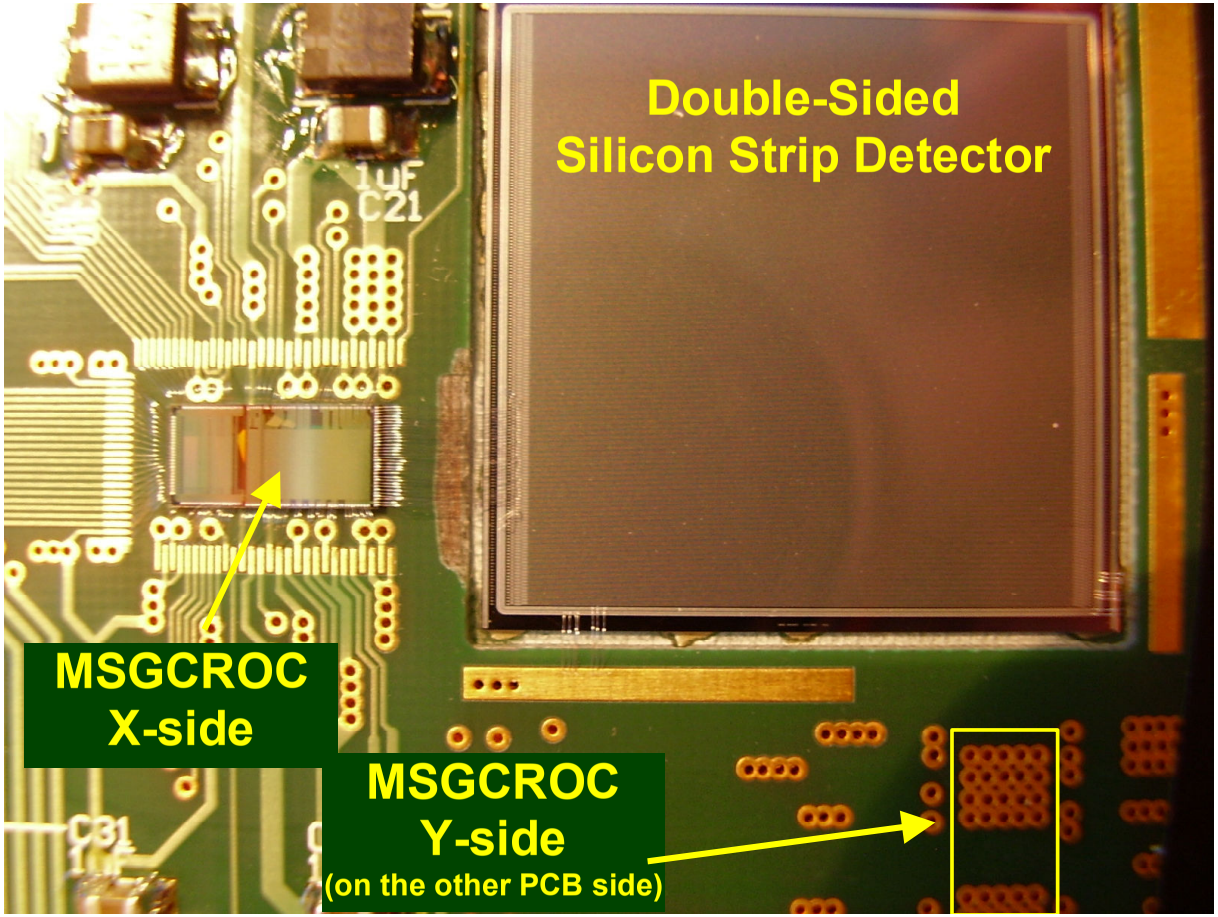


Kanał energetyczny (slow shaper)

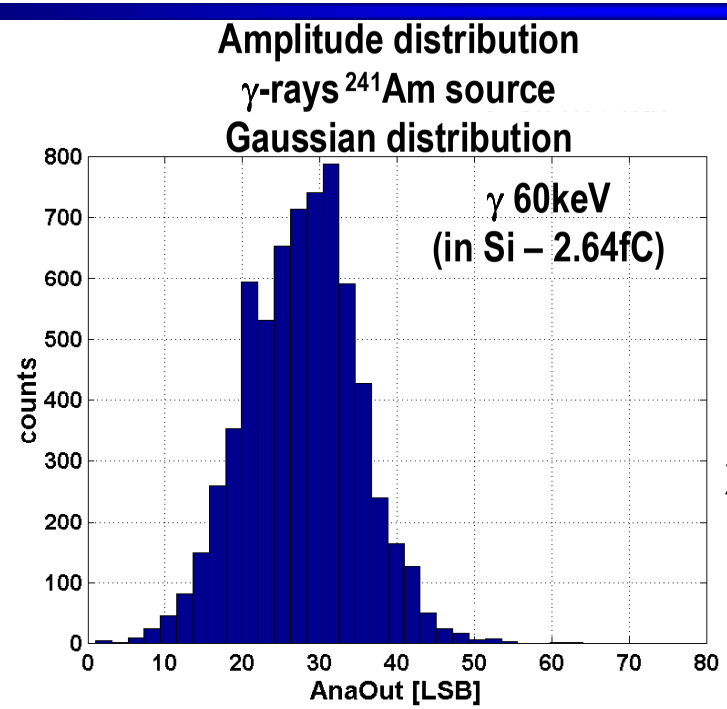


ASIC #32			ASIC #64	
Gain [mV/fC]	Offset [mV]		Gain [mV/fC]	Offset [mV]
0.6470±0.0056 (0.9%)	3.7 ±23.2	x1	0.6168±0.0048 (0.8%)	29.8 ±24.2
1.121 ±0.011	12.1±23.9	x1.7	1.0606 ±0.0099	39.8±25.2
2.341 ±0.020	7.7 ±23.5	x3.6	2.244 ±0.016	35.4 ±25.0
5.029 ±0.052	6.8 ±23.9	x7.8	4.835 ±0.044	35.9 ±25.3
12.68 ±0.15 (1.1%)	7.6 ±24.7	x19.7	12.28 ±0.11 (0.9%)	7.6 ±24.7

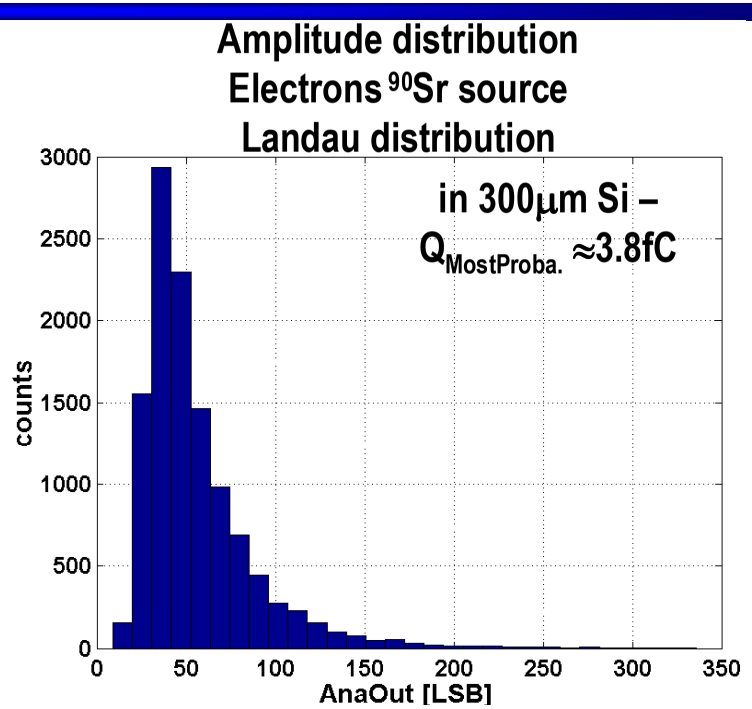
Pomiary ze źródłem promieniowania

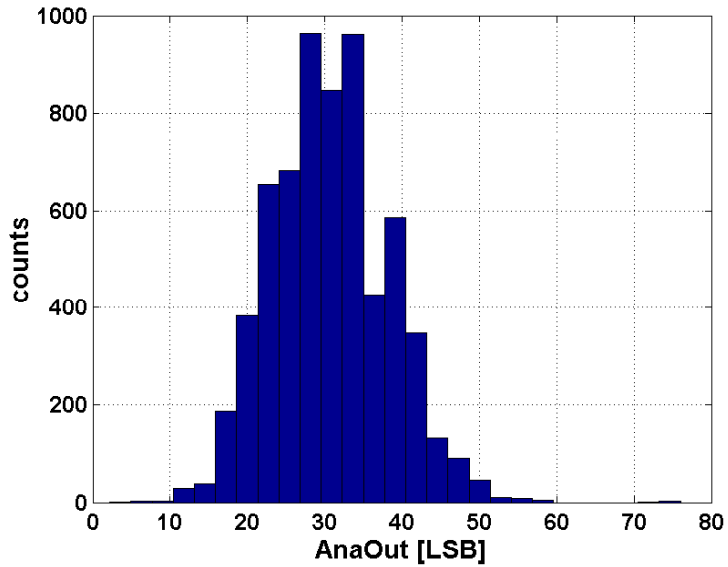


Pomiary ze źródłem promieniowania



X-strip





Y-strip