Power management in the ABCnext design

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Power distribution at LHC experiments

	ATLAS pixels	CMS pixels	ATLAS strips	CMS strips
Number of modules	1744	1440	4088	15148
Total number of channels	80 M	66 M	6.2 M	10 M
Total rack power incl. optical links and cable losses	30 kW	7 kW	45 kW	67 kW
ROIC name and technology	FE-I3 0.25 µm CMOS	PSI46 0.25 µm CMOS	ABCD 0.8 µm bi-CMOS	APV25 0.25 µm CMOS
ROIC analog (digital) voltage	1.6 V (2.0 V)	1.5 V (2.5 V)	3.5 V (4 V)	1.25/2.5 V (2.5 V)
ROIC power consumption/channel	84 µW	40 µW	3.6 mW	2.9 mW
Total ROIC current	3.8 kA	1.5 kA	6 kA	15 kA
Cable length (one way)/resistance (round trip)	~110 m	~50 m	~110 m/4.5 Ω	34-62 m
Power efficiency	~20%	~42%	~50%	52%
Power distribution schemes	IP[4]	PP[5]	IP	PP
Local regulators (near/on-detector)	Yes	Yes	No	Yes

Why independent powering fails at SLHC?

SLHC = 10x more channels in inner tracking detectors

1. Don't get 5 or 10 times more cables in
2. Power efficiency is too low (50% ATLAS SCT ⇔ ~15% SLHC)
3. Cable material budget: 0.2% of R.L. per layer (barrel normal incidence) ⇔ 1% or 2% SLHC
4. Packaging constraints

Each reason by itself is probably sufficient for a No-No

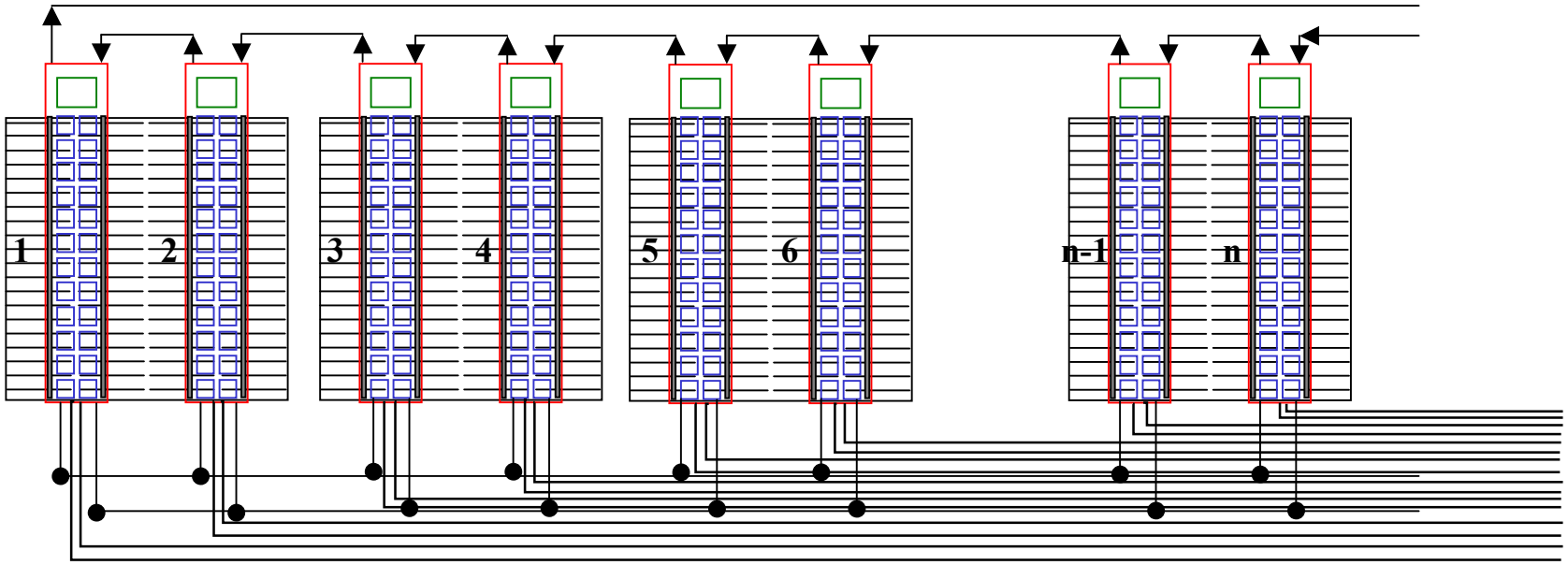
Why powering R&D?

Cannot afford cable pollution anymore and don't need to.
New systems will be much better
(cable number, material performance; packaging; power efficiency, cost)

Serial powering

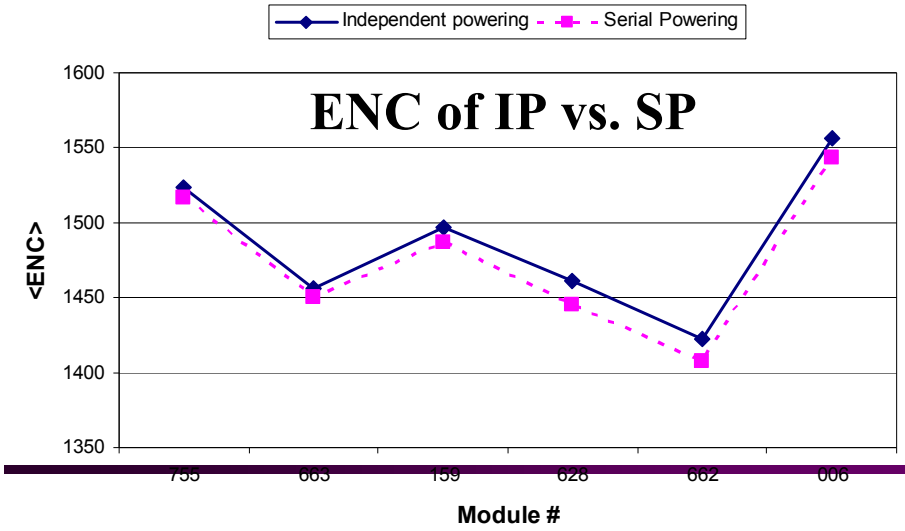
SP: n=20; $I_H = I_{PS} = 2.4$ A; $V_{PS} = nV_{ROIC} = 50$ V

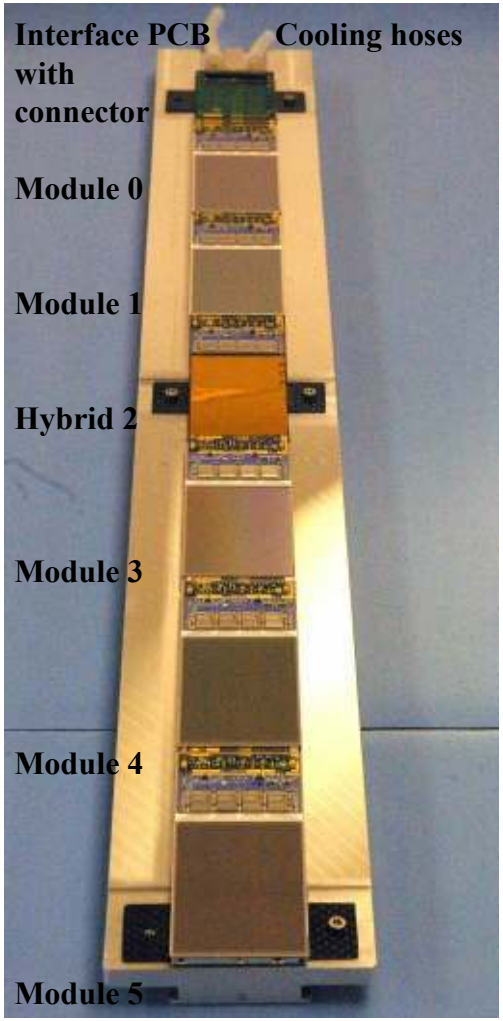
Features: saves factor ~8 in power cables/length over ATLAS SCT



Serial powering – proof of principle

ATLAS SCT module tests





6-module serial powering stave

ABCN

Prototype chip for Si strip readout in Upgrade Inner Tracker

Binary readout

Front-end optimised for short strips

Positive or negative input charge

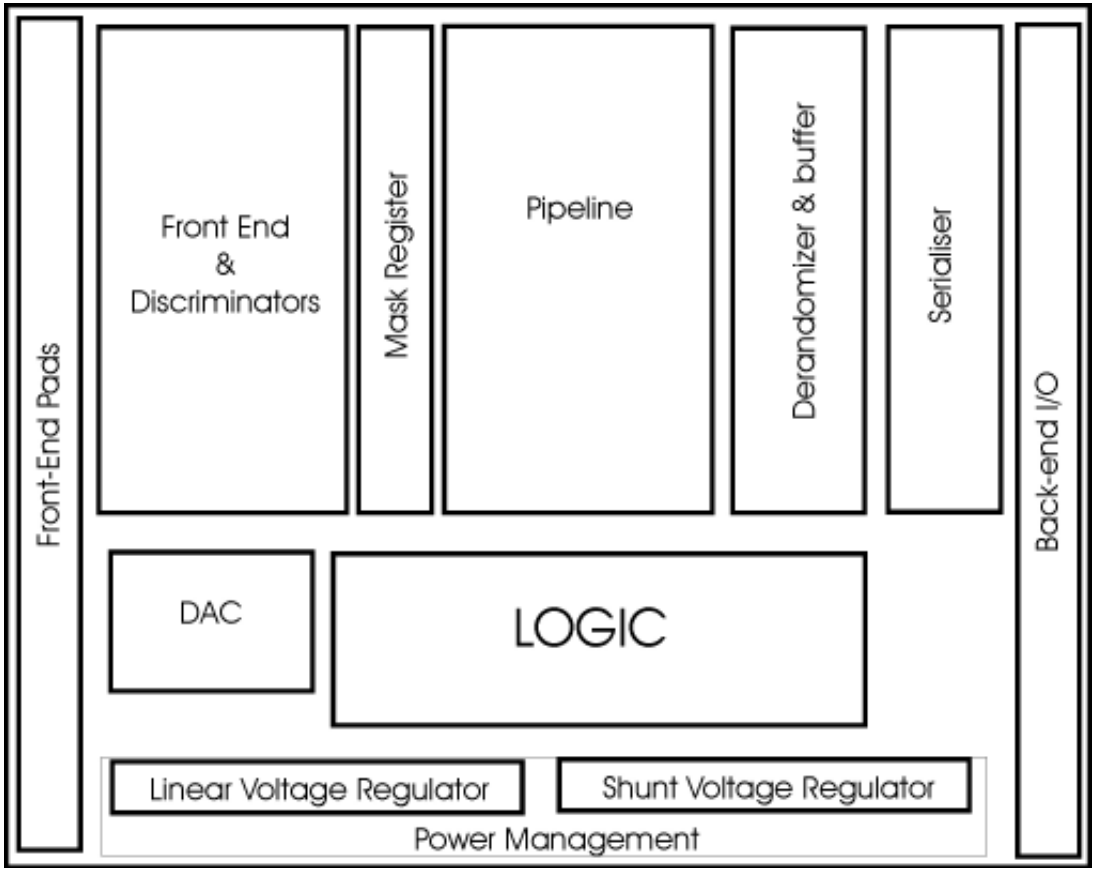
Readout clock up to 160 Mbits/sec

250 nm CMOS (IBM) technology

2.5 V digital power supply (100 mA)

2.2 V analogue power supply (30 mA)

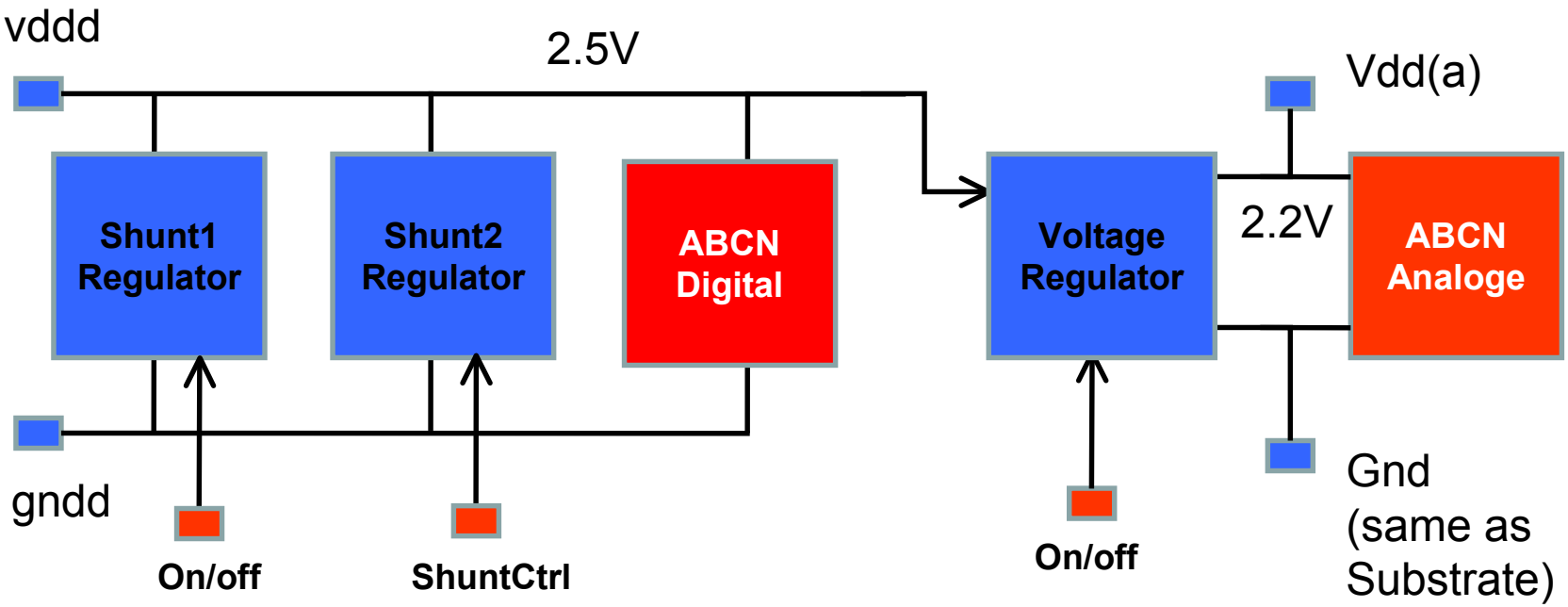
Compatible with serial powering scheme



On chip power management and distribution

Two optional shunt regulators

Serial voltage regulator (optional)



System issues

In the serial powering scheme the shunt regulators in the ABCNs (up to 20) on the module get connected in parallel

Two schemes are implemented in the ABCN prototype

1. **Full shunt regulator in each ABCN chip**
2. **Shunt transistor in each ABCN and regulation circuitry external common for all chips on the moule**

Distributed shunt regulator

Power dissipated in the shunt regulators is distributed uniformly across the hybrid,

No very high current devices required.

Single point of failure reduces compared to one regulator per hybrid.

Hybrid design fully scaleable with respect to power distribution.

Sensitivity to matching.

Powering-up modules

Nominal powering-up scenario

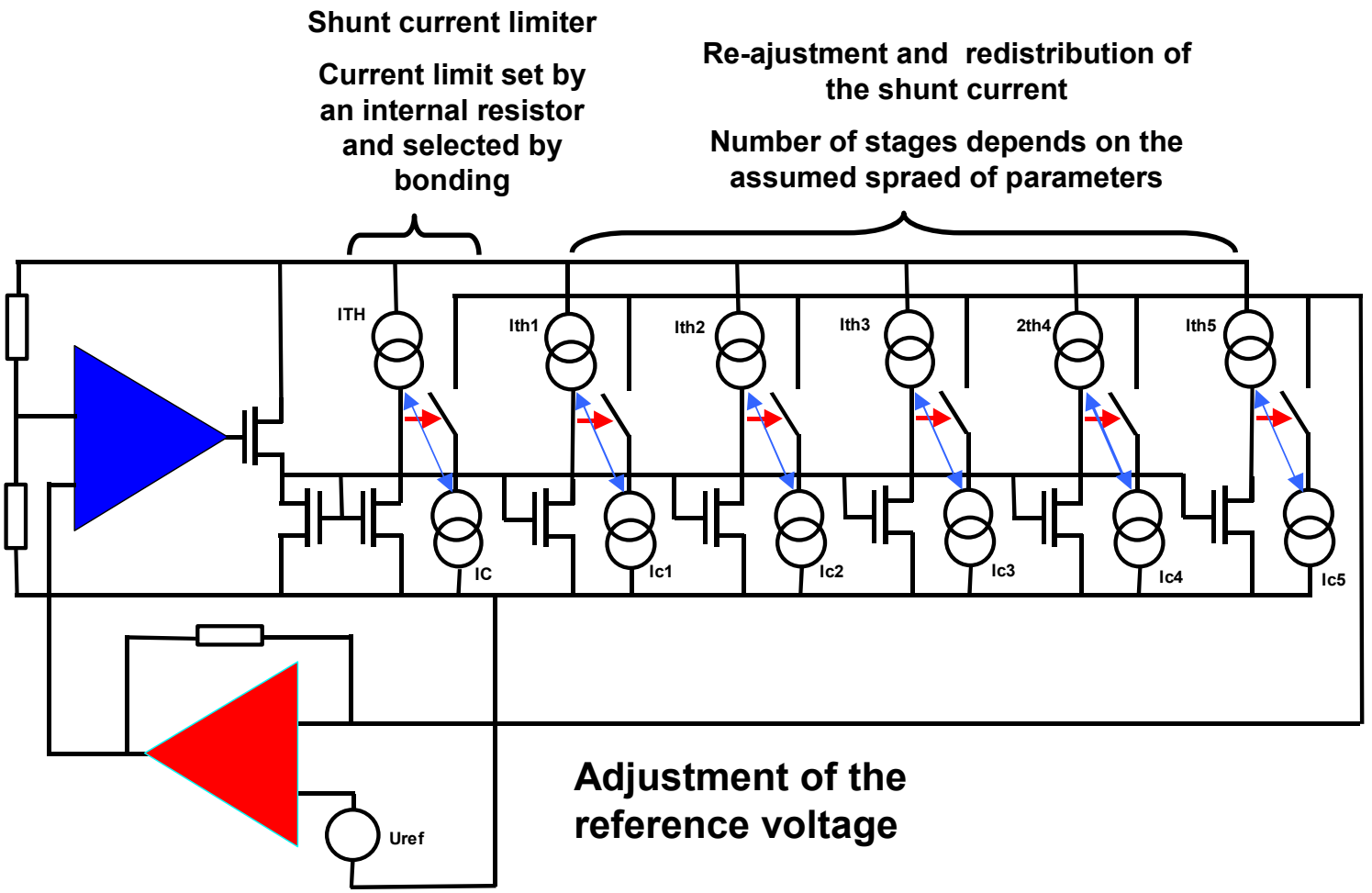
Supply current ramped up to the nominal required value with clock signal active in the digital part – digital switching current increase smoothly following the I-V characteristic of the digital load.

Critical scenarios

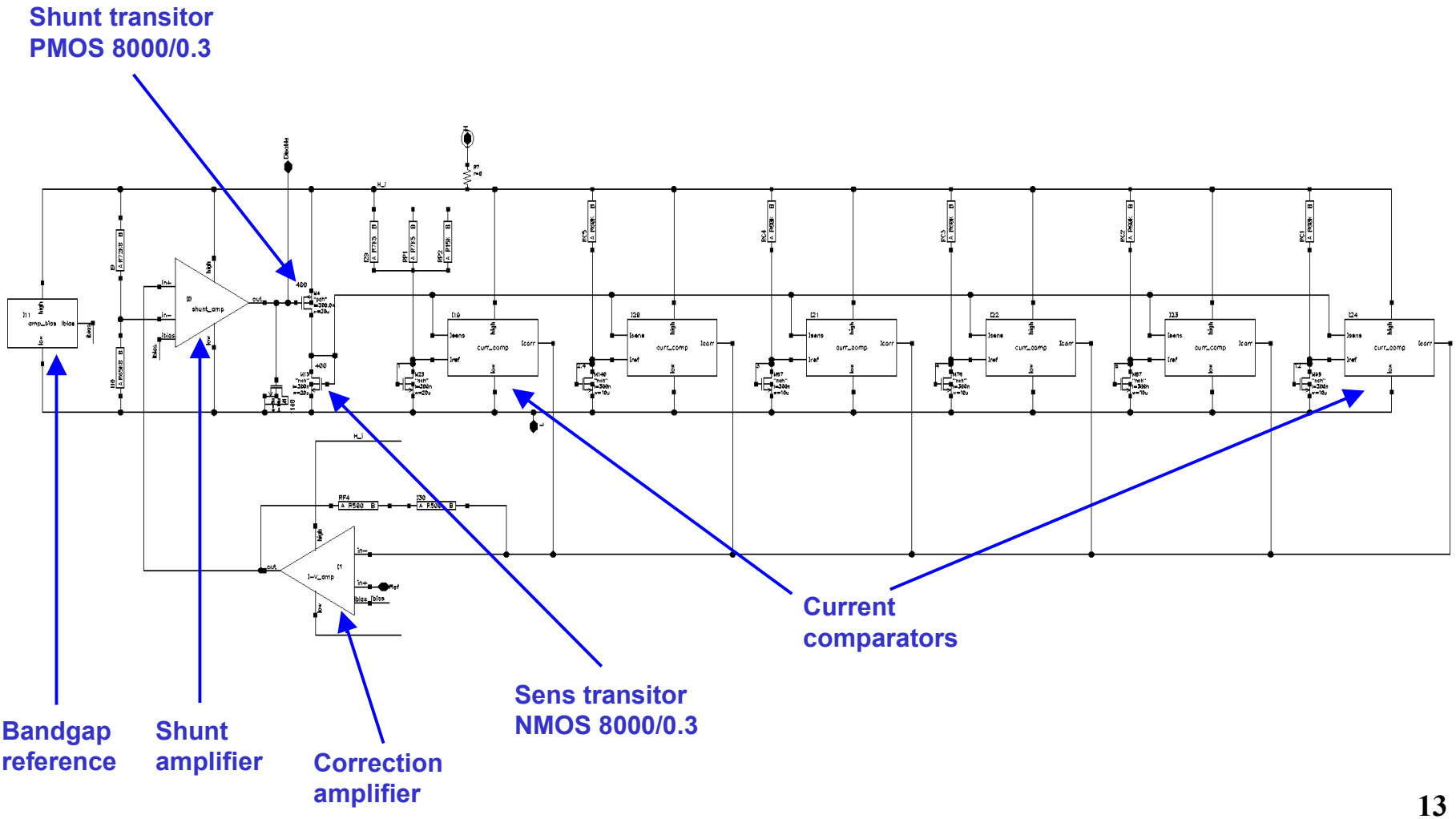
Clock signal is delayed with respect the power start-up – supply current forced by external current supply may temporarily go much above the ABCN current consumption.

Clock signal lost suddenly during normal operation – digital current consumption suddenly reduced.

Full shunt regulator on chip - design concept

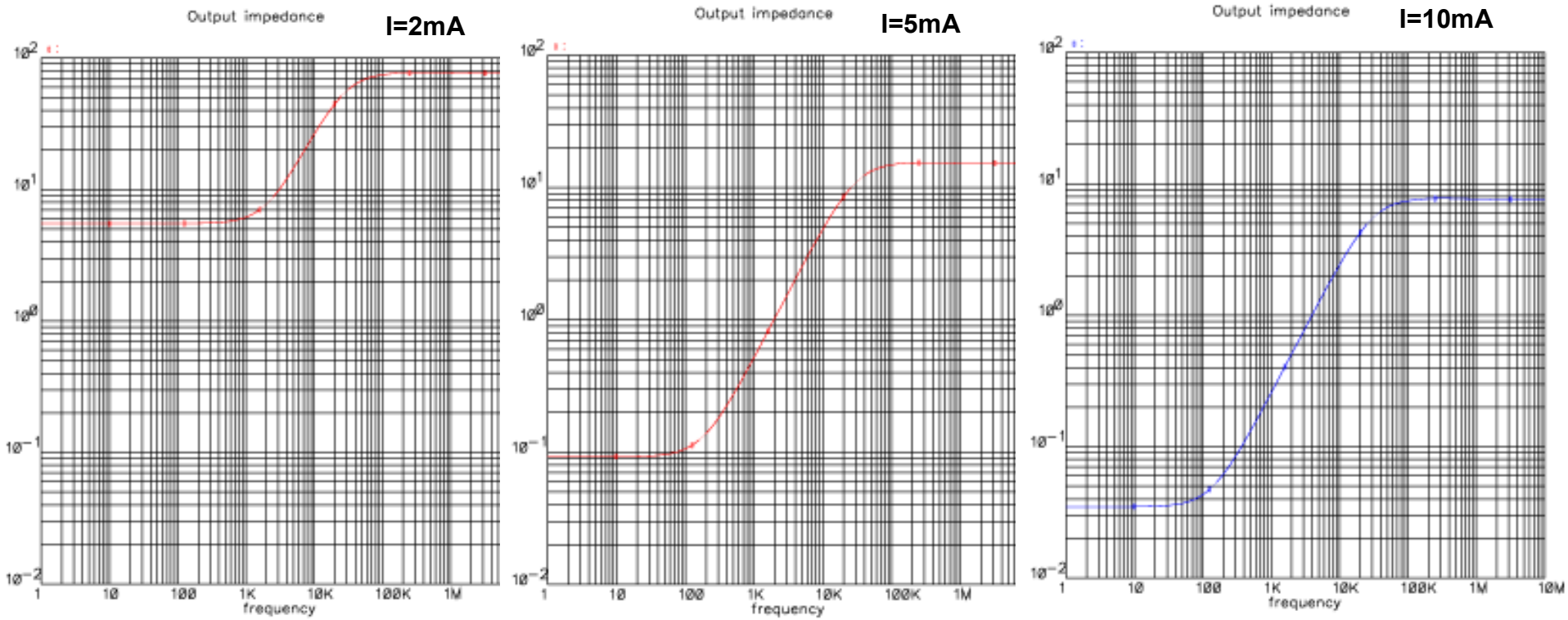


Implementation



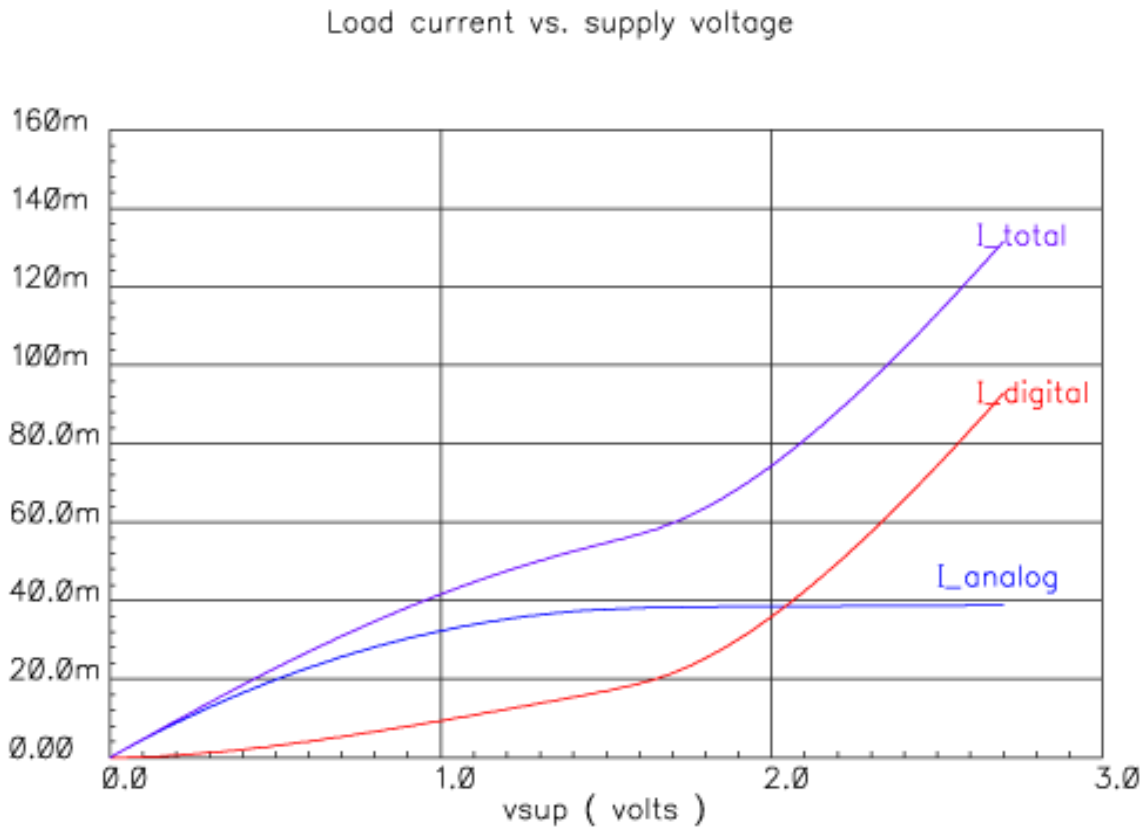
Ouput impedance - single shunt regulator

Shunt curent of 5 to 10 mA will be required



For a hybrid with 20 ABCNs the effective output impedance will be about 20 times smaller

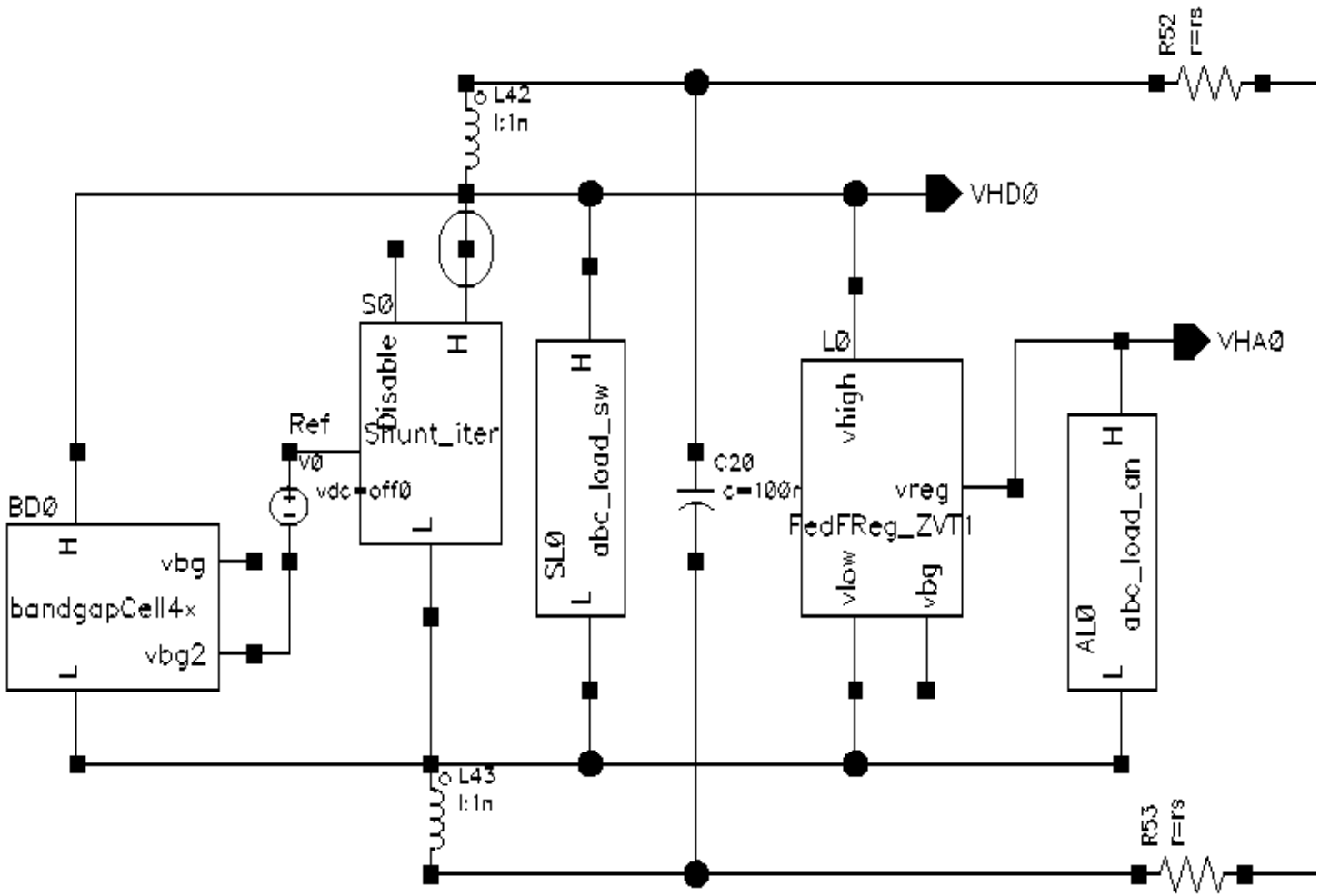
Model of ABCN load



I-V curve for digital current derived from simulation of switching digital circuitry

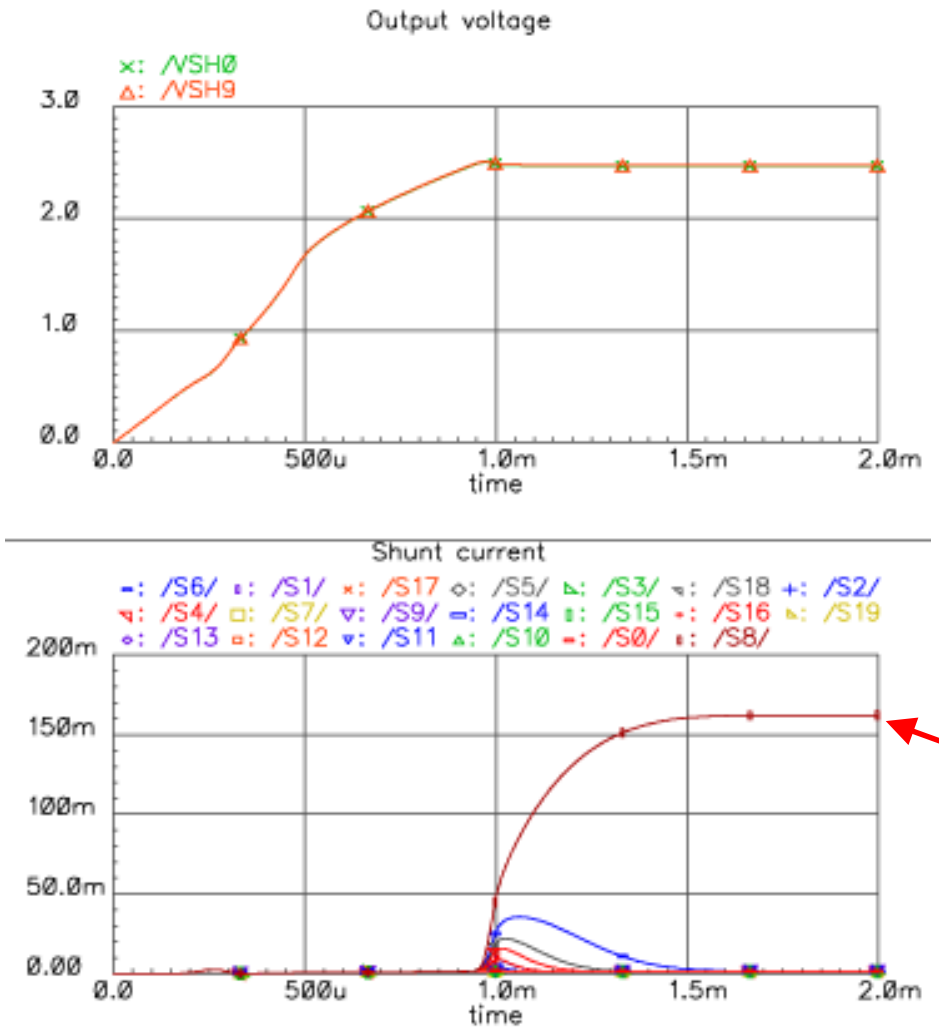
I-V curve for analog current derived from front-end simulation.

ABCN model


R52
r=rs
L42
l:1n
VHD0
S0
Disable
H
Shunt_iter
L
Ref
V0
vdc
off0
BD0
H
vbg
bandgapCell4x
vbg2
L
SL0
abc_load_sw
H
L
C20
c=100n
L0
vhigh
vreg
FedFReg_ZVT1
vlow
vbg
VHA0
AL0
abc_load_an
H
L
L43
l:1n
R53
r=rs

Matching problem

Clock is ON all the time



20 ABCNs with internal shunt regulators connected in parallel

All mismatch effects represented by mismatch of reference voltages

Flat distribution in a range –10 mV to +10 mV assumed

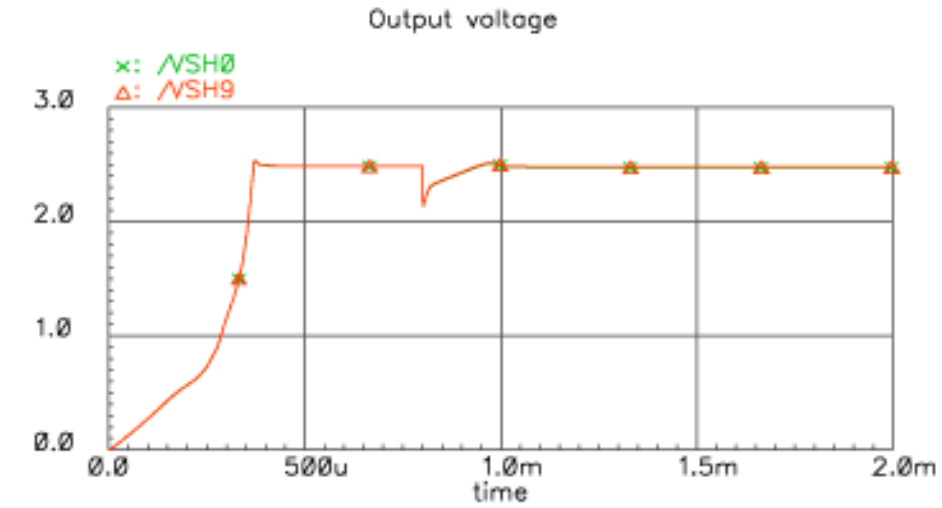
Average shunt current of 8 mA per device

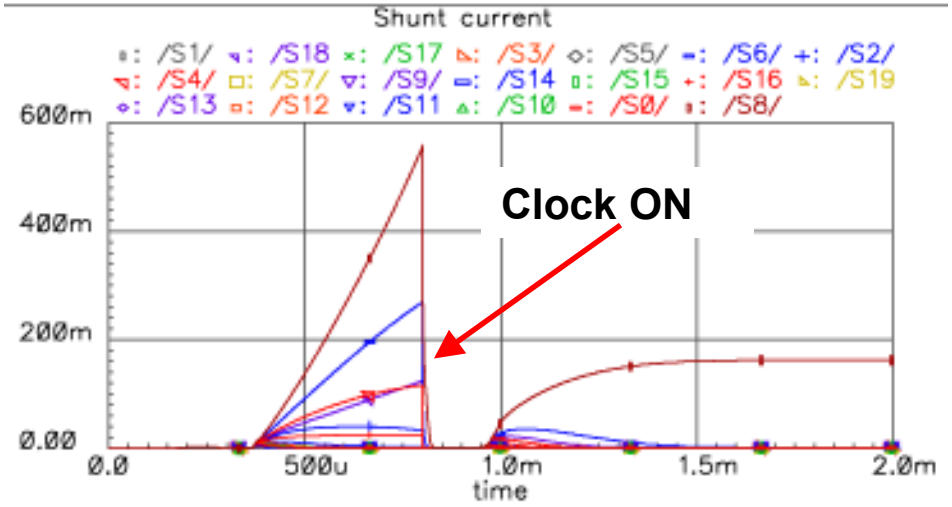
One shunt device always wins

This would happen even if we assumed perfect matching because of the voltage drops along the power busses on the hybrid

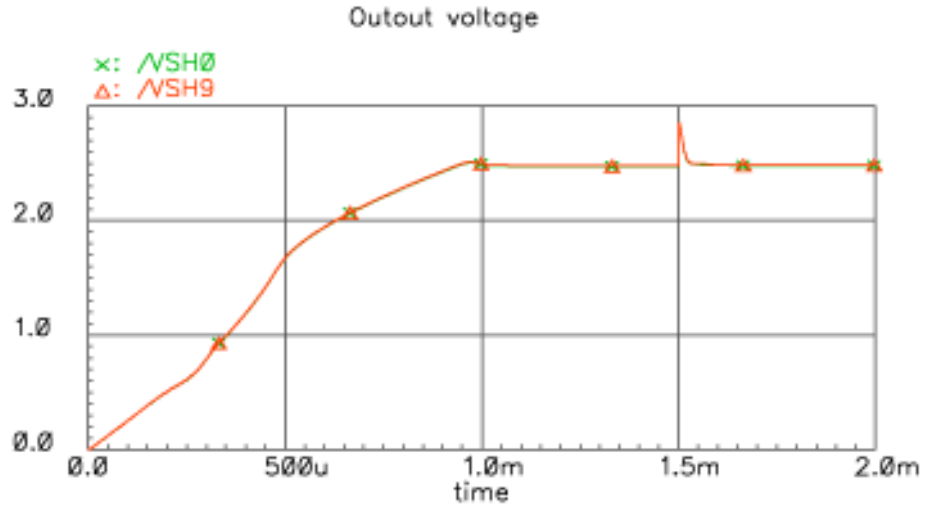
Matching problem

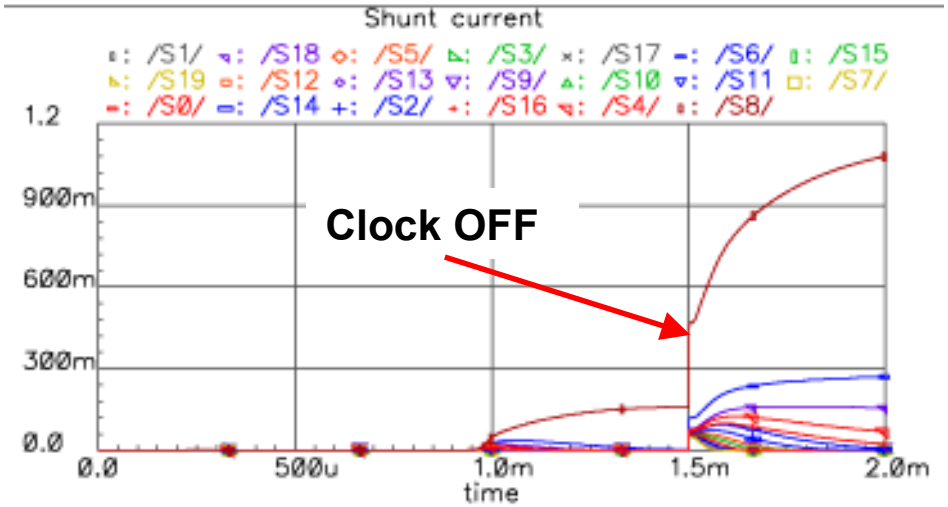
Clock delayed





Clock OFF during operation

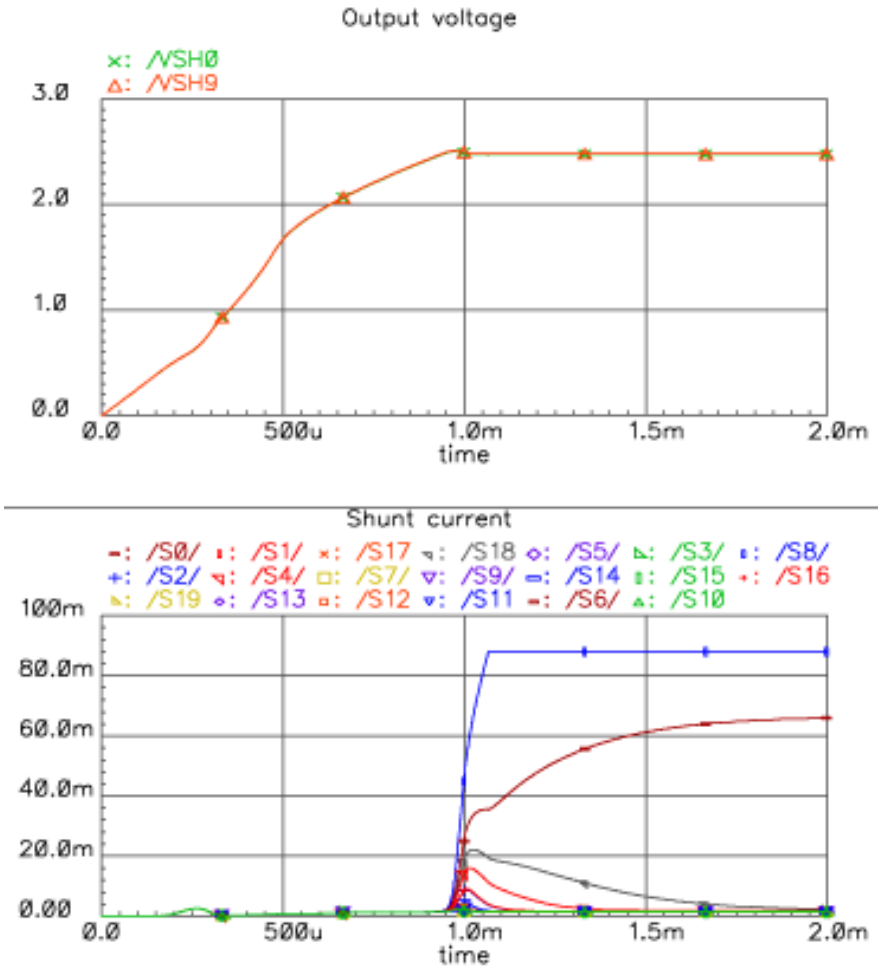




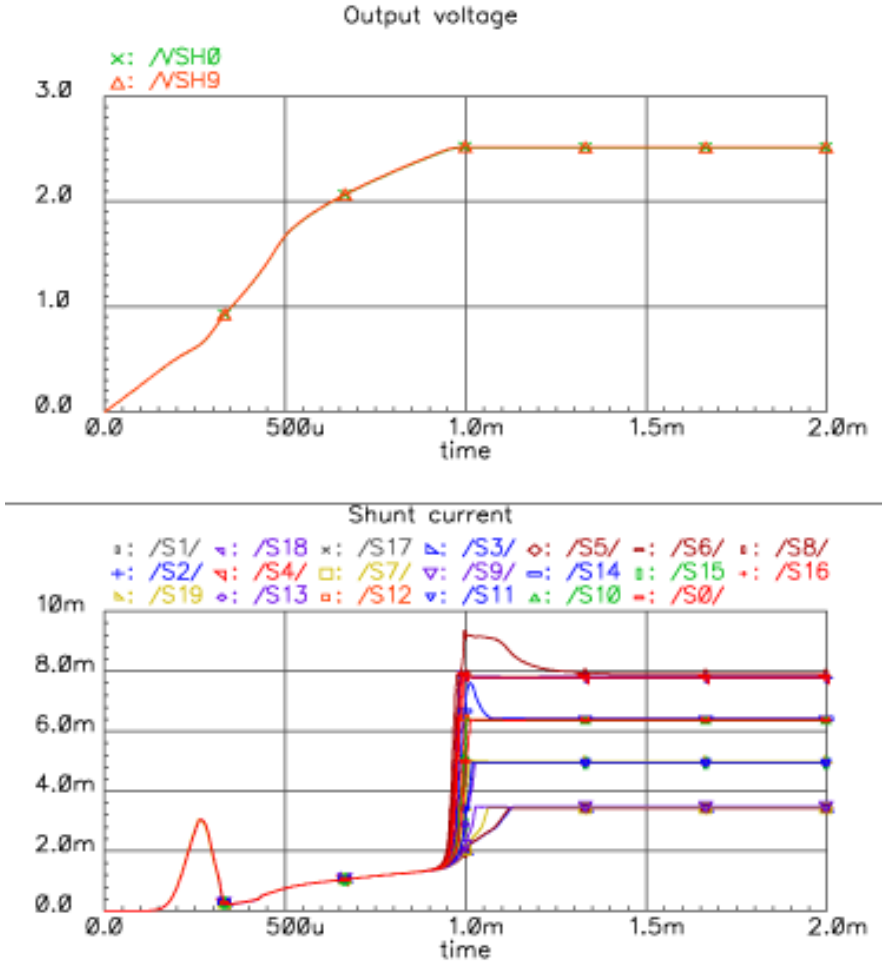
Performance of the auxiliary circuits

Clock is ON all the time

Only current limiter active

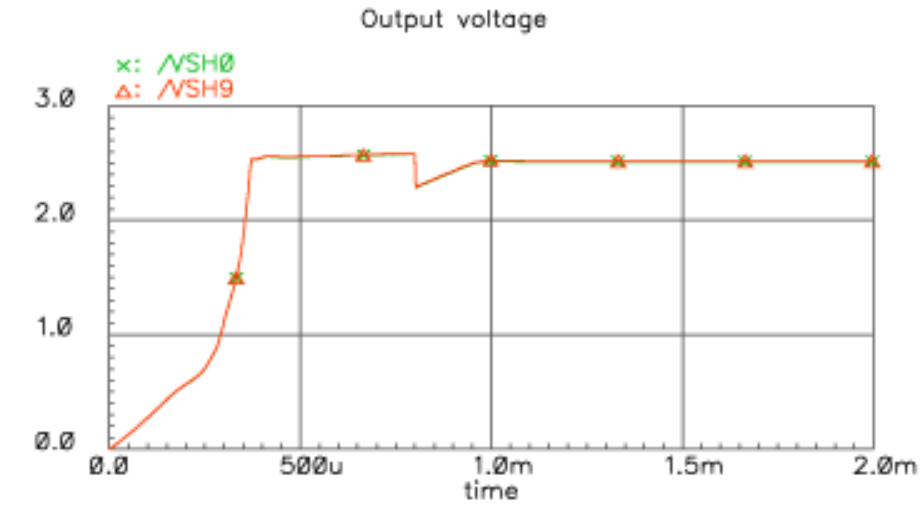


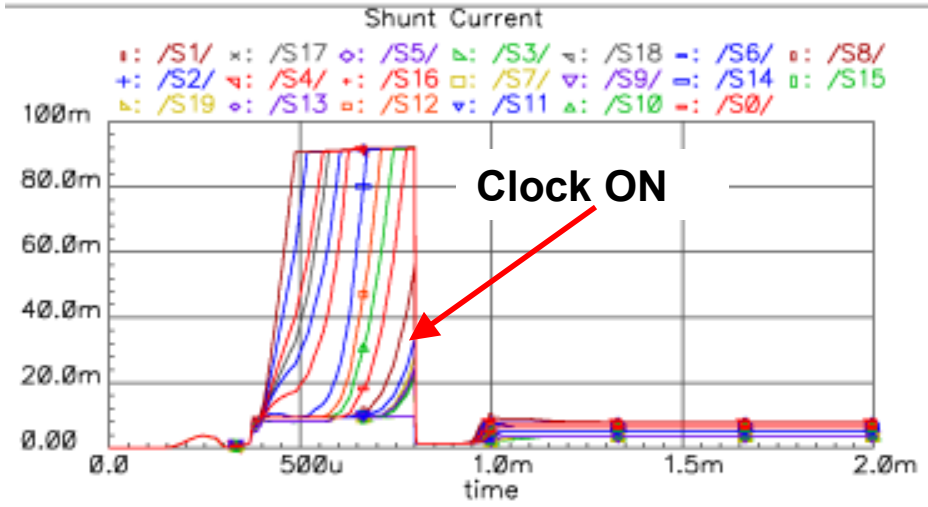
All circuitry active



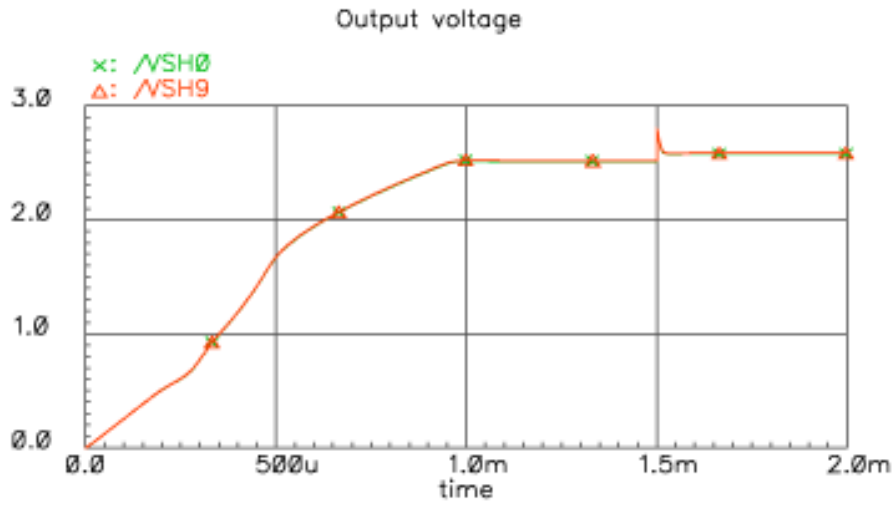
Performance of the auxiliary circuits

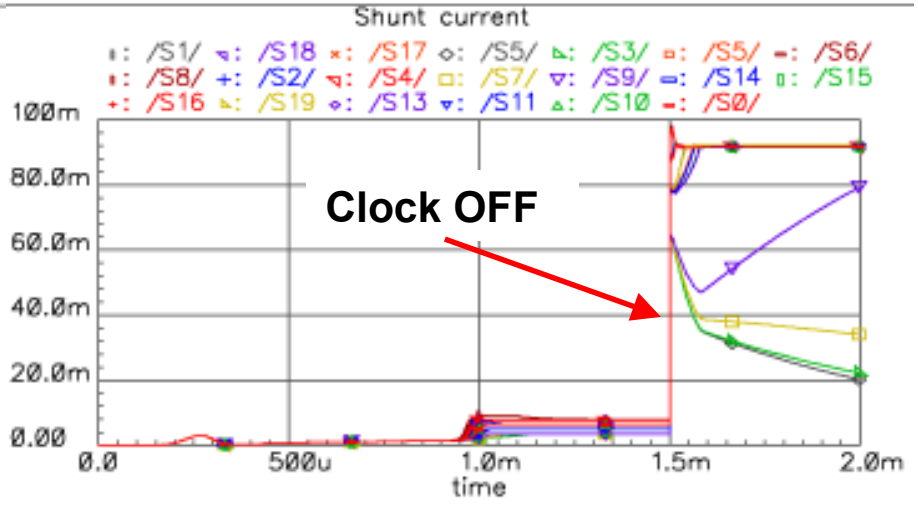
Clock delayed





Clock OFF during operation



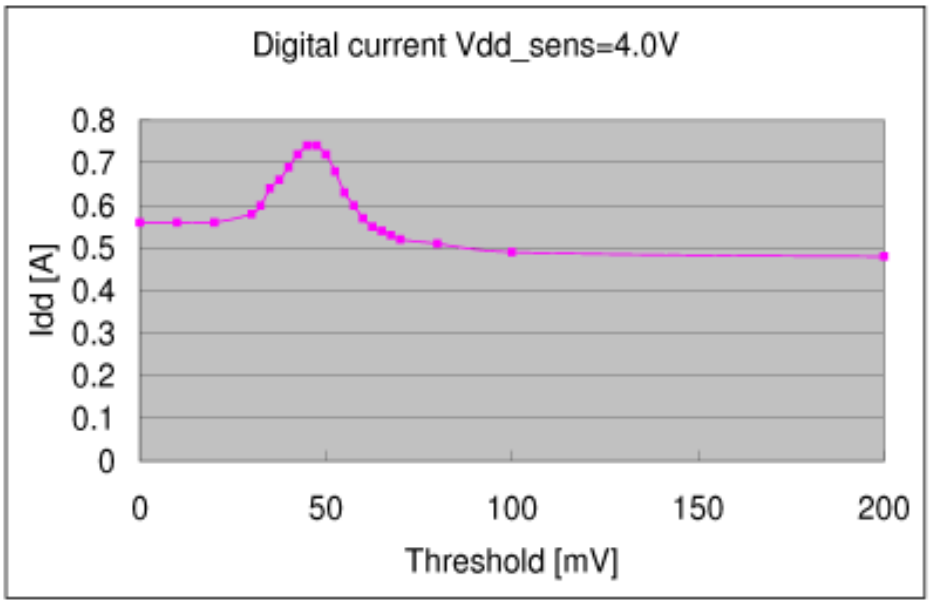


Expected fluctuations of digital current

... based on ABCD data

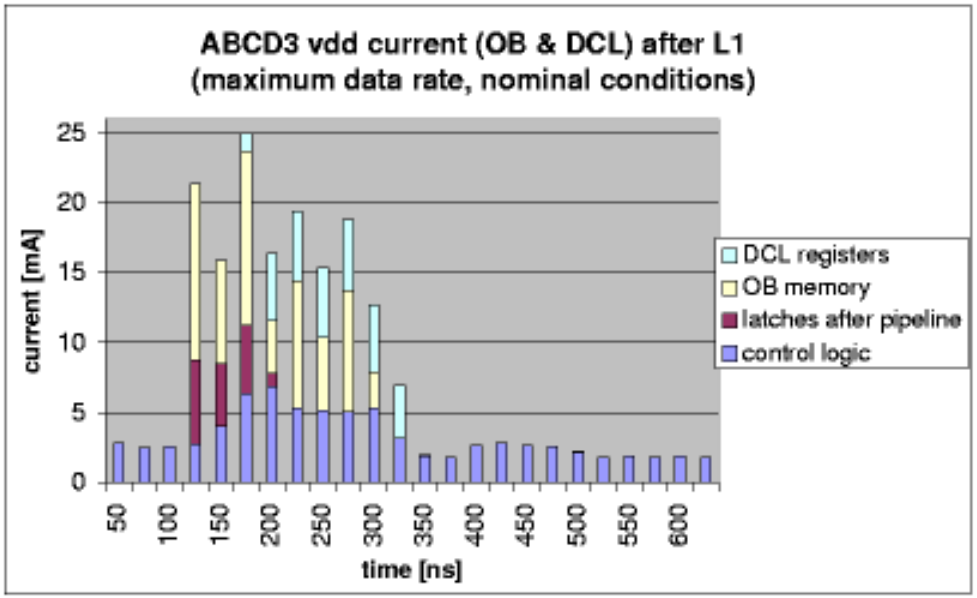
SLOW

digital current vs threshold (count rate)



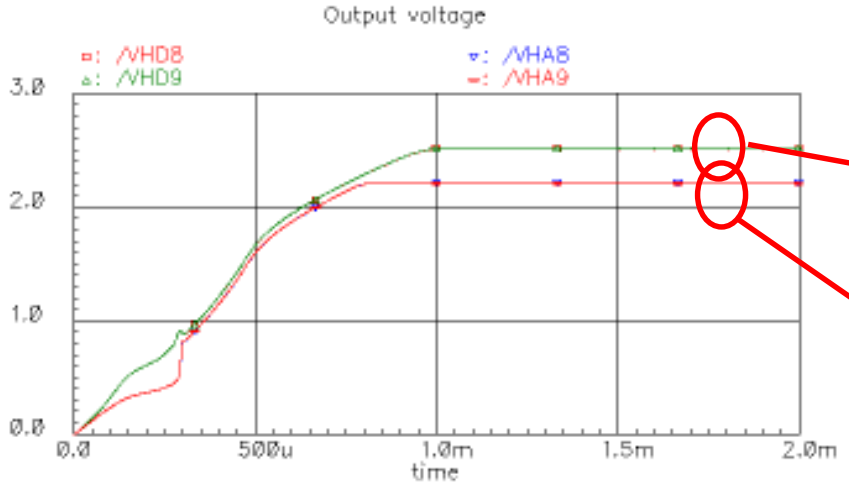
FAST

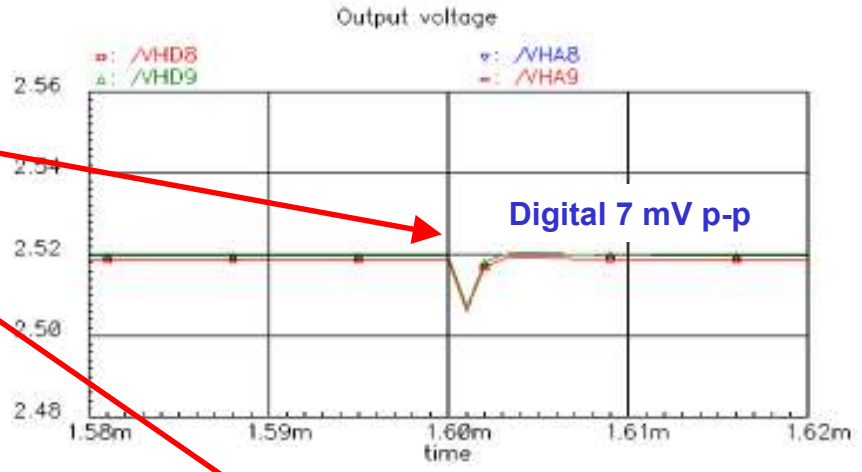
digital current spikes due to increased digital activity after receiving a trigger signal

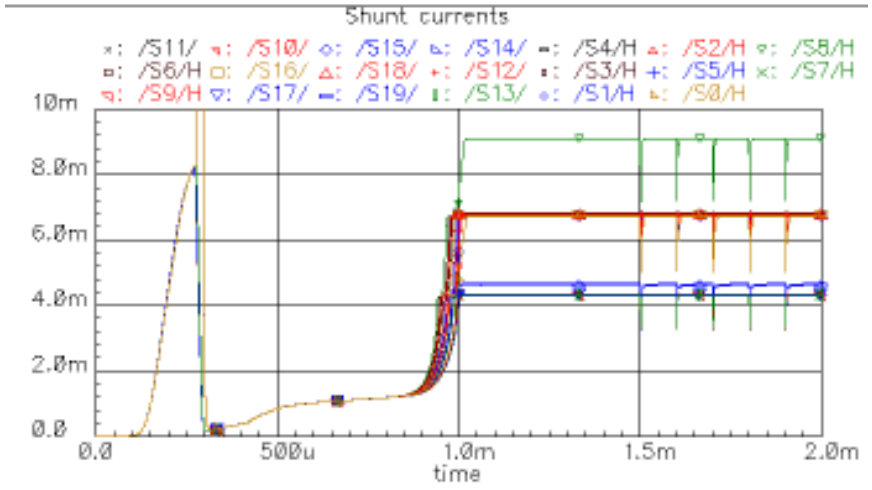


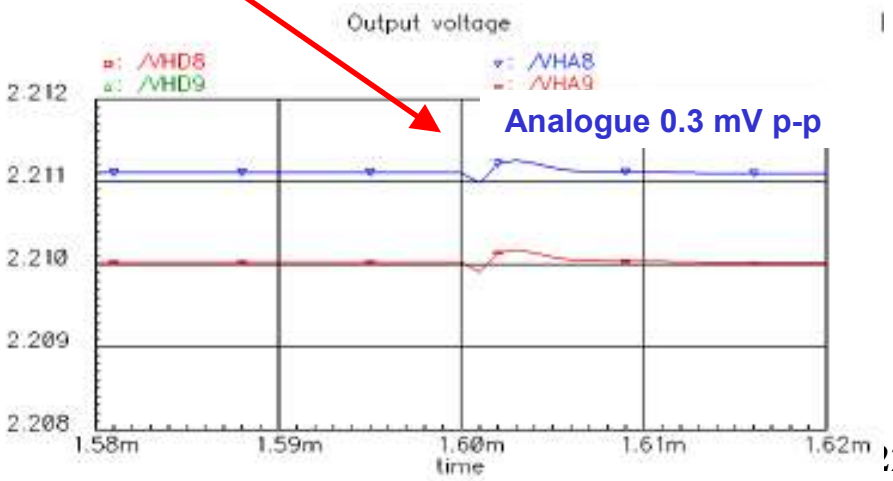
Filtering performance

Response to digital current spikes: 20 mA over 200 ns
(such spikes are observed in the ABCDs after receiving a trigger)



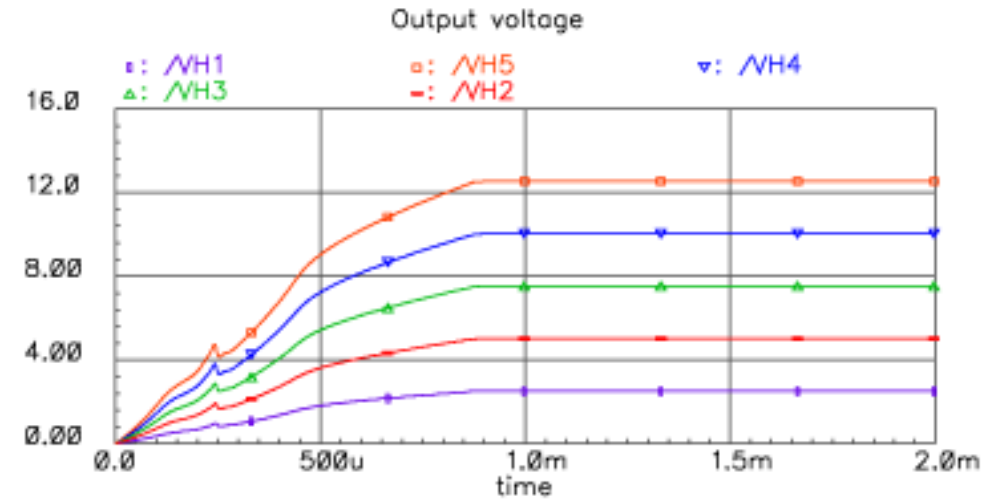


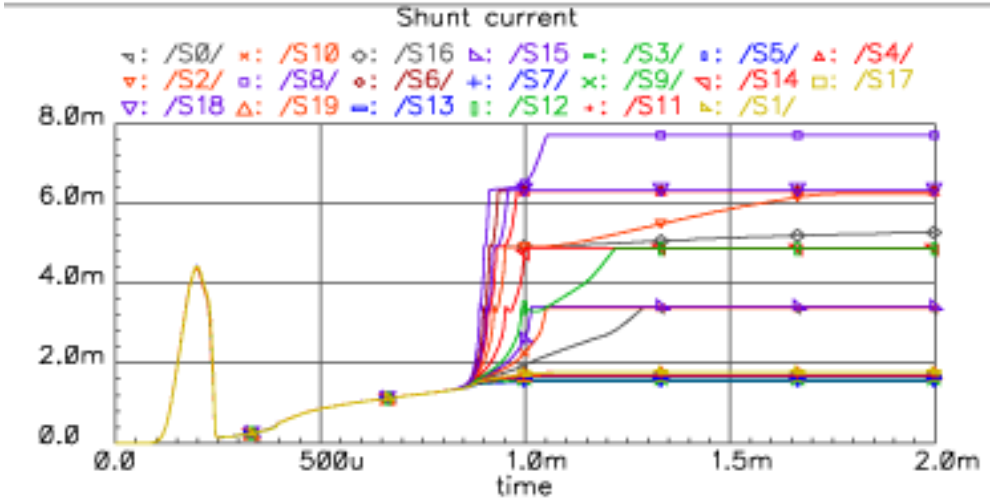




Current setting and control

5 modules (20 ABCNs each) in series





How do we set and control the supply current?

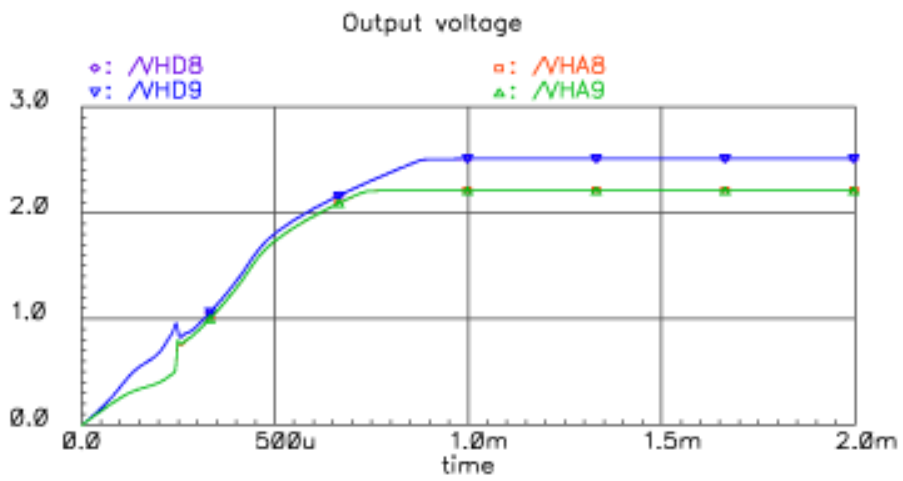
The digital current may vary substantially with occupancy (noise scan) and process variation

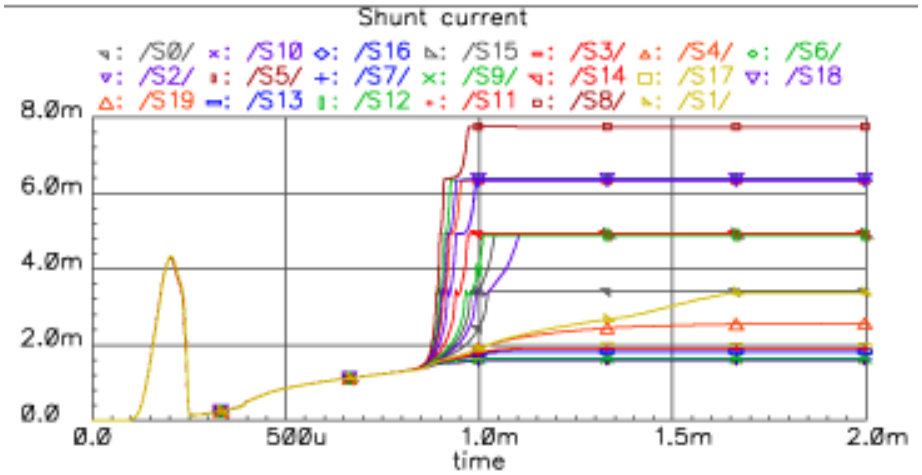
An ”ideal” solution: the supply current of a super module is controlled based on the voltage sensing and voltage regulation at the super module input only, e.g. for 5 modules: 5×2.5V

Implications for the overll powering system needs to be understood better

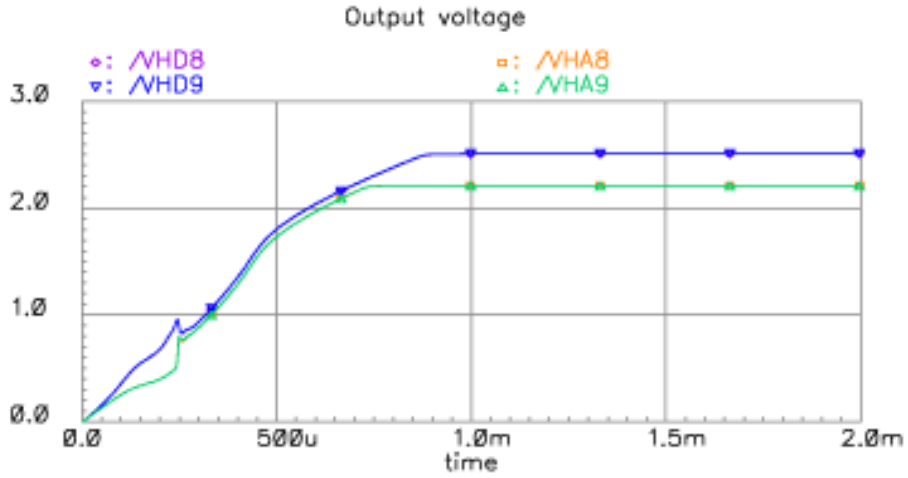
Sensitivity to shunt parameters matching (example)

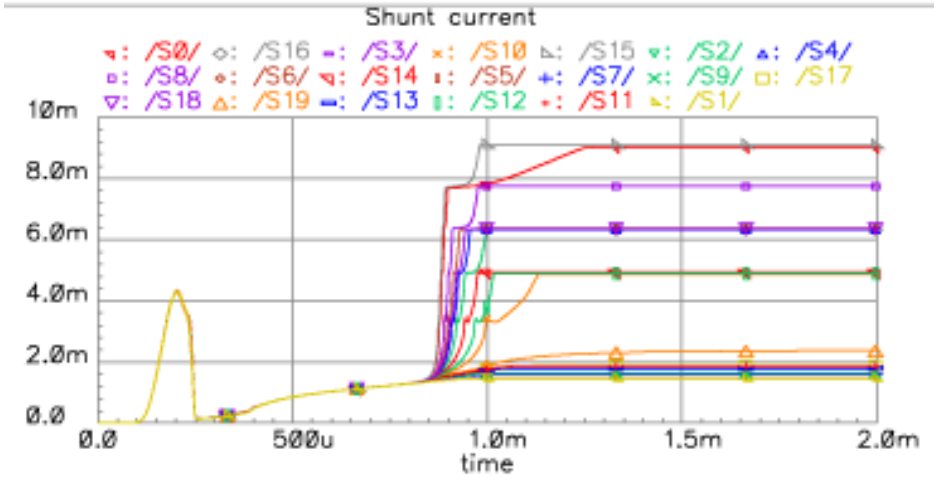
Flat distribution of the reference voltage –10 mA to +10mV





Two reference voltages offset by –20 mA and +20mV





Conclusions

The power management schemes implemented in the ABCN design will allow prototyping and testing modules with serial powering scheme.

Robustness of the proposed shunt designs w.r.t. production spread of parameters as well different ABCN operation modes needs to be proved using full size staves in realistic conditions.

Requirements for an external power supply system should be defined.