Development of general purpose low–power small–area 10 bit CMOS DAC

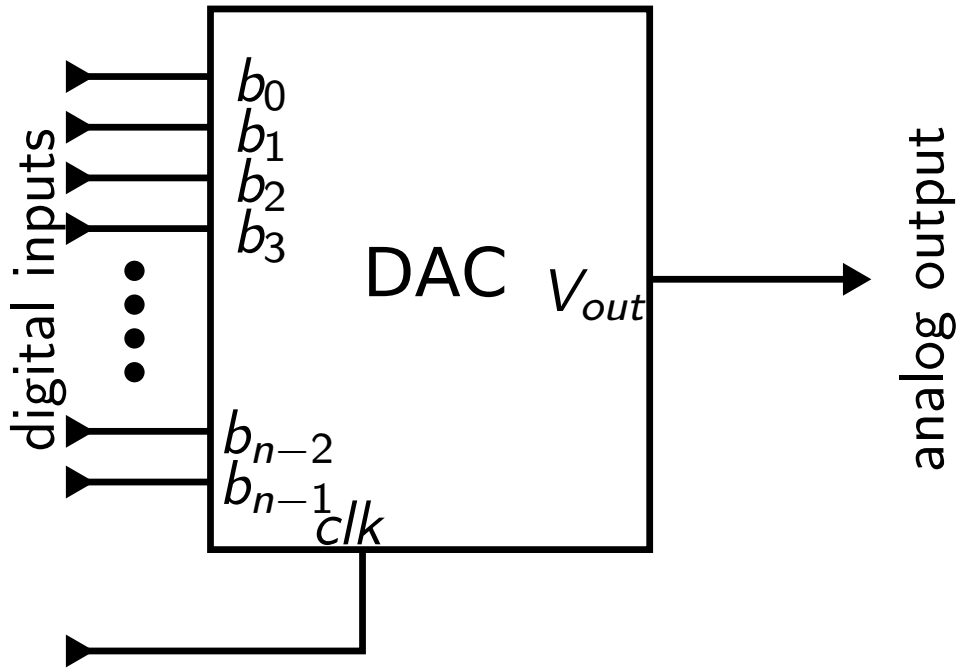
Dominik Przyborowski

April 1, 2009

Outline

1. DAC Architecture Overview
2. 10 bit Low–Power Small–Area Current–Steering DAC design.
   - Specification
   - Circuit Design.
   - Layout
3. 1^{st} Prototype Measurements Results
   - Static Measurements
   - Power Measurements
   - Transient Measurements
   - Comparison with other low–power 10 bit DACs
   - Possible Improvements.
4. Design of 2^{nd} prototype – Improvements.
   - Circuit.
   - Layout.

DAC Architecture Overview



Block diagram of digital–to–analog converter.

$$V_{out} = \sum_{k=0}^{n-1} b_k \cdot 2^k \cdot S_{ref},$$

S_{ref} – reference value (voltage, current or charge).

DAC Architecture Overview

Nyquist rate DACs architectures:

- charge division,
- resistor strings,
- voltage mode R–2R ladder,
- current mode R–2R ladder,
- current steering.

Oversampling DACs:

- $\Sigma - \Delta$ modulators – not discussed here.

DAC Architecture Overview

Nyquist rate DACs architectures:

- charge division,
- resistor strings,
- voltage mode R–2R ladder,
- current mode R–2R ladder,
- current steering.

Oversampling DACs:

- $\Sigma - \Delta$ modulators – not discussed here.

DAC Architecture Overview

Nyquist rate DACs architectures:

- charge division,
- resistor strings,
- voltage mode R–2R ladder,
- current mode R–2R ladder,
- current steering.

Oversampling DACs:

- $\Sigma - \Delta$ modulators – not discussed here.

DAC Architecture Overview

Nyquist rate DACs architectures:

- charge division,
- resistor strings,
- voltage mode R–2R ladder,
- current mode R–2R ladder,
- current steering.

Oversampling DACs:

- $\Sigma - \Delta$ modulators – not discussed here.

DAC Architecture Overview

Nyquist rate DACs architectures:

- charge division,
- resistor strings,
- voltage mode R–2R ladder,
- current mode R–2R ladder,
- current steering.

Oversampling DACs:

- $\Sigma - \Delta$ modulators – not discussed here.

DAC Architecture Overview

Nyquist rate DACs architectures:

- charge division,
- resistor strings,
- voltage mode R–2R ladder,
- current mode R–2R ladder,
- current steering.

Oversampling DACs:

- $\Sigma - \Delta$ modulators – not discussed here.

DAC Architecture Overview

Nyquist rate DACs architectures:

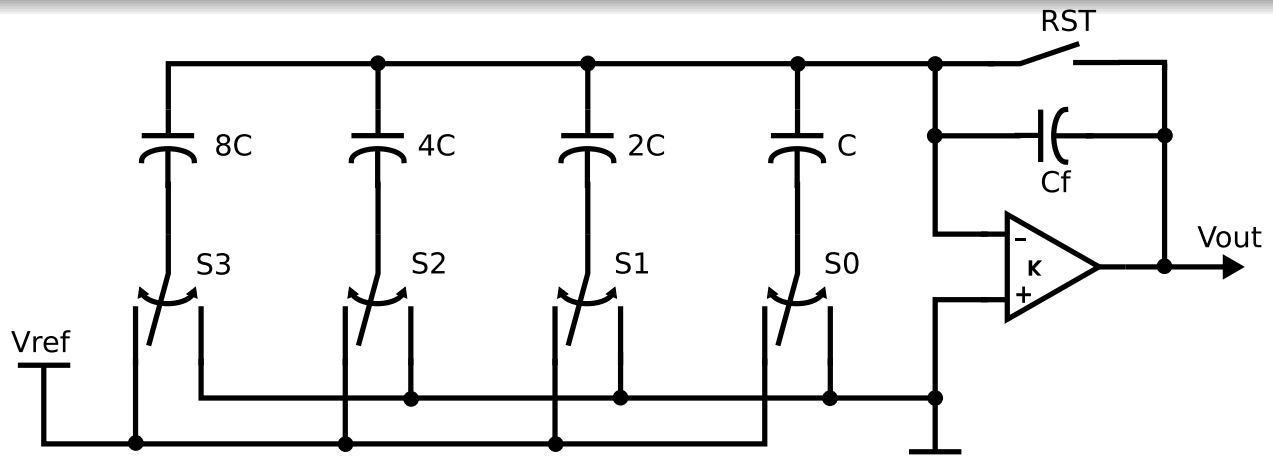
- charge division,
- resistor strings,
- voltage mode R–2R ladder,
- current mode R–2R ladder,
- current steering.

Oversampling DACs:

- $\Sigma - \Delta$ modulators – not discussed here.

DAC Architecture Overview

Charge Division.



4 bit binary–weighted capacitor DAC.

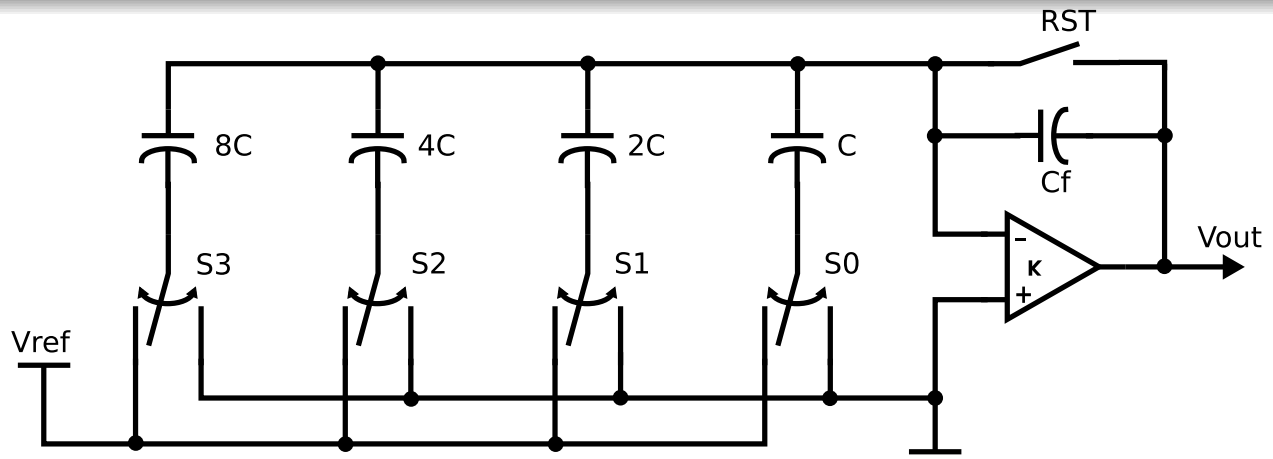
Properties

$$V_{out} = -\frac{C}{C_f} \cdot \sum_{k=0}^{N-1} 2^k \cdot S_k \cdot V_{ref}$$

- resolution up to 12 bits,
- low DC power consumption (only Op Amp and digital part),
- requires refreshing (capacitors leakage current is $\approx$ 1nA).

DAC Architecture Overview

Charge Division.



4 bit binary–weighted capacitor DAC.

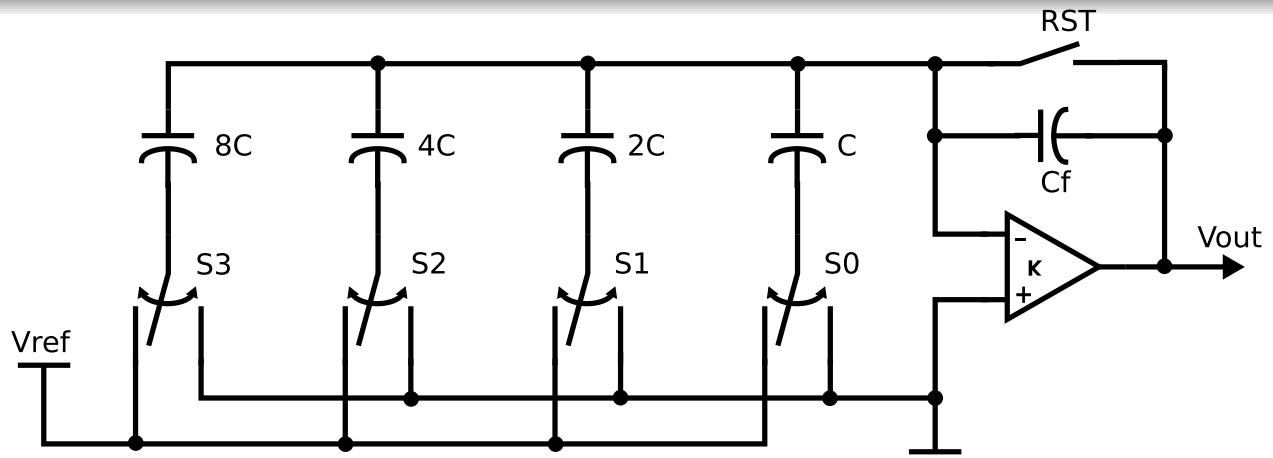
Properties

$$V_{out} = -\frac{C}{C_f} \cdot \sum_{k=0}^{N-1} 2^k \cdot S_k \cdot V_{ref}$$

- resolution up to 12 bits,
- low DC power consumption (only Op Amp and digital part)
- requires refreshing (capacitors leakage current is $\approx$ $1aA$)

DAC Architecture Overview

Charge Division.



4 bit binary–weighted capacitor DAC.

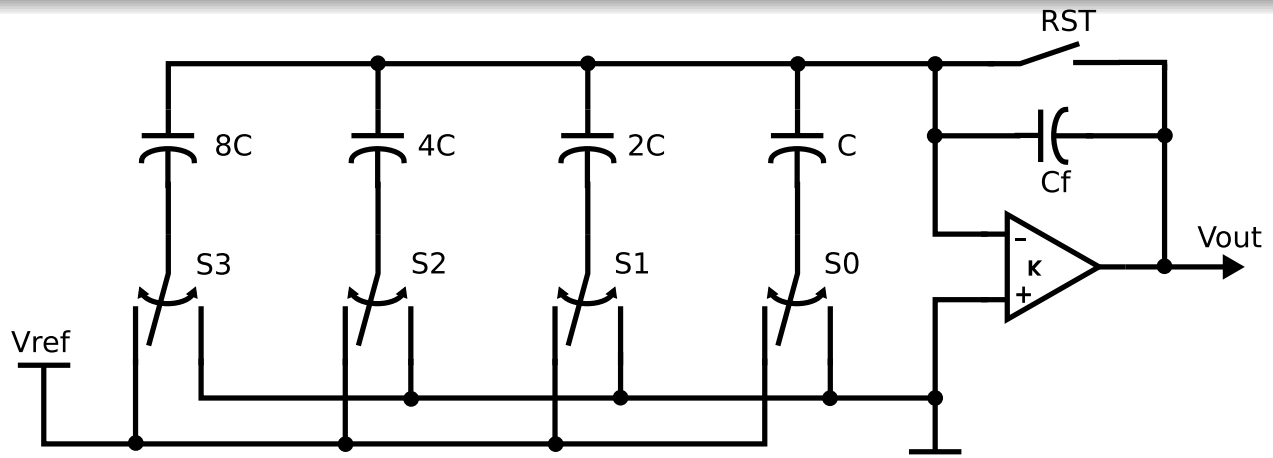
Properties

$$V_{out} = -\frac{C}{C_f} \cdot \sum_{k=0}^{N-1} 2^k \cdot S_k \cdot V_{ref}$$

- resolution up to 12 bits,
- low DC power consumption (only Op Amp and digital part)
- requires refreshing (capacitors leakage current is $\approx 1aA$)

DAC Architecture Overview

Charge Division.



4 bit binary–weighted capacitor DAC.

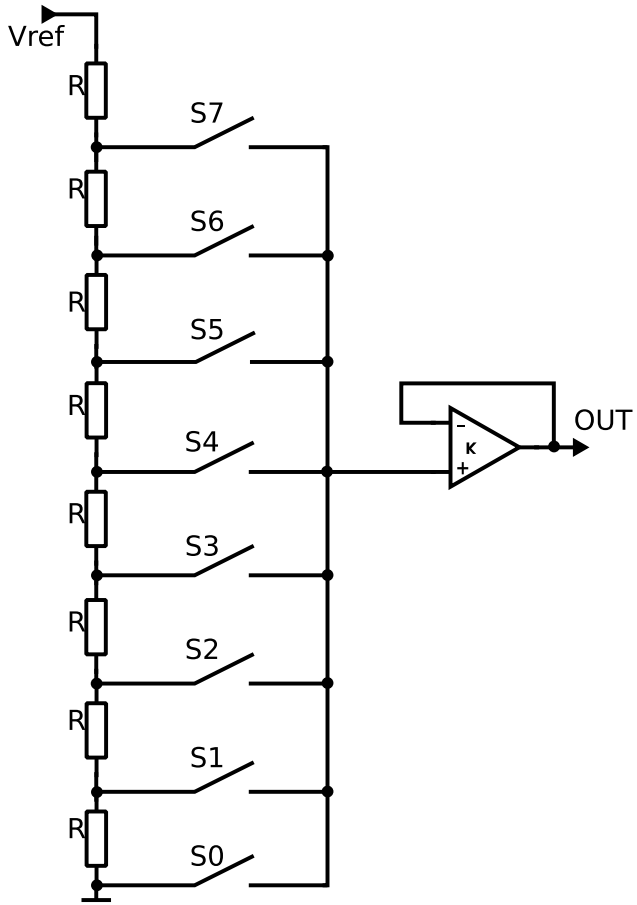
Properties

$$V_{out} = -\frac{C}{C_f} \cdot \sum_{k=0}^{N-1} 2^k \cdot S_k \cdot V_{ref}$$

- resolution up to 12 bits,
- low DC power consumption (only Op Amp and digital part)
- requires refreshing (capacitors leakage current is $\approx$ $1aA$)

DAC Architecture Overview

Resistor String.



3 bit resistor string DAC.

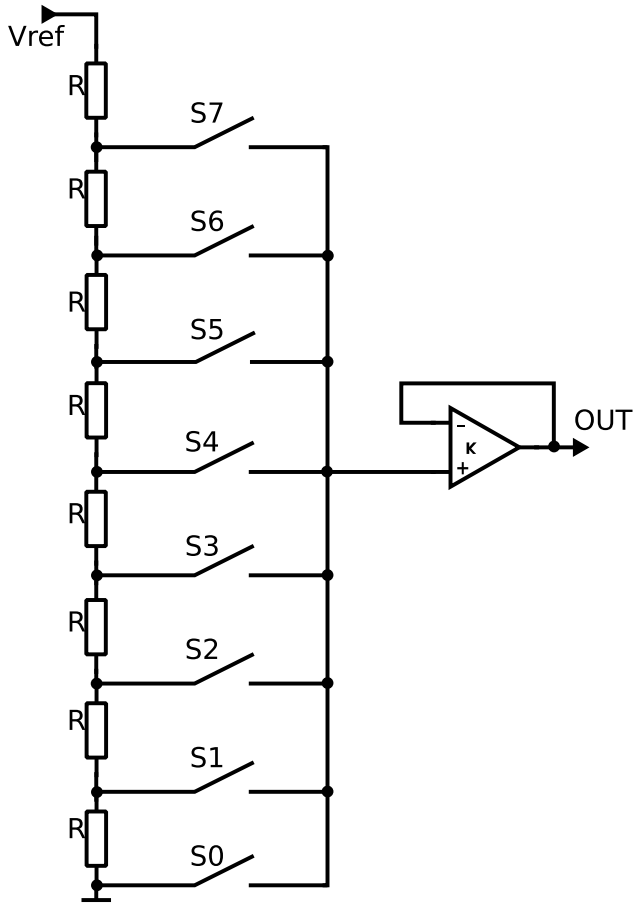
Properties

$$V_{out} = \frac{\sum_{k=0}^{N-1} S_k \cdot 2^k}{2^N} \cdot V_{ref}$$

- Requires rail-to-rail Op Amp.
- Requires *binary* → *1 from N* decoder.

DAC Architecture Overview

Resistor String.



3 bit resistor string DAC.

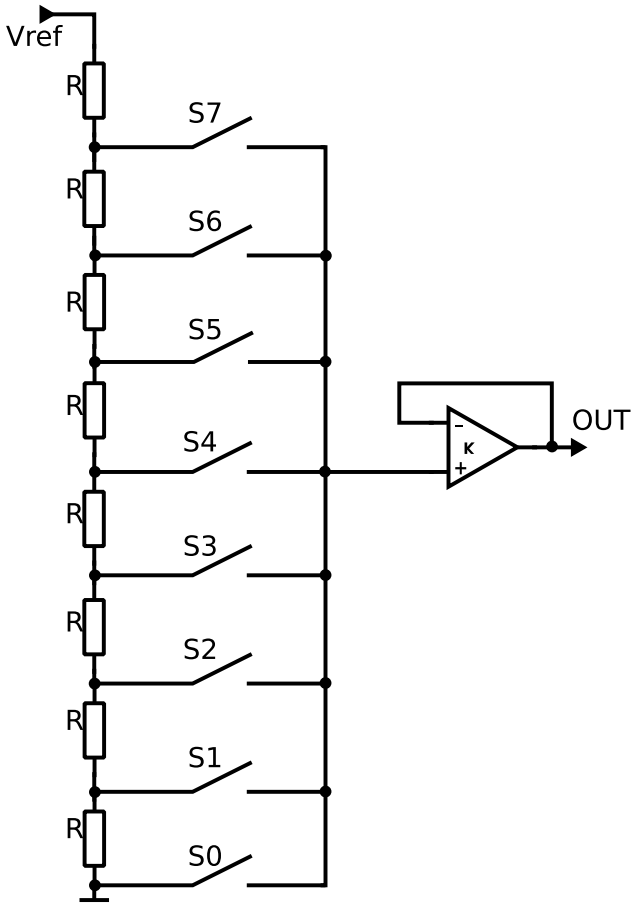
Properties

$$V_{out} = \frac{\sum_{k=0}^{N-1} S_k \cdot 2^k}{2^N} \cdot V_{ref}$$

- Requires rail–to–rail Op Amp.
- Requires *binary* $\longrightarrow$ *1 from N* decoder.

DAC Architecture Overview

Resistor String.



3 bit resistor string DAC.

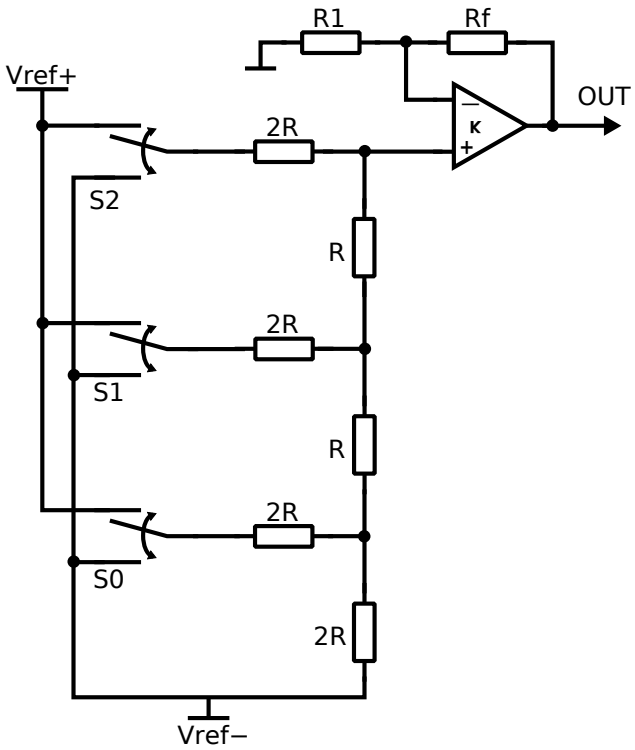
Properties

$$V_{out} = \frac{\sum_{k=0}^{N-1} S_k \cdot 2^k}{2^N} \cdot V_{ref}$$

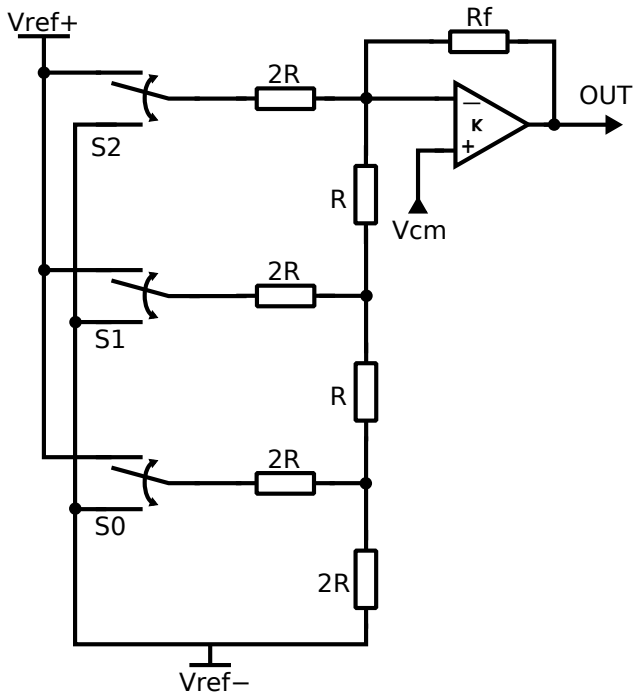
- Requires rail–to–rail Op Amp.
- Requires *binary* $\longrightarrow$ *1 from N* decoder.

DAC Architecture Overview

Resistor R–2R Ladder.



a) Voltage mode



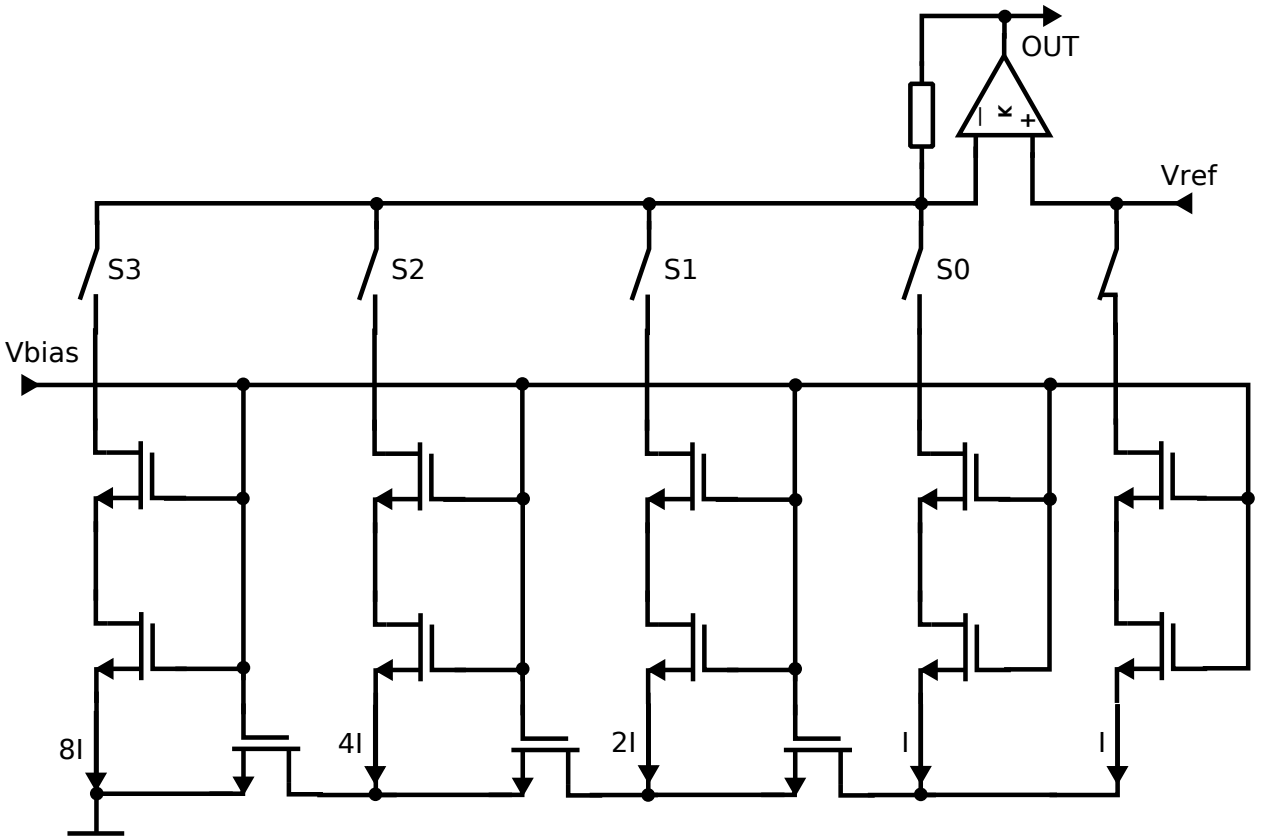
b) Current mode

$$V_{out} = \left(1 + \frac{R_f}{R_1}\right) \cdot \sum_{k=1}^{N} \frac{S_{N-k} \cdot V_{ref}}{2^k}$$

$$V_{out} = \frac{V_{ref}}{2}\left[1 + \frac{R_f}{R}\left(\sum_{k=1}^{N} \frac{S_{N-k}}{2^{N-k}} - 1\right)\right]$$

DAC Architecture Overview

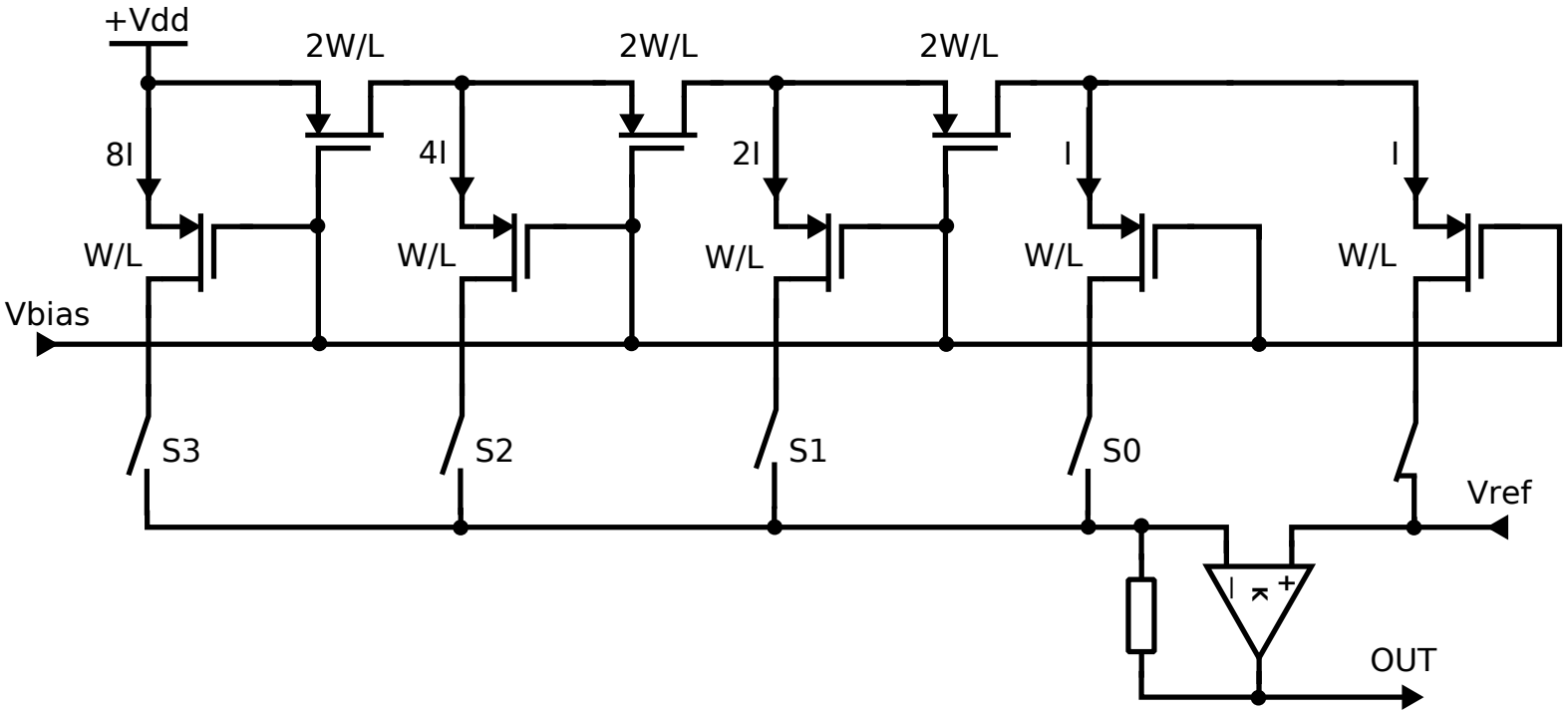
Resistor R–2R Ladder – MOS implementation I.



4 bit L–2L MOS Ladder DAC.

DAC Architecture Overview

Resistor R–2R Ladder – MOS implementation II.



4 bit W–2W MOS Ladder DAC.

DAC Architecture Overview

Resistor R–2R Ladder – MOS implementation III.

M-2M mismatch considerations

- In M–2M network transistors in different operational points.
- Matching in saturation region is determined by overdrive voltage:

$$\sigma(I_d) = \sqrt{\frac{A_\beta^2}{W \cdot L} + \left(\frac{2 \cdot 100\% \cdot A_{V_{th}}}{V_{ov}}\right)^2 \cdot \frac{1}{W \cdot L}}$$

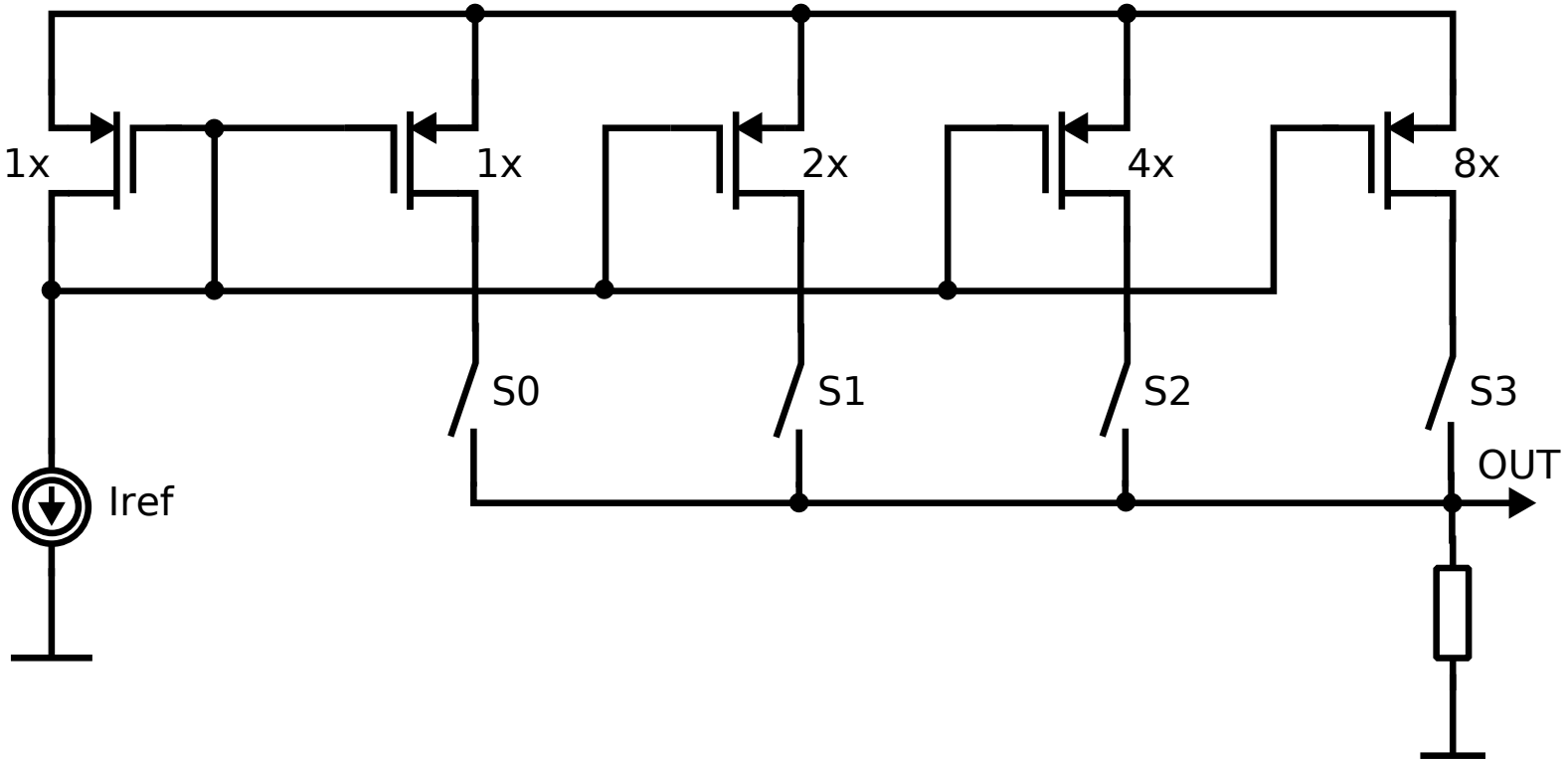
- Matching of MOS transistors in triode region is affected by output opamp offset:

$$\sigma(I_d) = \sqrt{\frac{A_\beta^2}{W \cdot L} + \left(\frac{100\% \cdot A_{V_{th}}}{V_{ov} - \frac{1}{2}V_{ds}}\right)^2 \cdot \frac{1}{W \cdot L} + \left(100\% \cdot \frac{\Delta V_{ds}}{V_{ds}}\right)^2}$$

- Simulations results required *special care* – problem with discontinuities of the BSIM transistors model.

DAC Architecture Overview

Current Steering.



4 bit Current Steering DAC.

$$V_{out} = I_{ref} \cdot R \cdot \sum_{K=0}^{N-1} S_k \cdot 2^k$$

Outline

10 bit Low–Power Small–Area Current–Steering DAC design.

Specification

Requirements:

- 10 bit resolution.
- High swing voltage output.
- Low power consumption – below 1 [mW].
- Small area.

Considered architectures:

- Current steering.
- Resistors ladder.

Chosen architecture:

- Current steering – matching of MOS better than resistors.

10 bit Low–Power Small–Area Current–Steering DAC design.

Specification

Requirements:

- 10 bit resolution.
- High swing voltage output.
- Low power consumption – below 1 [mW].
- Small area.

Considered architectures:

- Current steering.
- Resistors ladder.

Chosen architecture:

- Current steering – matching of MOS better than resistors.

10 bit Low–Power Small–Area Current–Steering DAC design.

Specification

Requirements:

- 10 bit resolution.
- High swing voltage output.
- Low power consumption – below 1 [mW].
- Small area.

Considered architectures:

- Current steering.
- Resistors ladder.

Chosen architecture:

- Current steering – matching of MOS better than resistors.

10 bit Low–Power Small–Area Current–Steering DAC design.

Specification

Requirements:

- 10 bit resolution.
- High swing voltage output.
- Low power consumption – below 1 [mW].
- Small area.

Considered architectures:

- Current steering.
- Resistors ladder.

Chosen architecture:

- Current steering – matching of MOS better than resistors.

10 bit Low–Power Small–Area Current–Steering DAC design.

Specification

Requirements:

- 10 bit resolution.
- High swing voltage output.
- Low power consumption – below 1 [mW].
- Small area.

Considered architectures:

- Current steering.
- Resistors ladder.

Chosen architecture:

- Current steering – matching of MOS better than resistors.

10 bit Low–Power Small–Area Current–Steering DAC design.

Specification

Requirements:

- 10 bit resolution.
- High swing voltage output.
- Low power consumption – below 1 [mW].
- Small area.

Considered architectures:

- Current steering.
- Resistors ladder.

Chosen architecture:

- Current steering – matching of MOS better than resistors.

10 bit Low–Power Small–Area Current–Steering DAC design.

Specification

Requirements:

- 10 bit resolution.
- High swing voltage output.
- Low power consumption – below 1 [mW].
- Small area.

Considered architectures:

- Current steering.
- Resistors ladder.

Chosen architecture:

- Current steering – matching of MOS better than resistors.

10 bit Low–Power Small–Area Current–Steering DAC design.

Specification

Requirements:

- 10 bit resolution.
- High swing voltage output.
- Low power consumption – below 1 [mW].
- Small area.

Considered architectures:

- Current steering.
- Resistors ladder.

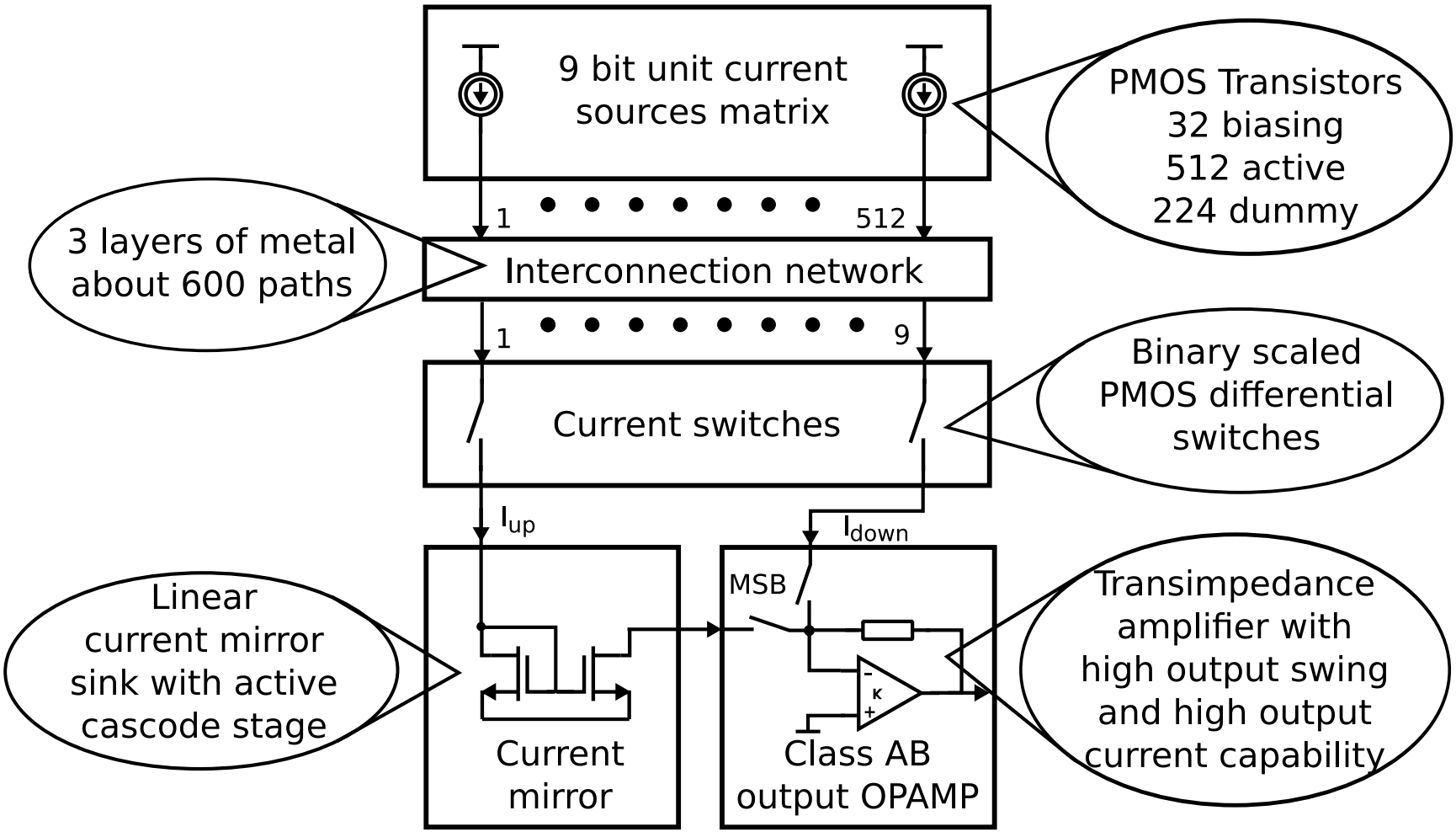
Chosen architecture:

- Current steering – matching of MOS better than resistors.

Outline

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design.



Block diagram of proposed DAC.

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – 9 bit Current Sources Array I.

Require for 9 bit resolution:

$$\delta I_{MSB} \leq \frac{1}{3} \cdot 2^{-9} \cdot 100\% = 0.065\%$$

Formulas for calculating dimensions:

$$\frac{W}{L} = \frac{2 \cdot I_D}{\beta \cdot V_{ov}^2}, \qquad \beta = \mu_0 \cdot C_{ox}$$

$$W \cdot L \geq \frac{1}{\sigma^2(I_D)} \cdot \left[A_\beta^2 + \left(\frac{2 \cdot A_{V_{th}}}{V_{ov}} \cdot 100\% \right)^2 \right]$$

Mismatch parameters in used technology:

NMOS: $A_\beta = 0.2\ [\mu m \cdot \%]$ $A_{V_{th}} = 8.2\ [\mu m \cdot mV]$

PMOS: $A_\beta = 0.4\ [\mu m \cdot \%]$ $A_{V_{th}} = 14.9\ [\mu m \cdot mV]$

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – 9 bit Current Sources Array I.

Require for 9 bit resolution:

$$\delta I_{MSB} \leq \frac{1}{3} \cdot 2^{-9} \cdot 100\% = 0.065\%$$

Formulas for calculating dimensions:

$$\frac{W}{L} = \frac{2 \cdot I_D}{\beta \cdot V_{ov}^2}, \qquad \beta = \mu_0 \cdot C_{ox}$$

$$W \cdot L \geq \frac{1}{\sigma^2(I_D)} \cdot \left[A_\beta^2 + \left(\frac{2 \cdot A_{V_{th}}}{V_{ov}} \cdot 100\% \right)^2 \right]$$

Mismatch parameters in used technology:

NMOS: $A_\beta = 0.2\ [\mu m \cdot \%]$ $A_{V_{th}} = 8.2\ [\mu m \cdot mV]$

PMOS: $A_\beta = 0.4\ [\mu m \cdot \%]$ $A_{V_{th}} = 14.9\ [\mu m \cdot mV]$

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – 9 bit Current Sources Array I.

Require for 9 bit resolution:

$$\delta I_{MSB} \leq \frac{1}{3} \cdot 2^{-9} \cdot 100\% = 0.065\%$$

Formulas for calculating dimensions:

$$\frac{W}{L} = \frac{2 \cdot I_D}{\beta \cdot V_{ov}^2}, \qquad \beta = \mu_0 \cdot C_{ox}$$

$$W \cdot L \geq \frac{1}{\sigma^2(I_D)} \cdot \left[A_\beta^2 + \left(\frac{2 \cdot A_{V_{th}}}{V_{ov}} \cdot 100\% \right)^2 \right]$$

Mismatch parameters in used technology:

NMOS: $A_\beta = 0.2\ [\mu m \cdot \%]$ $A_{V_{th}} = 8.2\ [\mu m \cdot mV]$

PMOS: $A_\beta = 0.4\ [\mu m \cdot \%]$ $A_{V_{th}} = 14.9\ [\mu m \cdot mV]$

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – 9 bit Current Sources Array II.

Choice of transistors size:

- Assumed LSB current $= 100[nA]$
- Assumed current source overdrive voltage $\geq 500[mV]$
- Chosen transistor type – PMOS
- Chosen W/L unit transistor ratio – 1/80 ($V_{ov} = 637[mV]$)
- Calculated unit current source dimensions – $0.5\mu/40\mu$

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – 9 bit Current Sources Array II.

Choice of transistors size:

- Assumed LSB current $= 100[nA]$
- Assumed current source overdrive voltage $\geq 500[mV]$
- Chosen transistor type – PMOS
- Chosen W/L unit transistor ratio – 1/80 ($V_{ov} = 637[mV]$)
- Calculated unit current source dimensions – $0.5\mu/40\mu$

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – 9 bit Current Sources Array II.

Choice of transistors size:

- Assumed LSB current $= 100[nA]$
- Assumed current source overdrive voltage $\geq 500[mV]$
- Chosen transistor type – PMOS
- Chosen W/L unit transistor ratio – $1/80$ ($V_{ov} = 637[mV]$)
- Calculated unit current source dimensions – $0.5\mu/40\mu$

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – 9 bit Current Sources Array II.

Choice of transistors size:

- Assumed LSB current $= 100[nA]$
- Assumed current source overdrive voltage $\geq 500[mV]$
- Chosen transistor type – PMOS
- Chosen W/L unit transistor ratio – 1/80 ($V_{ov} = 637[mV]$)
- Calculated unit current source dimensions – $0.5\mu/40\mu$

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – 9 bit Current Sources Array II.

Choice of transistors size:

- Assumed LSB current $= 100[nA]$
- Assumed current source overdrive voltage $\geq 500[mV]$
- Chosen transistor type – PMOS
- Chosen W/L unit transistor ratio – 1/80 ($V_{ov} = 637[mV]$)
- Calculated unit current source dimensions – $0.5\mu/40\mu$

10 bit Low–Power Small–Area Current–Steering DAC design.

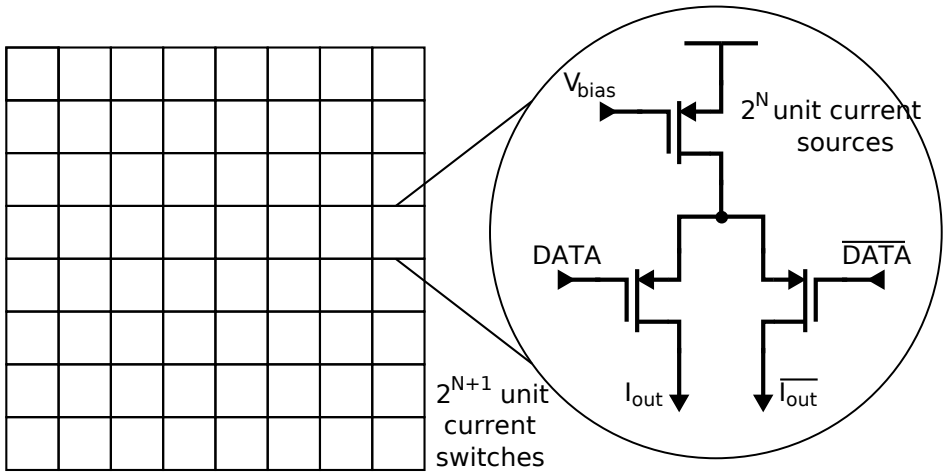
Circuit Design – 9 bit Current Sources Array II.

Choice of transistors size:

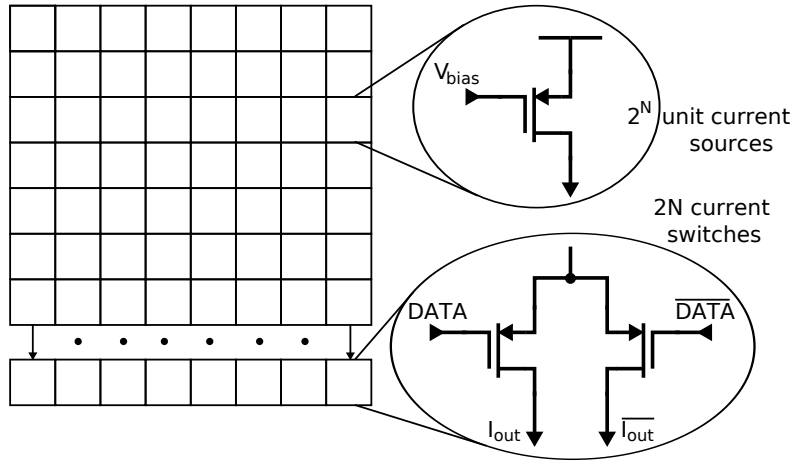
- Assumed LSB current $= 100[nA]$
- Assumed current source overdrive voltage $\geq 500[mV]$
- Chosen transistor type – PMOS
- Chosen W/L unit transistor ratio – 1/80 ($V_{ov} = 637[mV]$)
- Calculated unit current source dimensions – $0.5\mu/40\mu$

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Current Switches.



a) unary (best matching)



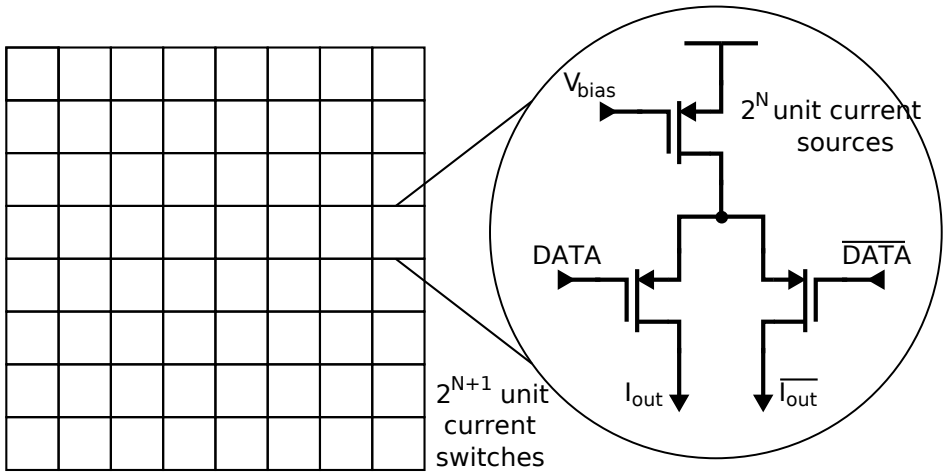
b) binary (lowest area)

Current switches – conclusion

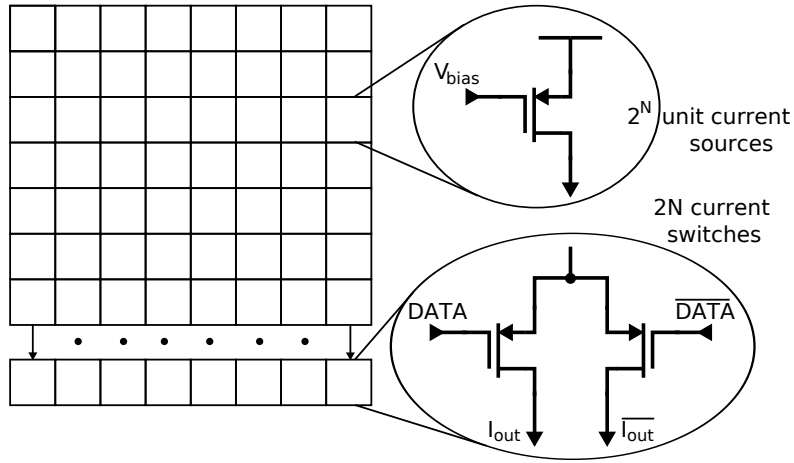
To minimize area binary switching (b) was chosen.
Dimensions of LSB switch – $0.4\mu/0.35\mu$.

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Current Switches.



a) unary (best matching)



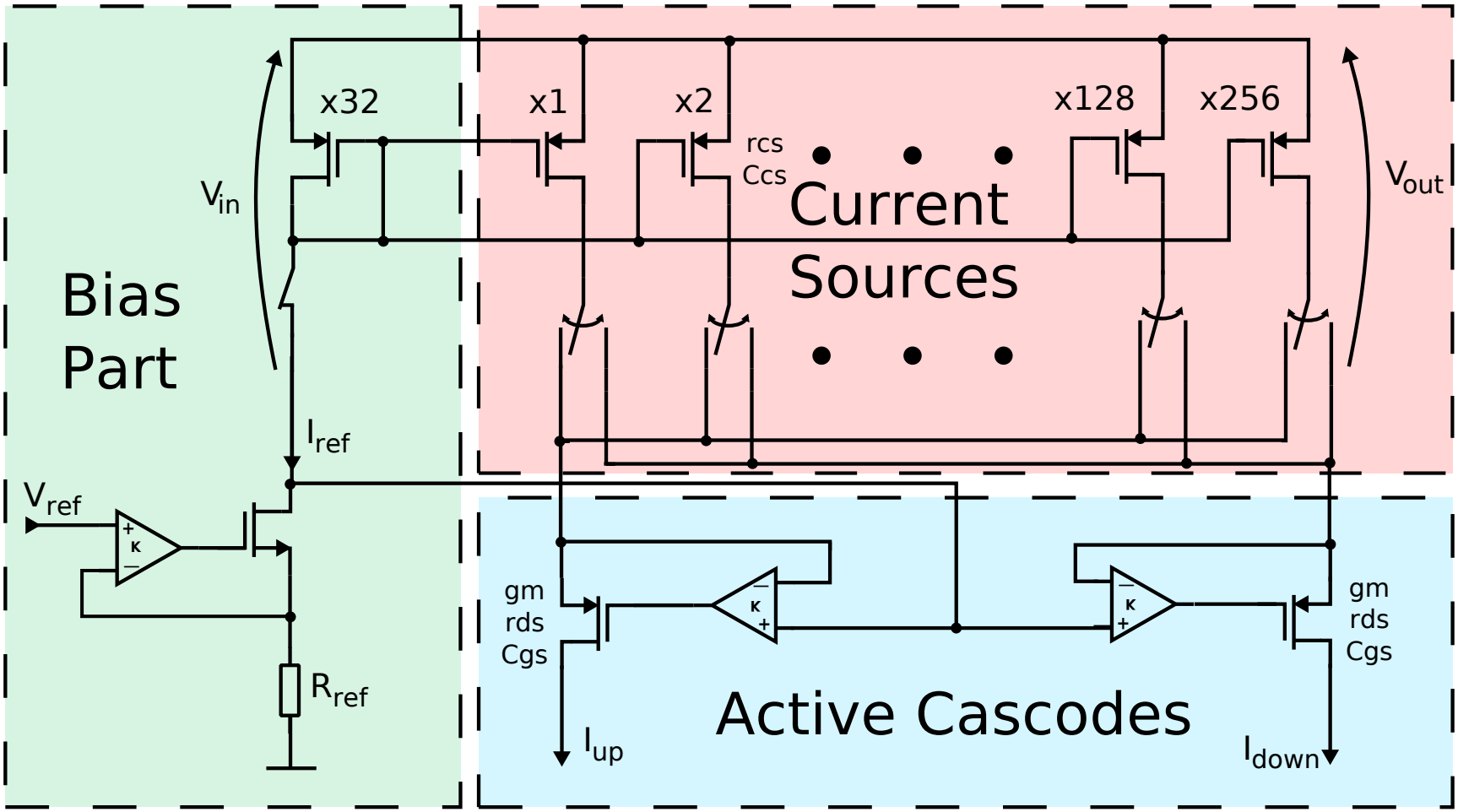
b) binary (lowest area)

Current switches – conclusion

To minimize area binary switching (b) was chosen.
Dimensions of LSB switch – $0.4\mu/0.35\mu$.

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Current Source Array with Active Cascodes Stage.



Bias circuit, current sources array and active cascode stage.

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Active Cascode Stage.

Advantages of active cascodes:

- Drain current independent from channel modulation factor.
- Strongly increases output resistance:

$$r_{out} \simeq K \cdot g_m \cdot r_{ds} \cdot r_{CS} \approx 10^{14} \div 10^{16} \Omega$$

- Glitch reduction.

Possibles problems:

- Stability

dominant pole	nondominant pole
p_1 of OTA	$\frac{g_m}{C_{gs} + \frac{C_{CS}}{K}}$

Needs minimum current!

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Active Cascode Stage.

Advantages of active cascodes:

- Drain current independent from channel modulation factor.
- Strongly increases output resistance:

$$r_{out} \simeq K \cdot g_m \cdot r_{ds} \cdot r_{CS} \approx 10^{14} \div 10^{16} \Omega$$

- Glitch reduction.

Possibles problems:

- Stability

dominant pole	nondominant pole
p_1 of OTA	$\frac{g_m}{C_{gs} + \frac{C_{CS}}{K}}$

Needs minimum current!

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Active Cascode Stage.

Advantages of active cascodes:

- Drain current independent from channel modulation factor.
- Strongly increases output resistance:

$$r_{out} \simeq K \cdot g_m \cdot r_{ds} \cdot r_{CS} \approx 10^{14} \div 10^{16} \Omega$$

- Glitch reduction.

Possibles problems:

- Stability

dominant pole	nondominant pole
p_1 of OTA	$\frac{g_m}{C_{gs} + \frac{C_{CS}}{K}}$

Needs minimum current!

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Active Cascode Stage.

Advantages of active cascodes:

- Drain current independent from channel modulation factor.
- Strongly increases output resistance:

$$r_{out} \simeq K \cdot g_m \cdot r_{ds} \cdot r_{CS} \approx 10^{14} \div 10^{16} \Omega$$

- Glitch reduction.

Possibles problems:

- Stability

dominant pole	nondominant pole
p_1 of OTA	$\frac{g_m}{C_{gs} + \frac{C_{CS}}{K}}$

Needs minimum current!

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Active Cascode Stage.

Advantages of active cascodes:

- Drain current independent from channel modulation factor.
- Strongly increases output resistance:

$$r_{out} \simeq K \cdot g_m \cdot r_{ds} \cdot r_{CS} \approx 10^{14} \div 10^{16} \Omega$$

- Glitch reduction.

Possibles problems:

- Stability

dominant pole	nondominant pole
p_1 of OTA	$\frac{g_m}{C_{gs} + \frac{C_{CS}}{K}}$

Needs minimum current!

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Active Cascode Stage.

Advantages of active cascodes:

- Drain current independent from channel modulation factor.
- Strongly increases output resistance:

$$r_{out} \simeq K \cdot g_m \cdot r_{ds} \cdot r_{CS} \approx 10^{14} \div 10^{16} \Omega$$

- Glitch reduction.

Possibles problems:

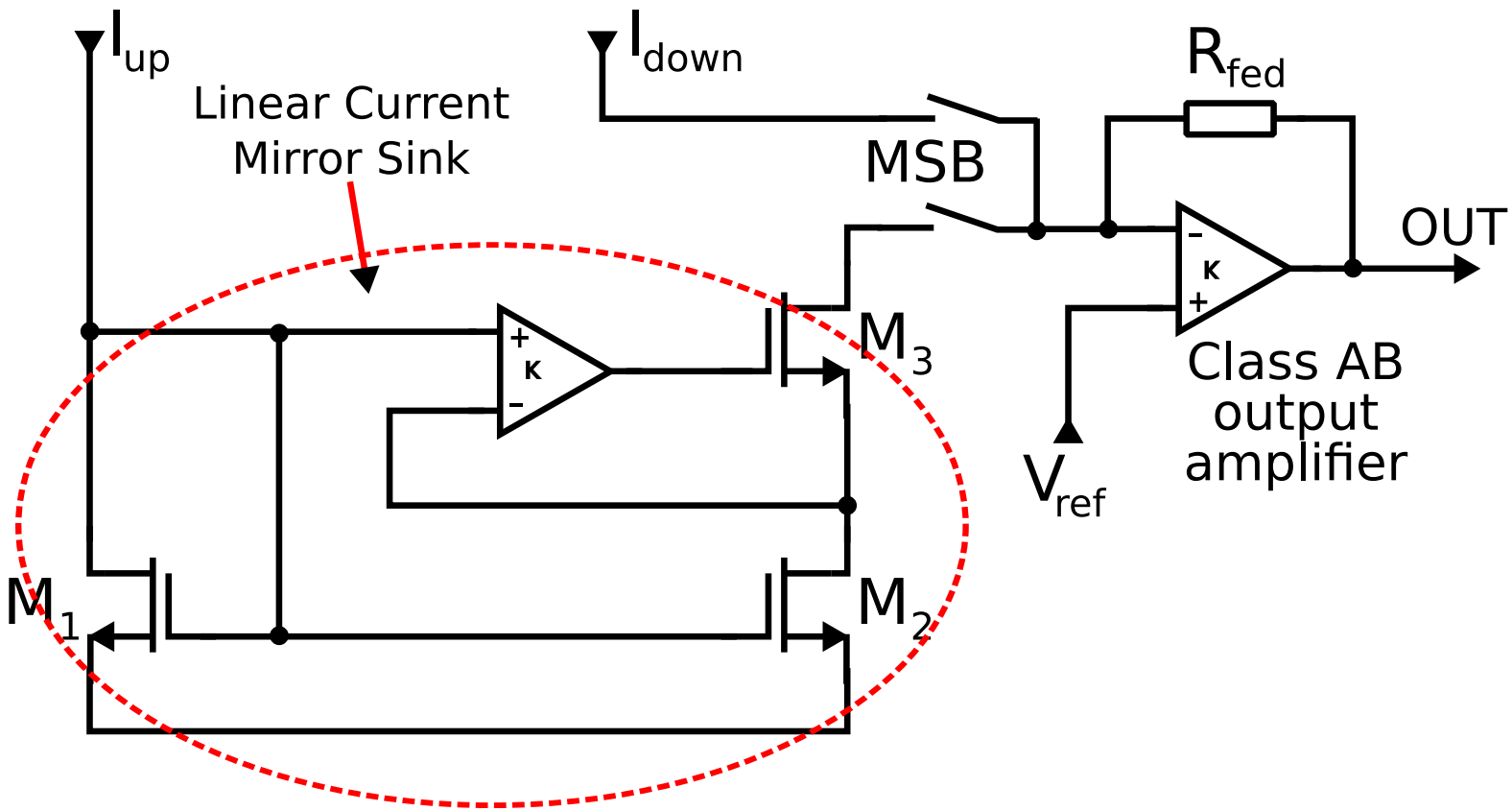
- Stability

dominant pole	nondominant pole
p_1 of OTA	$\frac{g_m}{C_{gs} + \frac{C_{CS}}{K}}$

Needs minimum current!

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – High Swing Output Stage (Including Current Mirror Sink) I.



$$\frac{W_1}{L_1} = \frac{W_2}{L_2} = 16 \cdot \frac{3.2\mu}{52.5\mu}$$

High swing output circuit.

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – High Swing Output Stage II.

Relation between I_{down} and I_{up}:

$$I_{down} = 511 \cdot I_{LSB} - B_{dec} \cdot I_{up}$$

B_{dec} – decimal representation of input word (without MSB bit).

Output voltage:

- MSB $= 0$: $V_{out} = V_{ref} - (511 - B_{dec}) \cdot I_{LSB} \cdot R_{fed}$
- MSB $= 1$: $V_{out} = V_{ref} + B_{dec} \cdot I_{LSB} \cdot R_{fed}$

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – High Swing Output Stage II.

Relation between I_{down} and I_{up}:

$$I_{down} = 511 \cdot I_{LSB} - B_{dec} \cdot I_{up}$$

B_{dec} – decimal representation of input word (without MSB bit).

Output voltage:

- MSB = 0: $V_{out} = V_{ref} - (511 - B_{dec}) \cdot I_{LSB} \cdot R_{fed}$
- MSB = 1: $V_{out} = V_{ref} + B_{dec} \cdot I_{LSB} \cdot R_{fed}$

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – High Swing Output Stage II.

Relation between I_{down} and I_{up}:

$$I_{down} = 511 \cdot I_{LSB} - B_{dec} \cdot I_{up}$$

B_{dec} – decimal representation of input word (without MSB bit).

Output voltage:

- MSB = 0: $V_{out} = V_{ref} - (511 - B_{dec}) \cdot I_{LSB} \cdot R_{fed}$
- MSB = 1: $V_{out} = V_{ref} + B_{dec} \cdot I_{LSB} \cdot R_{fed}$

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Single Stage OTAs.

Two types of amplifiers were used:

- Single stage OTAs in active cascode stages and biasing. Depending on voltage level OTA use either NMOS or PMOS input differential pair.
- Two stage class AB operational amplifier for output current–to–voltage converter.

Single stage OTA – details:

- Architecture – folded cascode.
- Power consumption [μW] – 3.5 (NMOS), 25 (PMOS).
- Open loop Gain [dB] – 60 (NMOS), 88 (PMOS).
- Gain x Bandwidth (GBW) [MHz] – 1 (NMOS), 7 (PMOS).
- Phase Margin $>$ 70°.

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Single Stage OTAs.

Two types of amplifiers were used:

- Single stage OTAs in active cascode stages and biasing. Depending on voltage level OTA use either NMOS or PMOS input differential pair.
- Two stage class AB operational amplifier for output current–to–voltage converter.

Single stage OTA – details:

- Architecture – folded cascode.
- Power consumption $[\mu W]$ – 3.5 (NMOS), 25 (PMOS).
- Open loop Gain [dB] – 60 (NMOS), 88 (PMOS).
- Gain x Bandwidth (GBW) [MHz] – 1 (NMOS), 7 (PMOS).
- Phase Margin $>$ 70^o.

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Single Stage OTAs.

Two types of amplifiers were used:

- Single stage OTAs in active cascode stages and biasing. Depending on voltage level OTA use either NMOS or PMOS input differential pair.
- Two stage class AB operational amplifier for output current–to–voltage converter.

Single stage OTA – details:

- Architecture – folded cascode.
- Power consumption [μW] – 3.5 (NMOS), 25 (PMOS).
- Open loop Gain [dB] – 60 (NMOS), 88 (PMOS).
- Gain x Bandwidth (GBW) [MHz] – 1 (NMOS), 7 (PMOS).
- Phase Margin $>$ 70°.

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Single Stage OTAs.

Two types of amplifiers were used:

- Single stage OTAs in active cascode stages and biasing. Depending on voltage level OTA use either NMOS or PMOS input differential pair.
- Two stage class AB operational amplifier for output current–to–voltage converter.

Single stage OTA – details:

- Architecture – folded cascode.
- Power consumption [μW] – 3.5 (NMOS), 25 (PMOS).
- Open loop Gain [dB] – 60 (NMOS), 88 (PMOS).
- Gain x Bandwidth (GBW) [MHz] – 1 (NMOS), 7 (PMOS).
- Phase Margin $>$ 70°.

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Single Stage OTAs.

Two types of amplifiers were used:

- Single stage OTAs in active cascode stages and biasing. Depending on voltage level OTA use either NMOS or PMOS input differential pair.
- Two stage class AB operational amplifier for output current–to–voltage converter.

Single stage OTA – details:

- Architecture – folded cascode.
- Power consumption [μW] – 3.5 (NMOS), 25 (PMOS).
- Open loop Gain [dB] – 60 (NMOS), 88 (PMOS).
- Gain x Bandwidth (GBW) [MHz] – 1 (NMOS), 7 (PMOS).
- Phase Margin $>$ 70^o.

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Single Stage OTAs.

Two types of amplifiers were used:

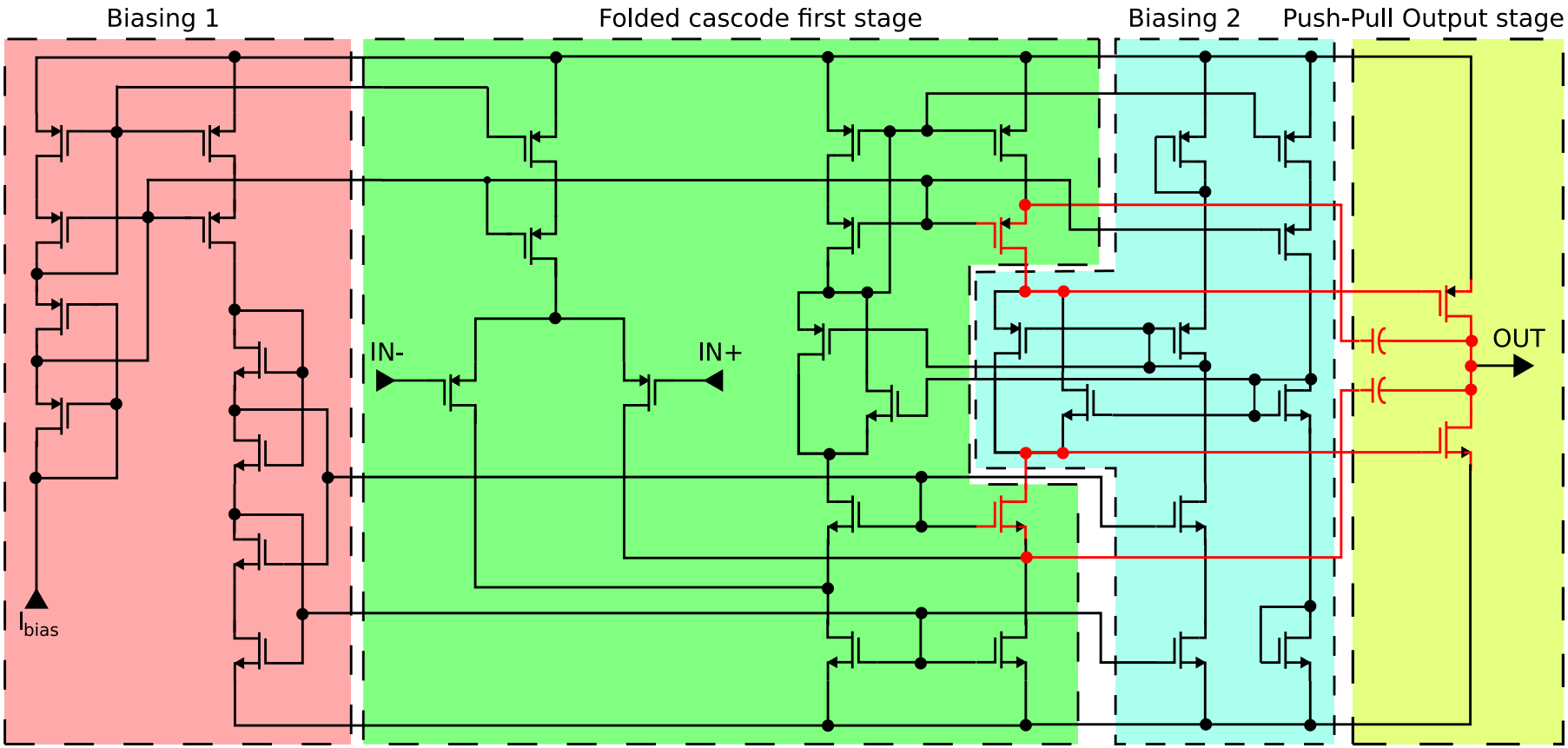
- Single stage OTAs in active cascode stages and biasing. Depending on voltage level OTA use either NMOS or PMOS input differential pair.
- Two stage class AB operational amplifier for output current–to–voltage converter.

Single stage OTA – details:

- Architecture – folded cascode.
- Power consumption [μW] – 3.5 (NMOS), 25 (PMOS).
- Open loop Gain [dB] – 60 (NMOS), 88 (PMOS).
- Gain x Bandwidth (GBW) [MHz] – 1 (NMOS), 7 (PMOS).
- Phase Margin $>$ 70^o.

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Class AB Operational Amplifier I.



Schematic of output class AB operational amplifier.

Cascoded Miller compensation.

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Class AB Operational Amplifier II.

Class AB OP–AMP:

- *Sooch* cascode current mirror used for biasing.
- 1^{st} stage build as a folded cascode.
- Bias of Push–Pull output stage designed as *floating current source*.
- Push–Pull output stage with cascoded Miller compensation technique.

Cascoded Miller compensation technique pros and cons:

- ✓ Better PSRR (Power Supply Rejection Ratio).
- ✓ Needs 2–3 times smaller comp. cap. (wider bandwidth).
- ✓ Doesn't require resistor.
- ✗ Complicated transfer function – 3 poles and 2 zeros (problems with high frequency gain peak).

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Class AB Operational Amplifier II.

Class AB OP–AMP:

- *Sooch* cascode current mirror used for biasing.
- 1^{st} stage build as a folded cascode.
- Bias of Push–Pull output stage designed as *floating current source*.
- Push–Pull output stage with cascoded Miller compensation technique.

Cascoded Miller compensation technique pros and cons:

- ✓ Better PSRR (Power Supply Rejection Ratio).
- ✓ Needs 2–3 times smaller comp. cap. (wider bandwidth).
- ✓ Doesn't require resistor.
- ✗ Complicated transfer function – 3 poles and 2 zeros (problems with high frequency gain peak).

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Class AB Operational Amplifier II.

Class AB OP–AMP:

- *Sooch* cascode current mirror used for biasing.
- 1^{st} stage build as a folded cascode.
- Bias of Push–Pull output stage designed as *floating current source*.
- Push–Pull output stage with cascoded Miller compensation technique.

Cascoded Miller compensation technique pros and cons:

- ✓ Better PSRR (Power Supply Rejection Ratio).
- ✓ Needs 2–3 times smaller comp. cap. (wider bandwidth).
- ✓ Doesn't require resistor.
- ✗ Complicated transfer function – 3 poles and 2 zeros (problems with high frequency gain peak).

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Class AB Operational Amplifier II.

Class AB OP–AMP:

- *Sooch* cascode current mirror used for biasing.
- 1^{st} stage build as a folded cascode.
- Bias of Push–Pull output stage designed as *floating current source*.
- Push–Pull output stage with cascoded Miller compensation technique.

Cascoded Miller compensation technique pros and cons:

- ✓ Better PSRR (Power Supply Rejection Ratio).
- ✓ Needs 2–3 times smaller comp. cap. (wider bandwidth).
- ✓ Doesn't require resistor.
- ✗ Complicated transfer function – 3 poles and 2 zeros (problems with high frequency gain peak).

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Class AB Operational Amplifier II.

Class AB OP–AMP:

- *Sooch* cascode current mirror used for biasing.
- 1^{st} stage build as a folded cascode.
- Bias of Push–Pull output stage designed as *floating current source*.
- Push–Pull output stage with cascoded Miller compensation technique.

Cascoded Miller compensation technique pros and cons:

- ✓ Better PSRR (Power Supply Rejection Ratio).
- ✓ Needs 2–3 times smaller comp. cap. (wider bandwidth).
- ✓ Doesn't require resistor.
- ✗ Complicated transfer function – 3 poles and 2 zeros (problems with high frequency gain peak).

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Class AB Operational Amplifier II.

Class AB OP–AMP:

- *Sooch* cascode current mirror used for biasing.
- 1^{st} stage build as a folded cascode.
- Bias of Push–Pull output stage designed as *floating current source*.
- Push–Pull output stage with cascoded Miller compensation technique.

Cascoded Miller compensation technique pros and cons:

- ✔ Better PSRR (Power Supply Rejection Ratio).
- ✔ Needs 2–3 times smaller comp. cap. (wider bandwidth).
- ✔ Doesn't require resistor.
- ✘ Complicated transfer function – 3 poles and 2 zeros (problems with high frequency gain peak).

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Class AB Operational Amplifier II.

Class AB OP–AMP:

- *Sooch* cascode current mirror used for biasing.
- 1^{st} stage build as a folded cascode.
- Bias of Push–Pull output stage designed as *floating current source*.
- Push–Pull output stage with cascoded Miller compensation technique.

Cascoded Miller compensation technique pros and cons:

- ✔ Better PSRR (Power Supply Rejection Ratio).
- ✔ Needs 2–3 times smaller comp. cap. (wider bandwidth).
- ✔ Doesn't require resistor.
- ✘ Complicated transfer function – 3 poles and 2 zeros (problems with high frequency gain peak).

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Class AB Operational Amplifier II.

Class AB OP–AMP:

- *Sooch* cascode current mirror used for biasing.
- 1^{st} stage build as a folded cascode.
- Bias of Push–Pull output stage designed as *floating current source*.
- Push–Pull output stage with cascoded Miller compensation technique.

Cascoded Miller compensation technique pros and cons:

- ✔ Better PSRR (Power Supply Rejection Ratio).
- ✔ Needs 2–3 times smaller comp. cap. (wider bandwidth).
- ✔ Doesn't require resistor.
- ✘ Complicated transfer function – 3 poles and 2 zeros (problems with high frequency gain peak).

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Class AB Operational Amplifier II.

Class AB OP–AMP:

- *Sooch* cascode current mirror used for biasing.
- 1^{st} stage build as a folded cascode.
- Bias of Push–Pull output stage designed as *floating current source*.
- Push–Pull output stage with cascoded Miller compensation technique.

Cascoded Miller compensation technique pros and cons:

- ✔ Better PSRR (Power Supply Rejection Ratio).
- ✔ Needs 2–3 times smaller comp. cap. (wider bandwidth).
- ✔ Doesn't require resistor.
- ✘ Complicated transfer function – 3 poles and 2 zeros (problems with high frequency gain peak).

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Class AB Operational Amplifier II.

Class AB OP–AMP:

- *Sooch* cascode current mirror used for biasing.
- 1^{st} stage build as a folded cascode.
- Bias of Push–Pull output stage designed as *floating current source*.
- Push–Pull output stage with cascoded Miller compensation technique.

Cascoded Miller compensation technique pros and cons:

- ✔ Better PSRR (Power Supply Rejection Ratio).
- ✔ Needs 2–3 times smaller comp. cap. (wider bandwidth).
- ✔ Doesn't require resistor.
- ✘ Complicated transfer function – 3 poles and 2 zeros (problems with high frequency gain peak).

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Class AB Operational Amplifier III.

Class AB OP–AMP parameters:

- Power consumption – 65 μW $(+V_{dd} \cdot I_{out})$.
- Open loop gain – 115 dB (for zero current load)
- GBW – 2 MHz
- Phase Margin $>$ 75^{o}.

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Class AB Operational Amplifier III.

Class AB OP–AMP parameters:

- Power consumption – 65 μW $(+V_{dd} \cdot I_{out})$.
- Open loop gain – 115 dB (for zero current load)
- GBW – 2 MHz
- Phase Margin $>$ 75^{o}.

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Class AB Operational Amplifier III.

Class AB OP–AMP parameters:

- Power consumption – 65 μW $(+V_{dd} \cdot I_{out})$.
- Open loop gain – 115 dB (for zero current load)
- GBW – 2 MHz
- Phase Margin $>$ 75^{o}.

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Class AB Operational Amplifier III.

Class AB OP–AMP parameters:

- Power consumption – 65 μW $(+V_{dd} \cdot I_{out})$.
- Open loop gain – 115 dB (for zero current load)
- GBW – 2 MHz
- Phase Margin $>$ 75^{o}.

10 bit Low–Power Small–Area Current–Steering DAC design.

Circuit Design – Class AB Operational Amplifier III.

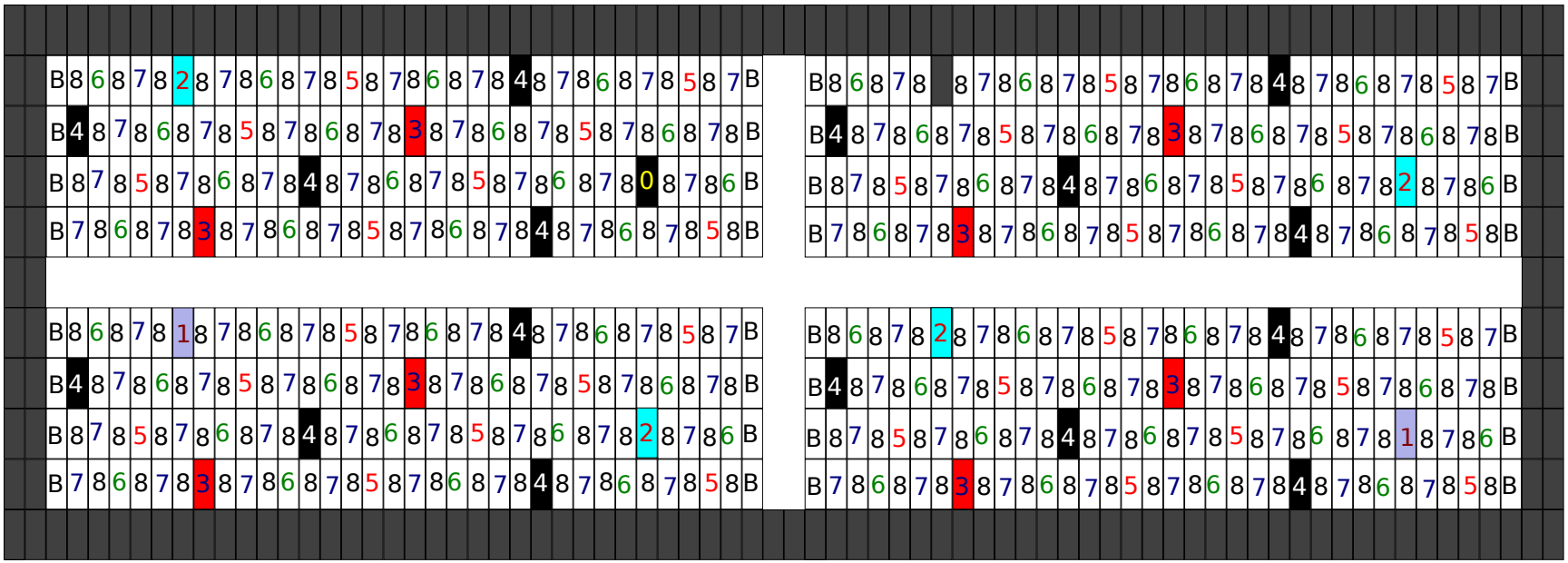
Class AB OP–AMP parameters:

- Power consumption – 65 μW $(+V_{dd} \cdot I_{out})$.
- Open loop gain – 115 dB (for zero current load)
- GBW – 2 MHz
- Phase Margin $>$ 75^{o}.

Outline

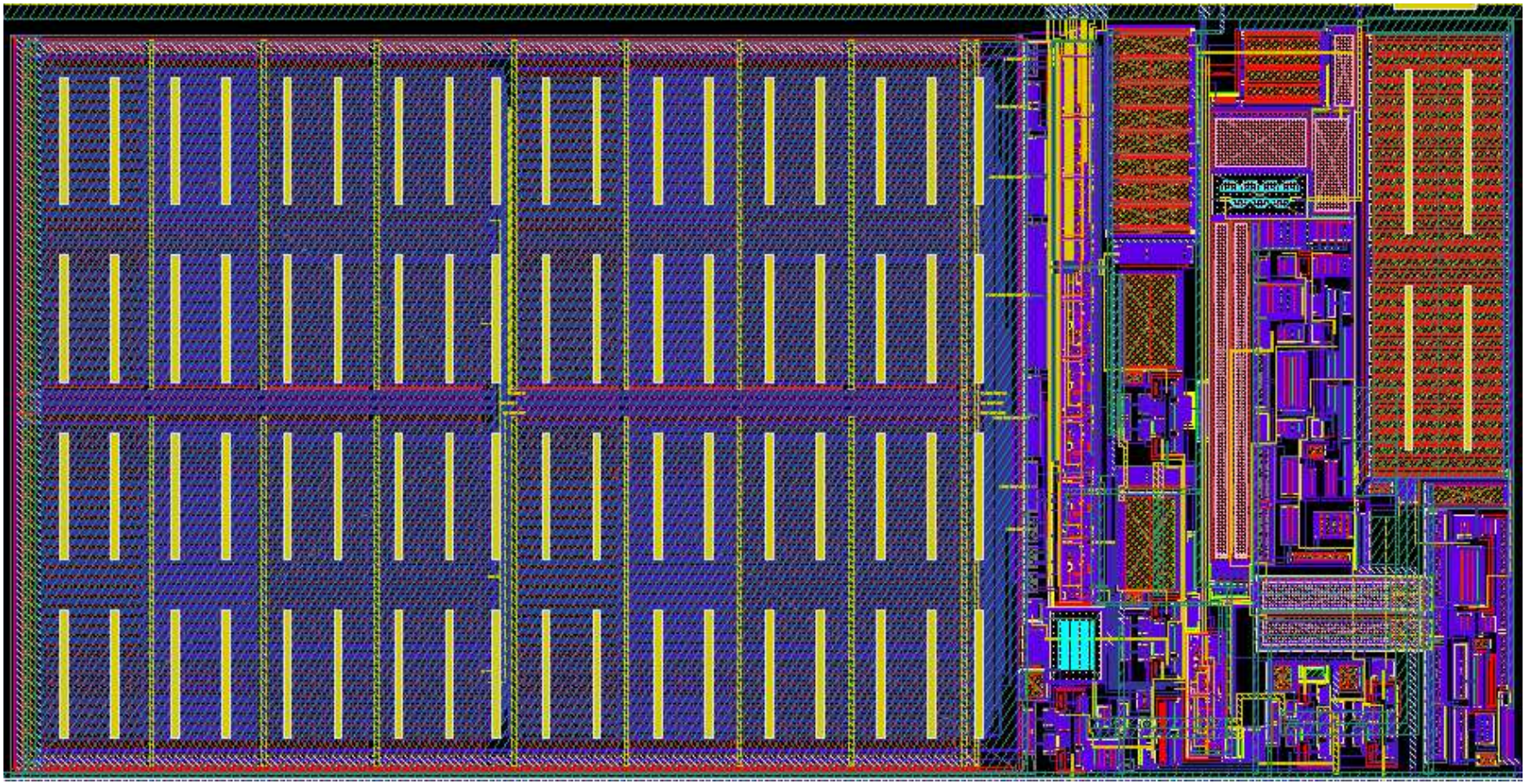
Layout

9 bit Current Sources Array.



Block Diagram of DAC Matrix Layout.

Layout
DAC Core.

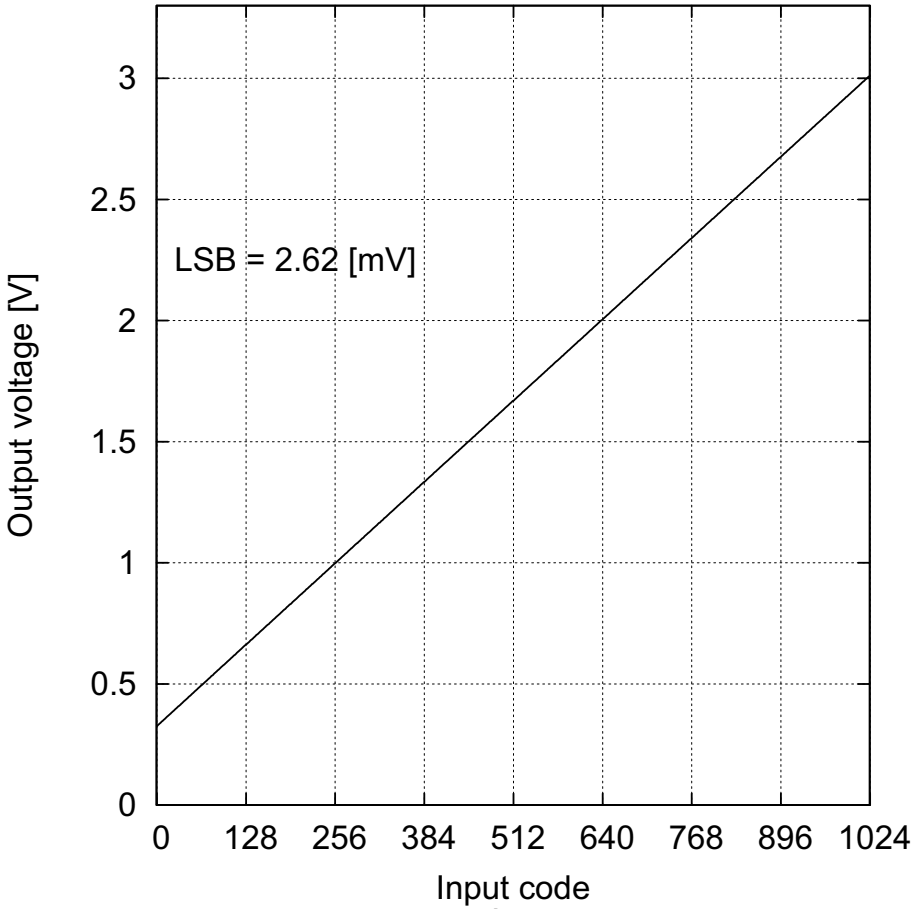


Layout of 1^{st} prototype (295x595μm).

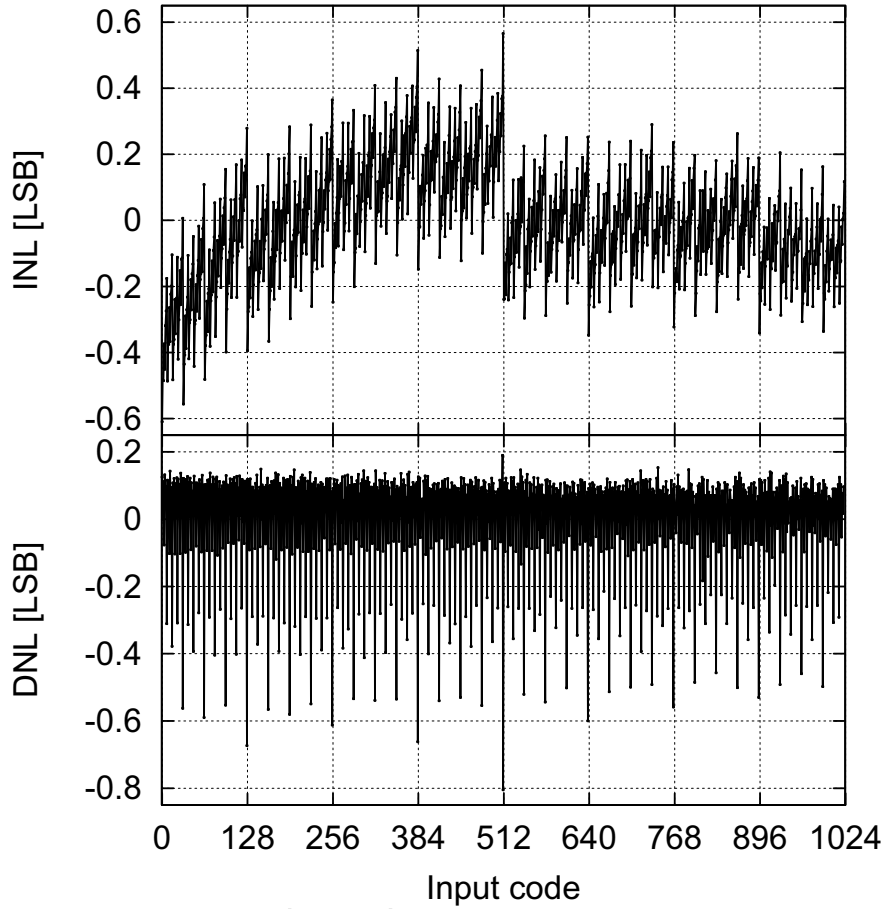
Outline

1^{st} Prototype Measurements Results

Static Measurements I.



DAC transfer curve



Integral (INL) and differential (DNL) nonlinearities.

1^{st} Prototype Measurements Results

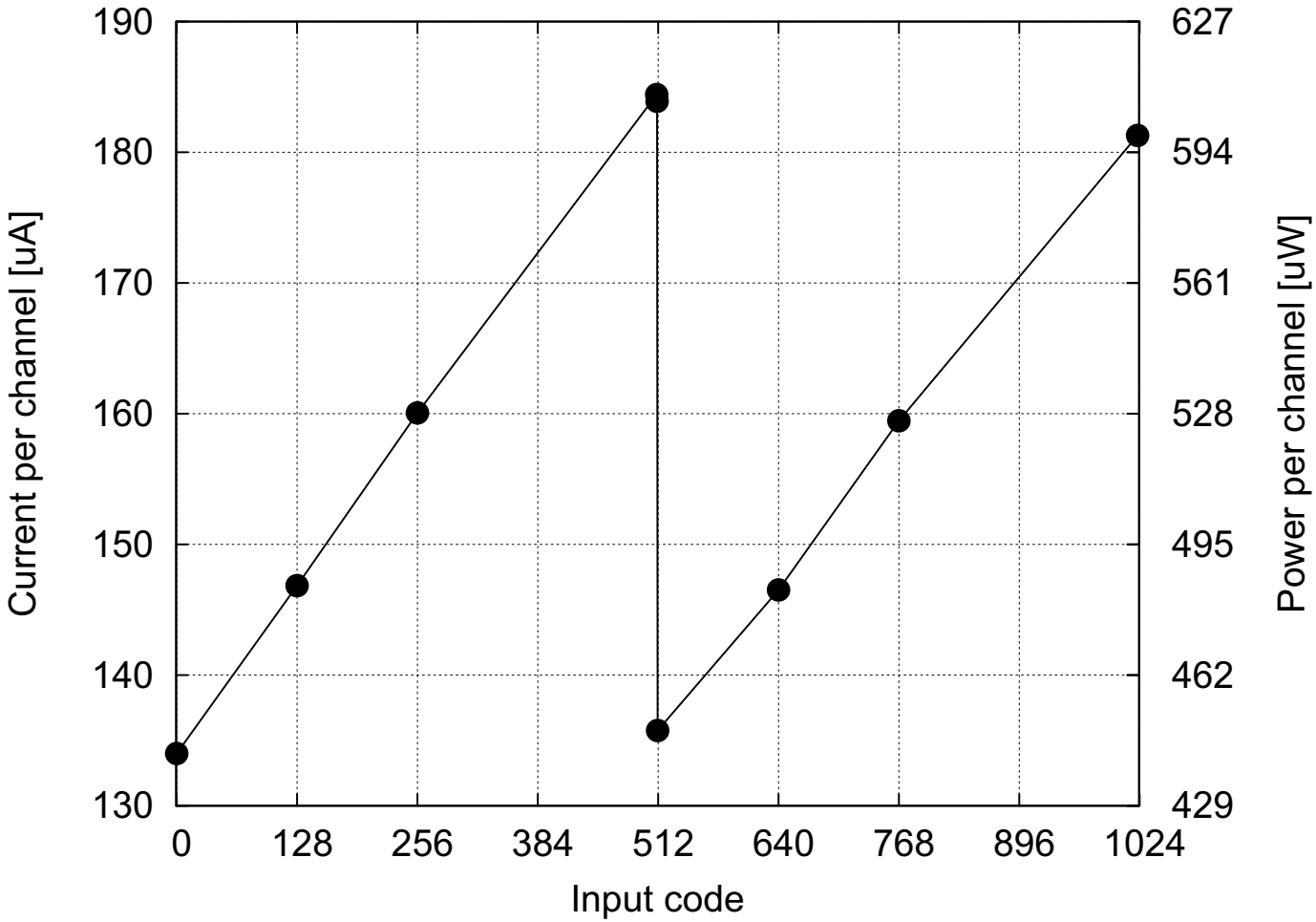
Static Measurements II.

1st chip	Channel no	1	2	3	4	5
	LSB value [mV]	2.62	2.59	2.62	2.64	2.68
	max. |INL| [LSB]	0.65	0.75	0.6	0.6	0.65
	max. |DNL| [LSB]	1.1	0.9	1.1	0.9	1.05
	Codes of |DNL| $>$ 0.5	13	17	14	8	26
	Nr of missing values	4	0	2	0	3
2nd chip	Channel no	1	2	3	4	5
	LSB value [mV]	2.58	2.59	2.62	2.61	2.63
	max. |INL| [LSB]	0.45	0.5	0.6	0.6	0.7
	max. |DNL| [LSB]	0.75	0.95	0.8	0.7	1.2
	Codes of |DNL| $>$ 0.5	15	2	29	22	20
	Nr of missing values	0	2	0	0	2

Outline

1^{st} Prototype Measurements Results

Power Measurements

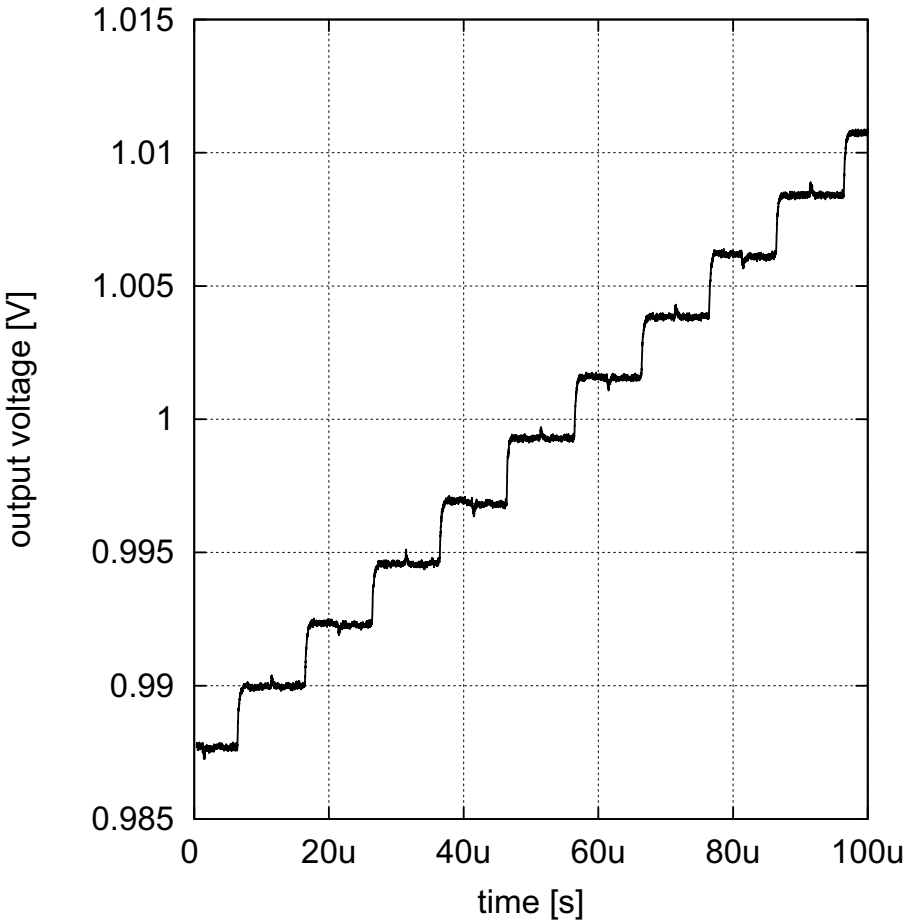


Relation between power consumption and DAC input code.

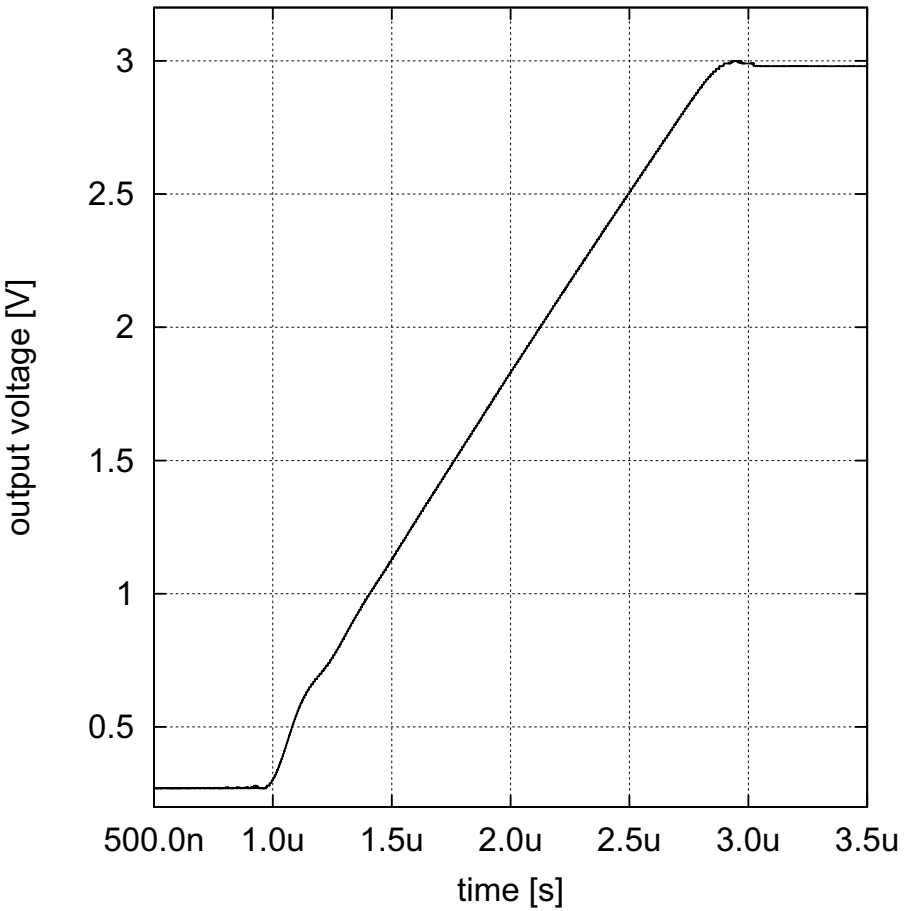
Outline

1^{st} Prototype Measurements Results

Transient Measurements.



Waveform showing 1 LSB steps.



Worst case settling time (between first and last input code).

Outline

Comparison with other low–power 10 bit DACs

	1	2	3	4	This work
architecture	current steering	R–2R ladder	resistor ladder	resistor string	current steering
technology	0.35 μm CMOS	0.18 μm CMOS	0.35 μm CMOS	0.13 μm CMOS	0.35 μm CMOS
power cons. [mW]	$\leq$ 7.8	4	0.07 (analog part)	0.5	$\leq$ 0.6
area [mm^2]	0.23	0.01	0.022	0.18	0.18
max INL [LSB]	0.2	0.75	0.7	2.0	0.6
max DNL [LSB]	0.2	0.7	0.35	0.5	0.8
speed	upd. rate 30 MS/s	low frequency	set. time 3 $\mu s/10pF$	upd. rate 2MS/s	worst t_{set} 2 μs 1 LSB t_r $<$ 500 ns
output type	current $\leq$2.5mA	current $<$2.2mA	voltage without buffer	voltage high–swing	voltage high–swing

1 M. Borremans, A. Van den Bosch, M. Steyeart, W. Sansen, *A low power 10–bit CMOS D/A converter for high speed applications*, IEEE 2001 custom integrated circuits conference.

2 B. Greenlay, R. Veith, Dong–Young Chang, Un–Ku Moon, *A low–voltage 10–bit CMOS DAC in 0.01–mm^2 die area*, IEEE Transactions on Circuits and Systems, vol. 52, no 5, 2005.

3 Y. Perelman, R. Ginosar, *A low–power inverted ladder D/A converter*, IEEE Transactions on Circuits and Systems, vol. 53, no 6, 2006.

4 F. Ge, M. Trivedi, B. Thomas, W. Jiang, H. Song, *1.5V 0.5mW 2MSPS 10B DAC with rail–to–rail output in 0.13μm CMOS technology*, SOC Conference, 2008 IEEE International.

Outline

Possible Improvements.

What is not good:

- DNL higher than expected (over 0.5 LSB).
  Some missing values.
- Asymmetry of rise time for outputs signals input code with MSB = 1 and MSB = 0.

Solutions:

- Layout of current source matrix to be improved.
- Large time constant of linear current mirror sink.

Possible Improvements.

What is not good:

- DNL higher than expected (over 0.5 LSB).
  Some missing values.
- Asymmetry of rise time for outputs signals input code with MSB = 1 and MSB = 0.

Solutions:

- Layout of current source matrix to be improved.
- Large time constant of linear current mirror sink.

Possible Improvements.

What is not good:

- DNL higher than expected (over 0.5 LSB).
  Some missing values.
- Asymmetry of rise time for outputs signals input code with MSB = 1 and MSB = 0.

Solutions:

- Layout of current source matrix to be improved.
- Large time constant of linear current mirror sink.

Outline

Design of 2^{nd} prototype – Improvements.

Circuit improvements:

- New layout of the current sources matrix.
- Small improvements in amplifiers design.
- Decreased dimensions of linear current mirror sink and adds trimming.

Parameters of amplifiers in 2^{nd} prototype:

	OTA N	OTA P	OP–AMP
Gain [dB]	96	93	136
GBW [Hz] (10pF load)	65k	130k	3M
PM [°] (10pF load)	96	90	70
Total power cons. [μW]	5	10	72.5

Design of 2^{nd} prototype – Improvements.

Circuit improvements:

- New layout of the current sources matrix.
- Small improvements in amplifiers design.
- Decreased dimensions of linear current mirror sink and adds trimming.

Parameters of amplifiers in 2^{nd} prototype:

	OTA N	OTA P	OP–AMP
Gain [dB]	96	93	136
GBW [Hz] (10pF load)	65k	130k	3M
PM [°] (10pF load)	96	90	70
Total power cons. [μW]	5	10	72.5

Design of 2^{nd} prototype – Improvements.

Circuit improvements:

- New layout of the current sources matrix.
- Small improvements in amplifiers design.
- Decreased dimensions of linear current mirror sink and adds trimming.

Parameters of amplifiers in 2^{nd} prototype:

	OTA N	OTA P	OP–AMP
Gain [dB]	96	93	136
GBW [Hz] (10pF load)	65k	130k	3M
PM [°] (10pF load)	96	90	70
Total power cons. [μW]	5	10	72.5

Design of 2^{nd} prototype – Improvements.

Circuit improvements:

- New layout of the current sources matrix.
- Small improvements in amplifiers design.
- Decreased dimensions of linear current mirror sink and adds trimming.

Parameters of amplifiers in 2^{nd} prototype:

	OTA N	OTA P	OP–AMP
Gain [dB]	96	93	136
GBW [Hz] (10pF load)	65k	130k	3M
PM [°] (10pF load)	96	90	70
Total power cons. [μW]	5	10	72.5

Design of 2^{nd} prototype – Improvements.

Circuit improvements:

- New layout of the current sources matrix.
- Small improvements in amplifiers design.
- Decreased dimensions of linear current mirror sink and adds trimming.

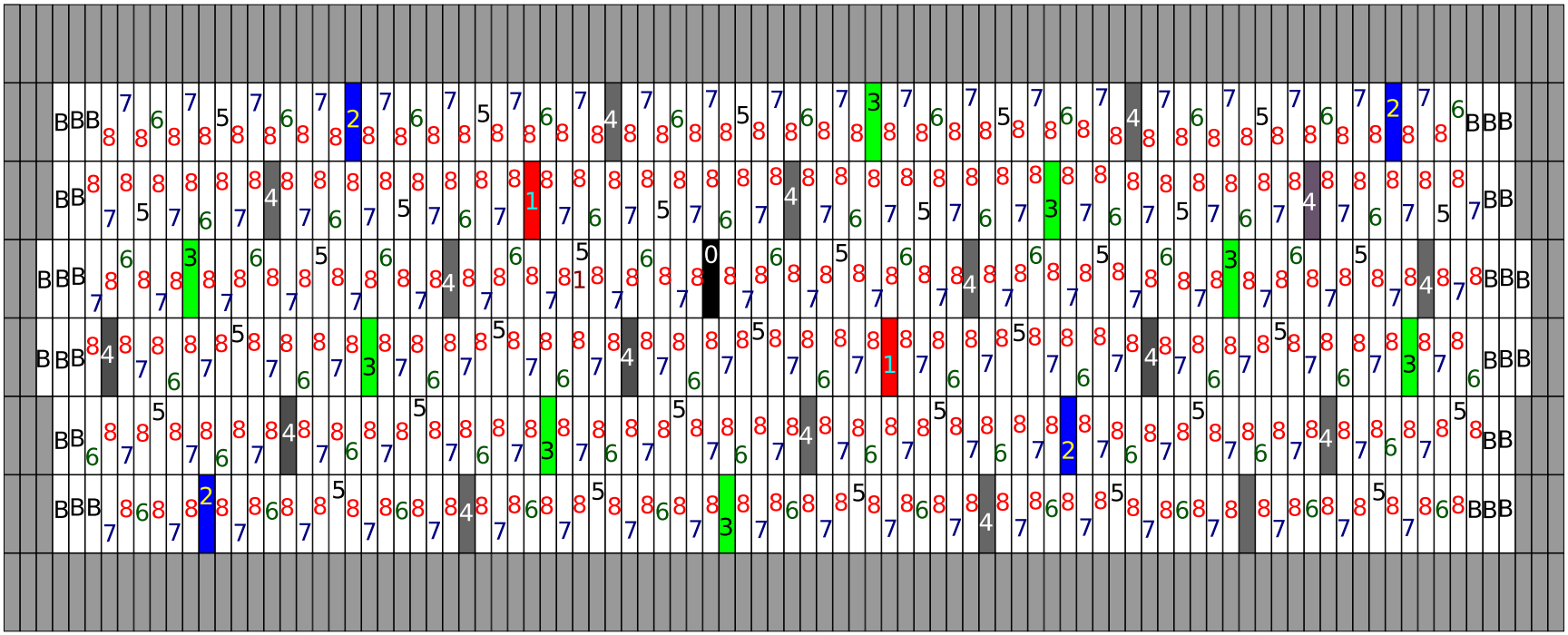
Parameters of amplifiers in 2^{nd} prototype:

	OTA N	OTA P	OP–AMP
Gain [dB]	96	93	136
GBW [Hz] (10pF load)	65k	130k	3M
PM [^{o}] (10pF load)	96	90	70
Total power cons. [μW]	5	10	72.5

Outline

Layout of 2^{nd} prototype – Improvements.

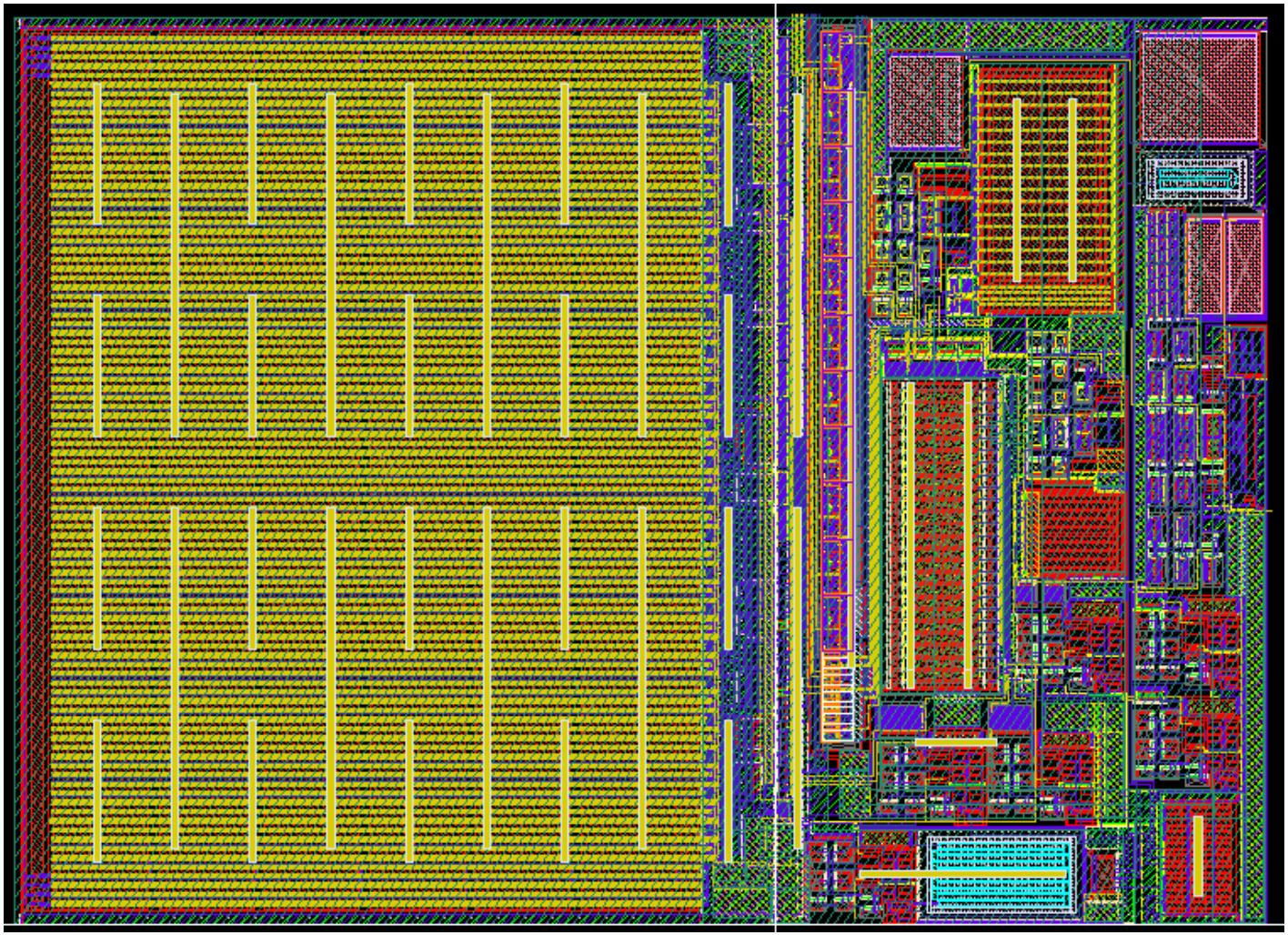
9 bit Current Sources Array.



Block Diagram of DAC Matrix Layout.

Layout of 2^{nd} prototype – Improvements.

DAC Core.



Layout of 2^{nd} prototype (385x530μm).

Summary

- 1^{st} prototype of 10 bit DAC is fully functional.
- Measurements results are generally in good agreement with simulations:
  - Transfer curve – LSB $\simeq$ 2.6 [mV]
  - Integral Non–Linearity (INL) $\simeq$ 0.6 [LSB]
  - Differential Non–Linearity (DNL) $\simeq$ 0.8 [LSB]
  - Full scale settling time = 2 [μs]
  - 1 LSB settling time $<$ 500 [ns].
- Differential non–linearity is slightly higher than expected – attributed to CS matrix layout.
- Improved design is completed and ready for submission.