Investigation of M – 2M and Exponential Digital–to–Analog Converters

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Outline

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8 bits M–2M DACs
Goals of Design

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- Static 8 bits DAC
- Low power consumption $<$ 100 μW
- Small core size $<$ 0.05 mm^2

Destination

Fine adjustment of voltages in every channel

Proposed architecture

M–2M Ladder

- Small number of elements (4N+1)
- Simple layout

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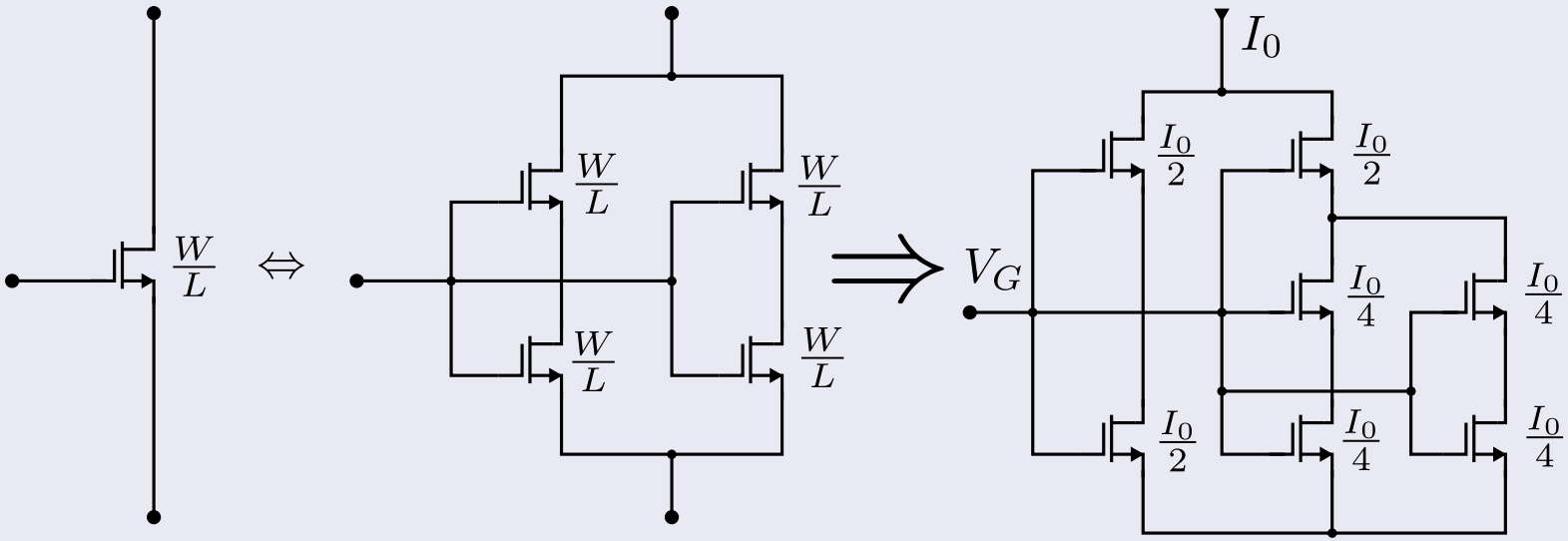
Principle of Operation

MOS transistor equivalent circuit



Current flowing into series–parallel identically designed transistors is equally divided between them

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Mismatch Consideration

Mismatch considerations

- Matching in saturation region is determined by overdrive voltage:

$$\sigma(I_d) = \sqrt{\frac{A_\beta^2}{W \cdot L} + \left(\frac{2 \cdot 100\% \cdot A_{V_{th}}}{V_{ov}}\right)^2 \cdot \frac{1}{W \cdot L}}$$

- Matching of MOS transistors in triode region is affected by output opamp offset:

$$\sigma(I_d) = \sqrt{\frac{A_\beta^2}{W \cdot L} + \left(\frac{100\% \cdot A_{V_{th}}}{V_{ov} - \frac{1}{2}V_{ds}}\right)^2 \cdot \frac{1}{W \cdot L} + \left(100\% \cdot \frac{\Delta V_{ds}}{V_{ds}}\right)^2}$$

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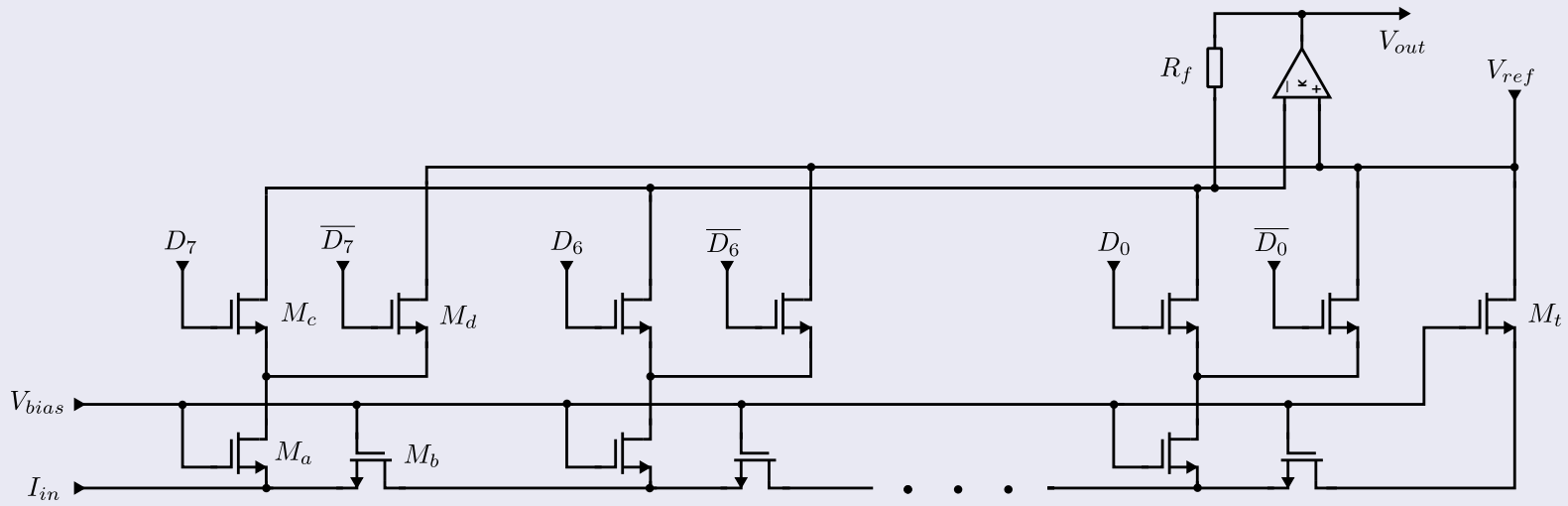
8 bits M–2M DACs
Implementation

Schematic diagram of proposed M–2M DAC



- Logic "1" must be equal V_{bias}
- Two modes of operation – current division ($I_{in} \neq 0$) or current source/sink ($I_{in} = 0$)
- Transistors can work in various regions of operation
- Simulations results required *special care* – problem with discontinuities of the BSIM transistors model.

8 bits M–2M DACs
Implementation

Nominal parameters

- $V_{LSB} = 0.5mV$
- $I_{LSB} = 25nA$ $(R_f = 20k\Omega)$
- $V_{bias} \simeq 1.2V$ $(NMOS)$ or $\simeq 1.45V$ $(PMOS)$
- $V_{ref} \in (1:2)V$
- $P_{ladder} \simeq 20\mu W$

Transistor dimensions

- NMOS Ladder:

$$\frac{W}{L} = \frac{5\mu}{25\mu}$$

- PMOS Ladder:

$$\frac{W}{L} = \frac{7.5\mu}{30\mu}$$

Outline

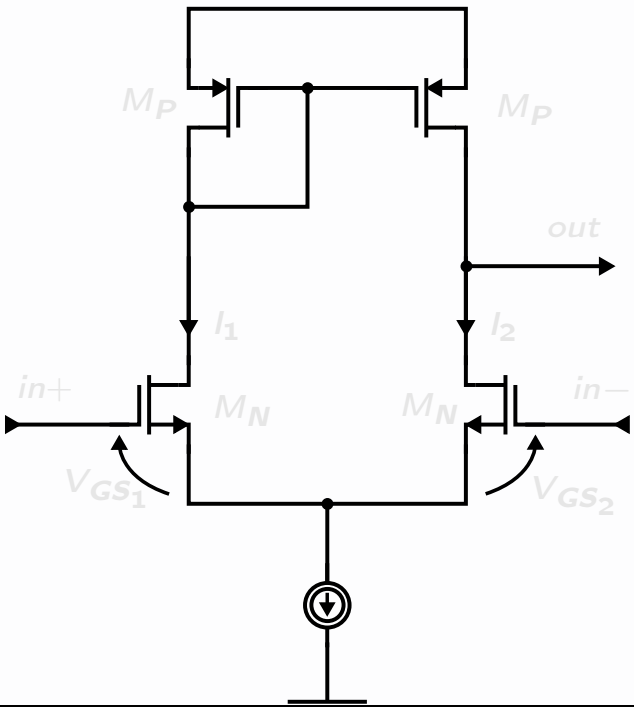
8 bits M–2M DACs

Design of Output OPAMP – assumptions

Design goals

- Low offset $<$ 5 mV – most important
- Low noise $<$ 0.2 mV
- Low power $<$ 50 μW
- Output current capability $>$ 100 μA

Low offset diff–amp design



$$V_{os} = V_{GS_1} - V_{GS_2} \approx \sqrt{\sigma^2_{V_{Th_N}} + \frac{I \cdot \sigma^2_{I_P}}{g_{m_N}} + \frac{V^2_{od_N} \cdot \sigma^2_{\beta_N}}{4}}$$

Conclusion:

Input pair transistors shuold have high W/L ration (high transconductance), however W/L ratio of loading transistors should be low (high overdrive voltage).

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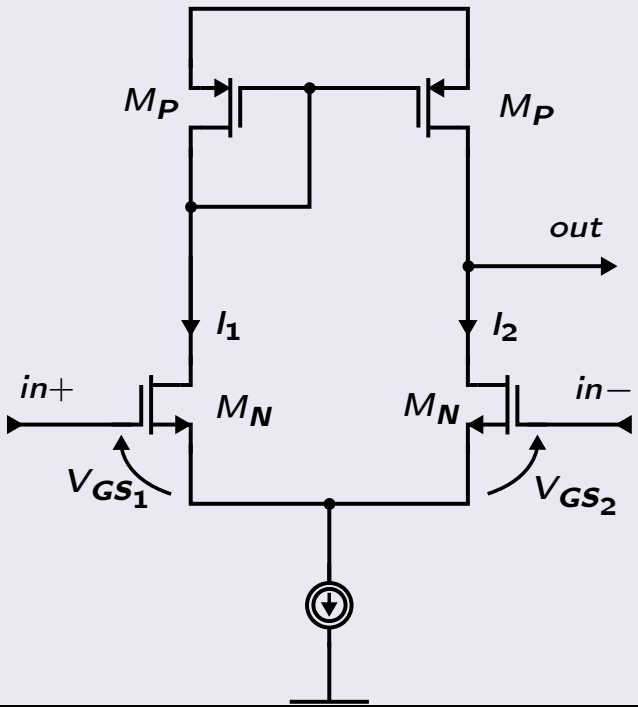

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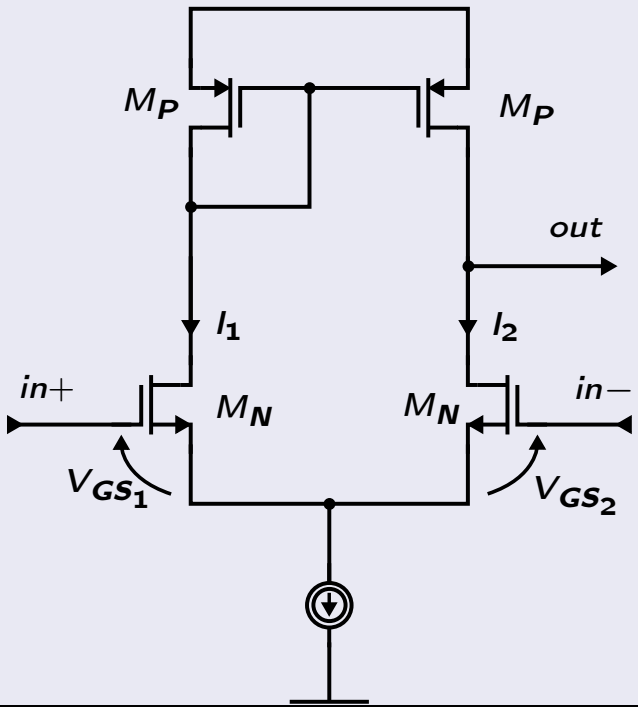

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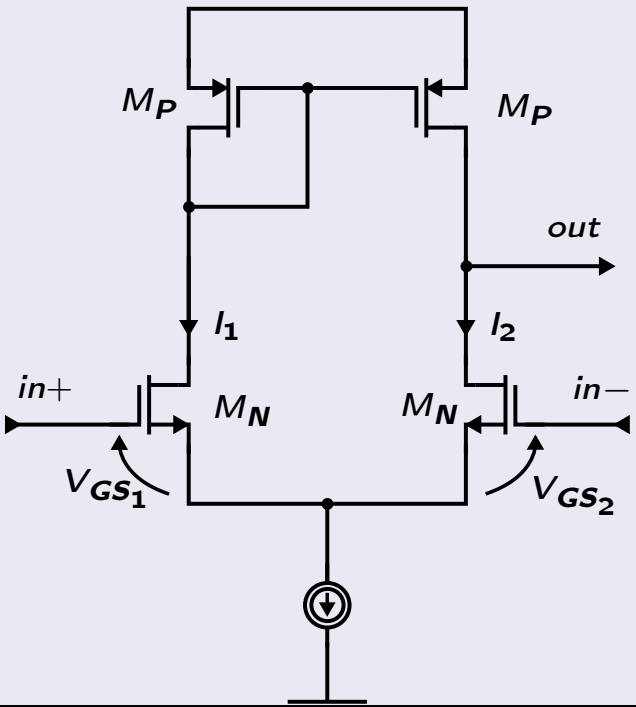

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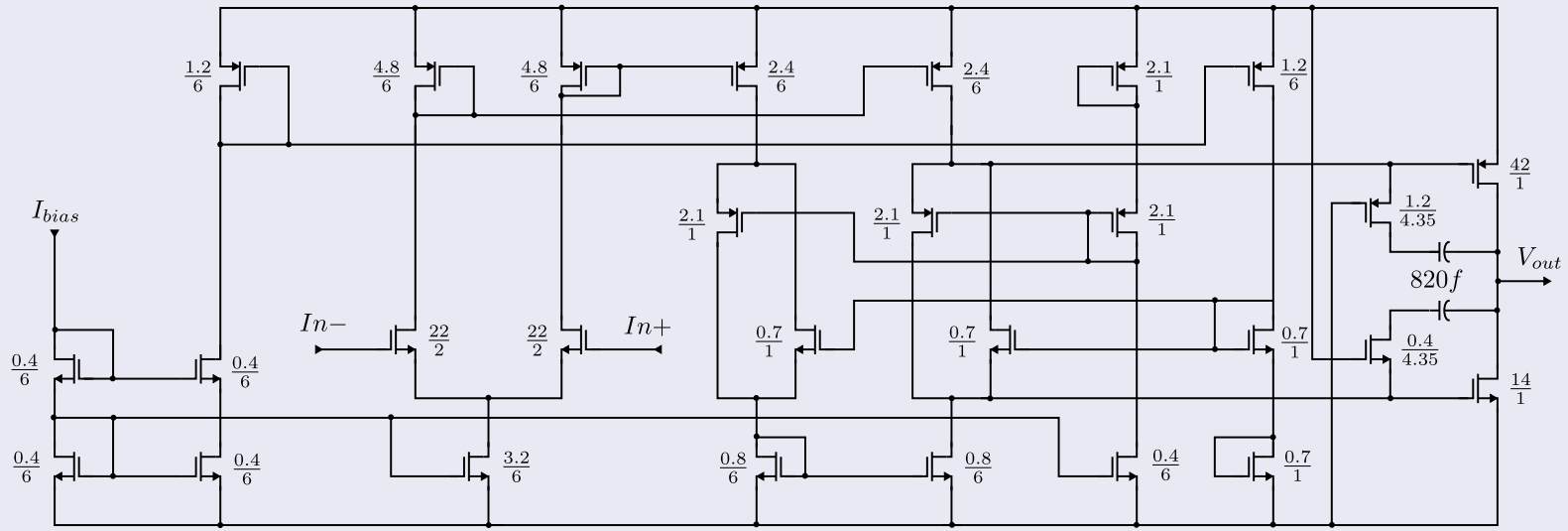
Design of Output OPAMP – implementation and results

Implementation



Simulation results

- Quiscent power = 60.6 μW ($I_{bias} = 500nA$)
- DC Gain (quiscent) = 108.8 dB
- Phase Margin (quiscent) = 72^o (10 pF load)
- Input offset (1σ) = 2 mV
- Noise rms = 105 μV (10 pF load)
- Gain Bandwitdh Product = 2.1 MHz (10 pF load)
- Output current capability = 4 mA

8 bits M–2M DACs

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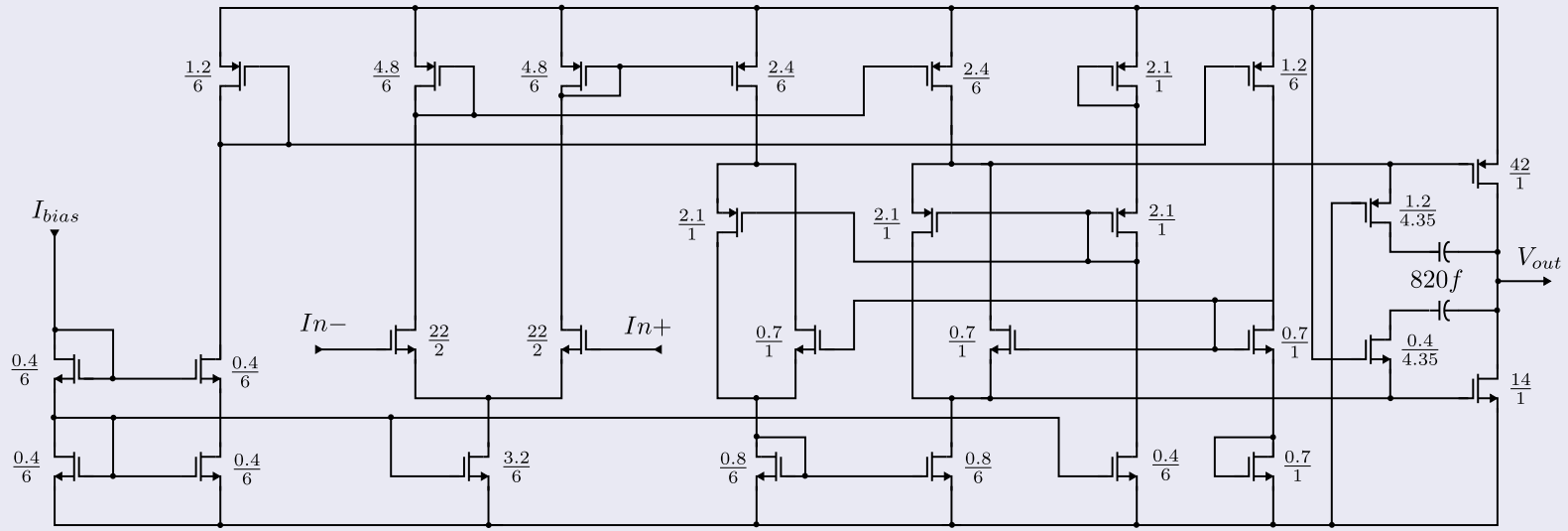

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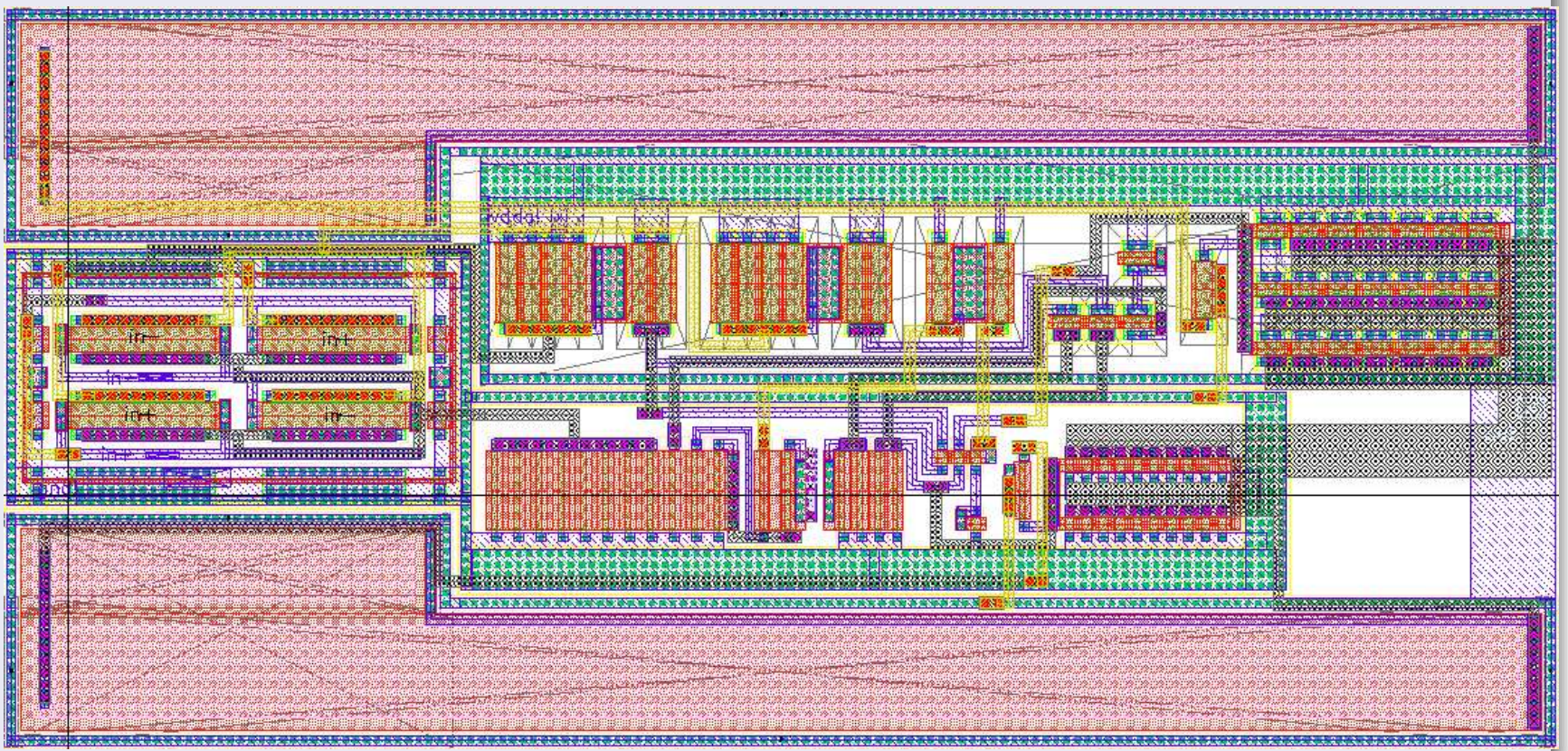
Design of Output OPAMP – layout

Layout – 119 $\times$ 57 μm^2

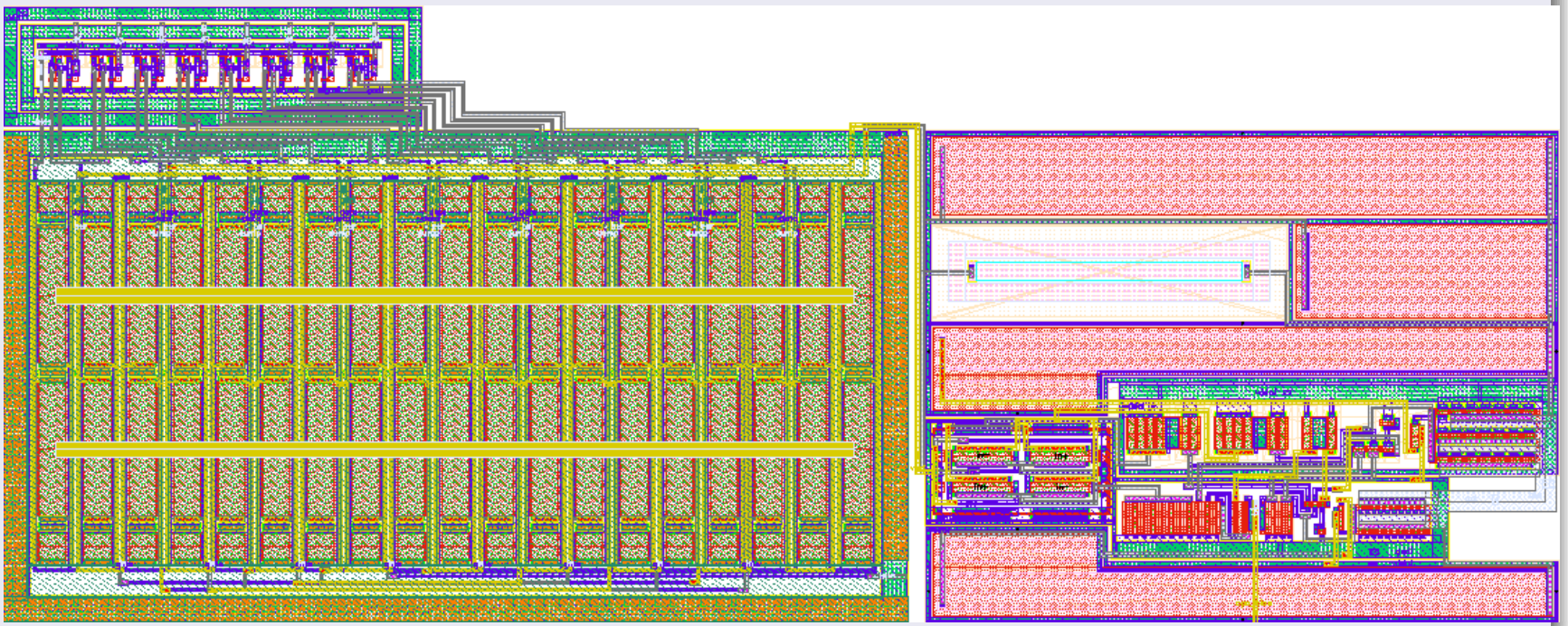


Outline

8 bits M–2M DACs

Layout

NMOS L–2L DAC – core area $= 295 \times 116 \mu m^2$



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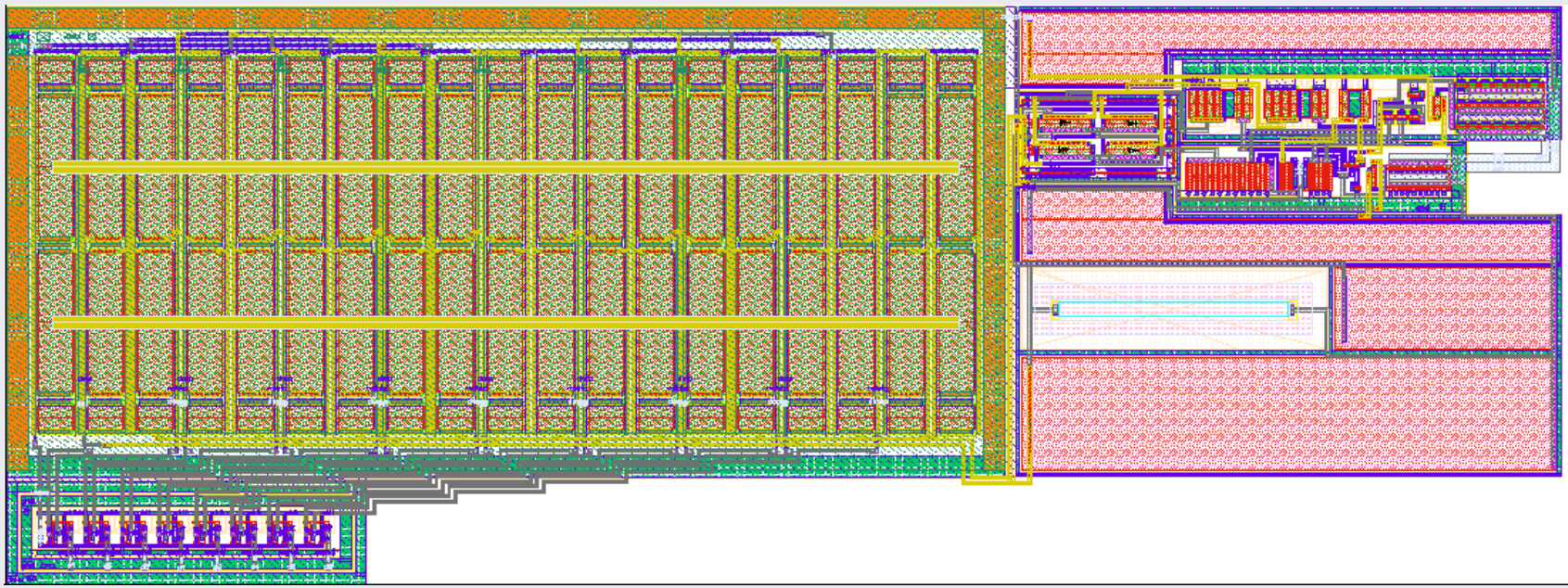
Layout

PMOS L–2L DAC – core area $= 340 \times 125 \mu m^2$



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Exponential 7–bit DAC

Idea of circuit

Goals of design

- Biasing DAC with a few orders of magnitude of output current (power scalling)
- Relatively low area and number of bits
- About 10 % of increment step

Proposition – exponential transfer function, with 8.5% increment and 7 bits resolution

Input	Output current $[I_{LSB}]$
0	1
1	1.09
...	...
15	3.58
16	3.90
...	...
127	48 776.31

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Exponential 7–bit DAC
Implementation

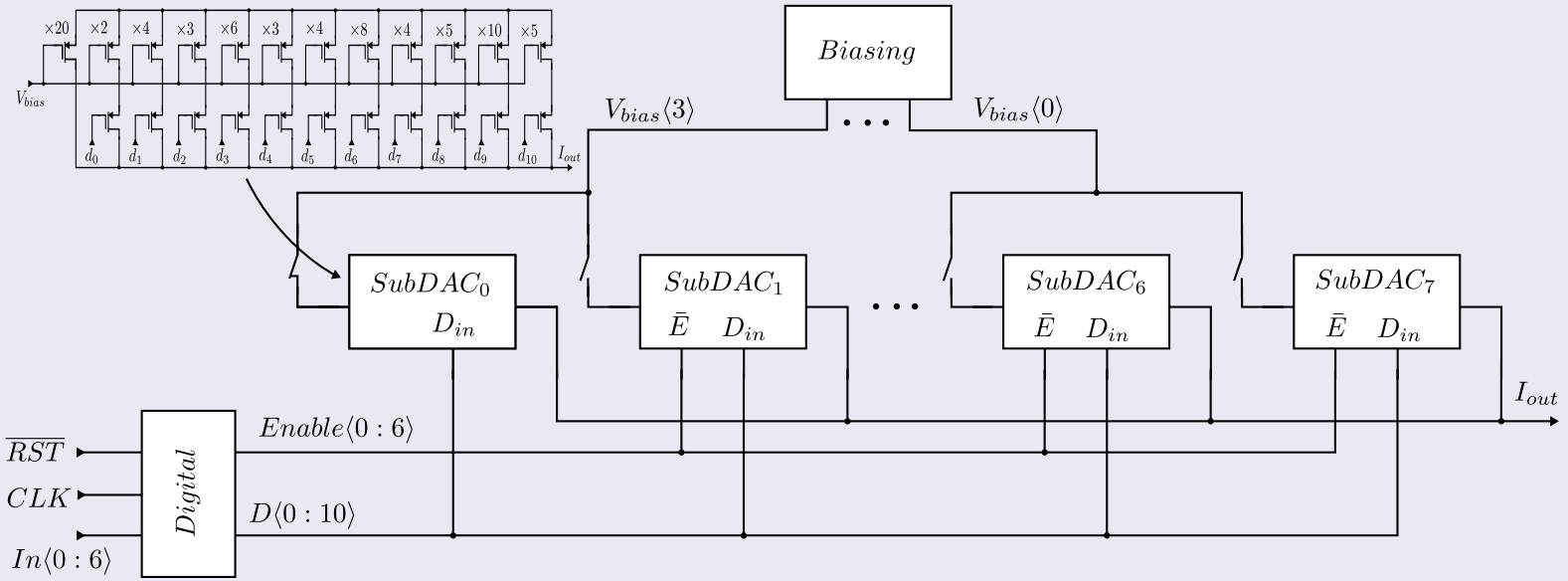
Solution – 8 4–bits subDACs

Input	Ideal weigths	Implemented weigths	Mismatch (%)
0	1	1	0
1	1.09	1.1	1.04
2	1.19	1.2	1.24
3	1.29	1.3	0.74
4	1.40	1.45	3.21
5	1.53	1.6	4.6
6	1.67	1.75	5.09
7	1.81	1.9	4.8
8	1.97	2.1	6.39
9	2.15	2.3	7.03
10	2.34	2.5	6.85
11	2.55	2.7	6
12	2.77	2.95	6.38
13	3.02	3.2	5.99
14	3.29	3.45	4.96
15	3.58	3.7	3.39
0 (next stage)	3.90	4	2.66

Outline

Exponential 7–bit DAC
Implementation

Block diagram of Exp–DAC



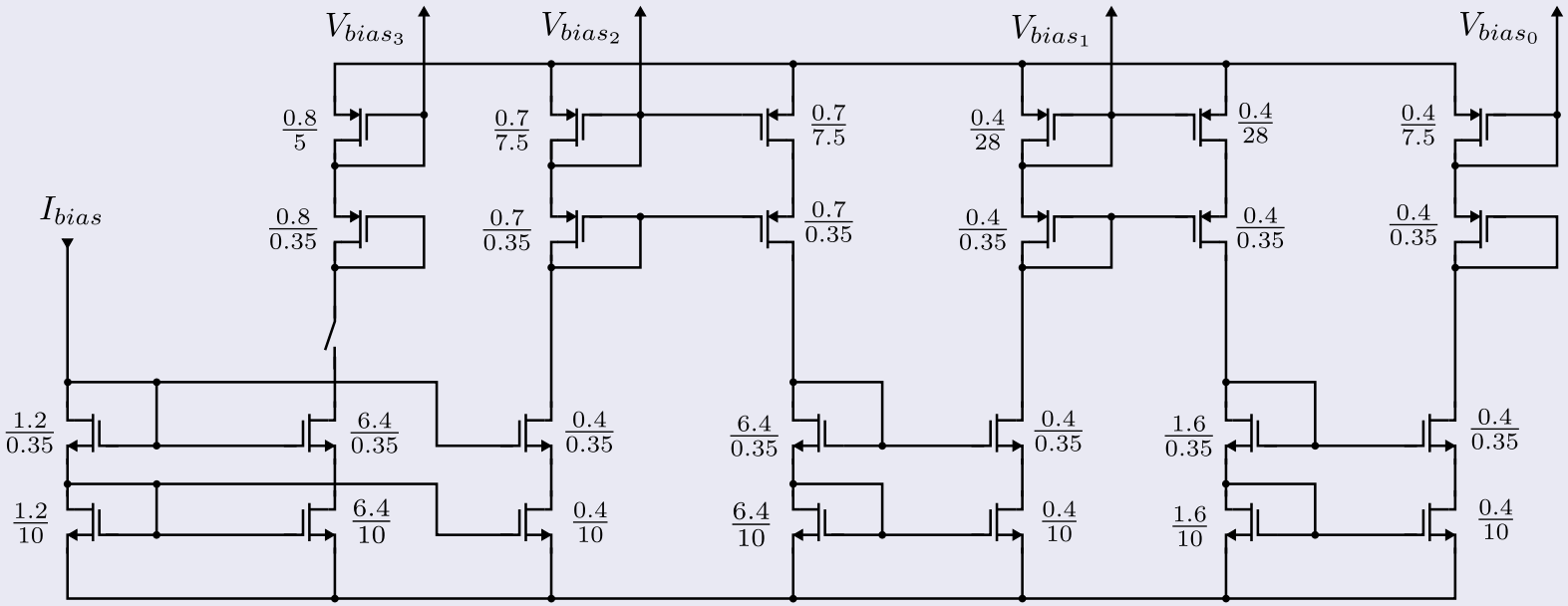
$\frac{W}{L}$ of $\frac{SubDAC_{n+1}}{SubDAC_n} = 4$ (with this same V_{bias})

Dimensions of SubDACs Current Sources

SubDAC No	0	1	2	3	4	5	6	7
Unit CS $\frac{W}{L}$	$\frac{0.4}{28}$	$\frac{0.4}{7.5}$	$\frac{0.4}{28}$	$\frac{0.4}{7}$	$\frac{0.7}{7.5}$	$\frac{1.4}{3.75}$	$\frac{0.8}{5}$	$\frac{1.6}{2.5}$

Exponential 7–bit DAC
Implementation

Schematic of biasing circuit



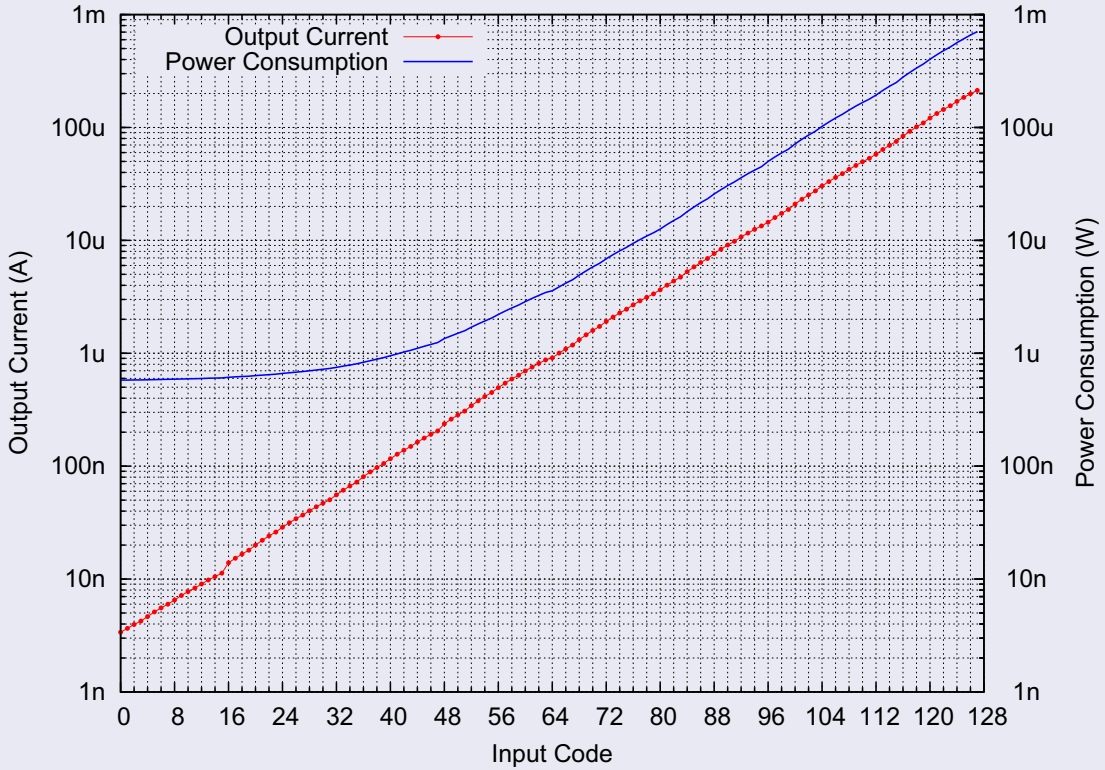
Branch	I_{bias}	V_{bias_3}	V_{bias_2}	V_{bias_1}	V_{bias_0}
Current	100 nA	533 nA	33.3 nA	2.1 nA	516 pA

Outline

Exponential 7–bit DAC

Simulation results – DC

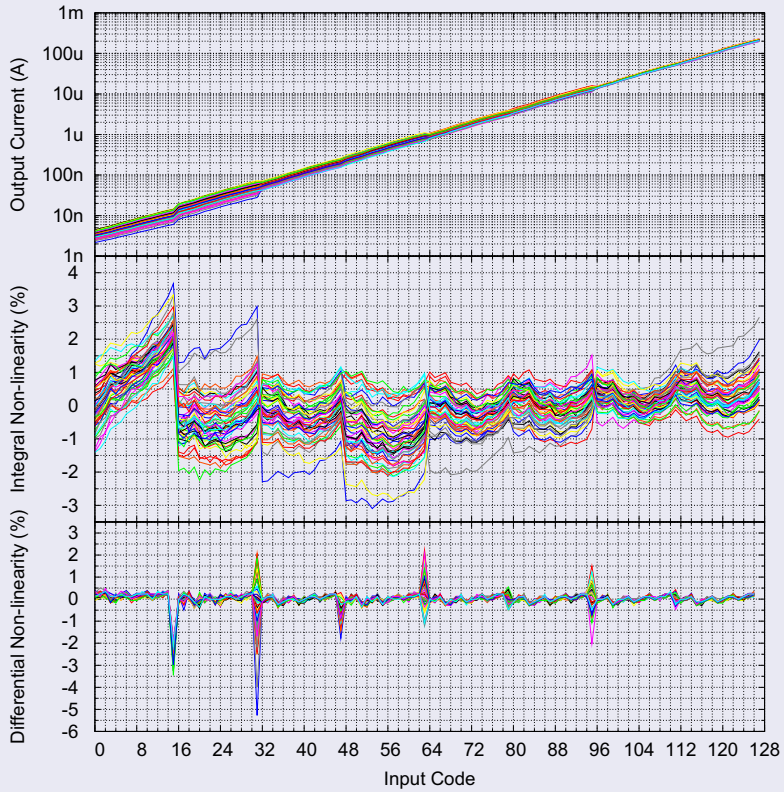
DC characteristic



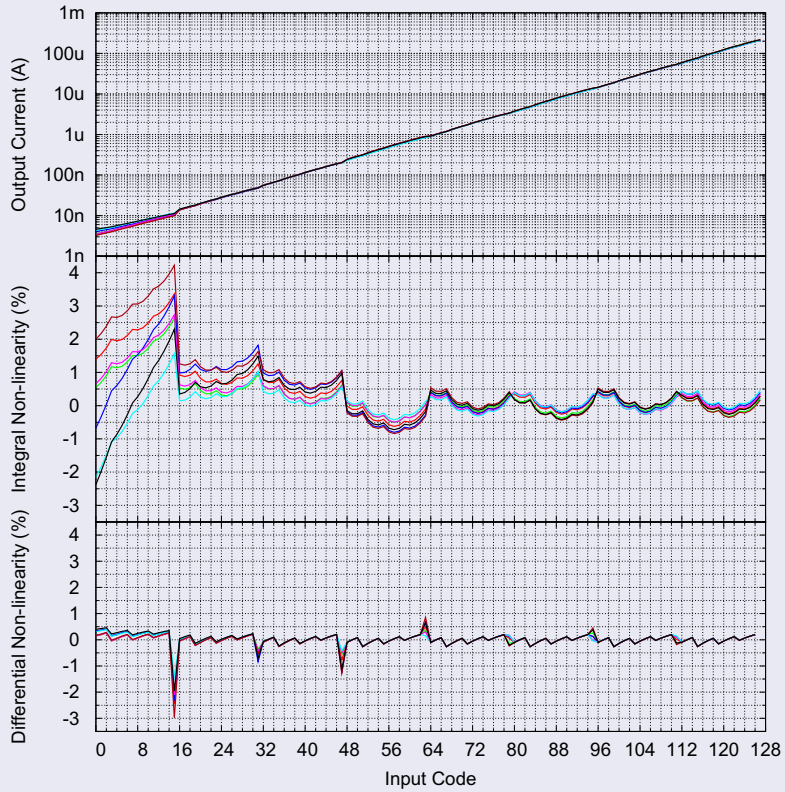
Exponential 7–bit DAC

Simulation results – Monte Carlo Worst Cases

Monte Carlo & Worst Cases



Monte Carlo



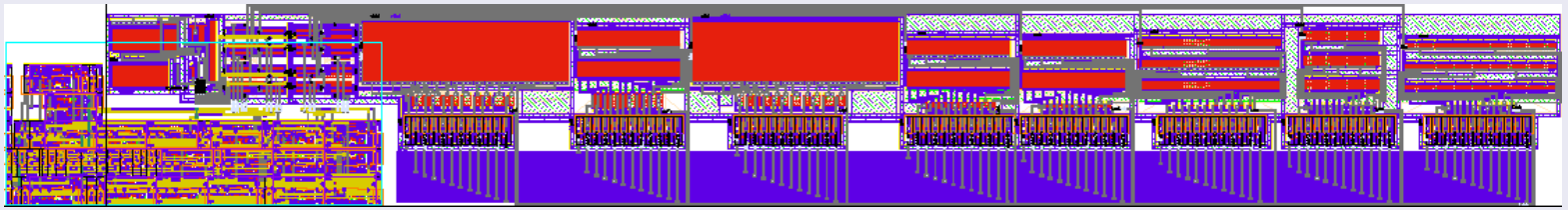
Worst Cases

Outline

Exponential 7–bit DAC

Layout

Core area $725 \times 93\ \mu m$



Conclusion

M–2M DAC

- M–2M ladder seems to be promising Low–power and Small-area DAC architecture.
- Offset of output OPAMP is main resolution limitation for ladder working in triode region.
- Simulation results should be done using EKV MOS model – usually not delivered with the technology.
- The measurements tell us the truth

Exp DAC

- The 7–bits DAC with exponential transfer function is designed.
- 5 order of magnitude of output current with similar area to linear DAC.
- Used as biasing circuit should be ideally for ASICs with aggressive power scalling.

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