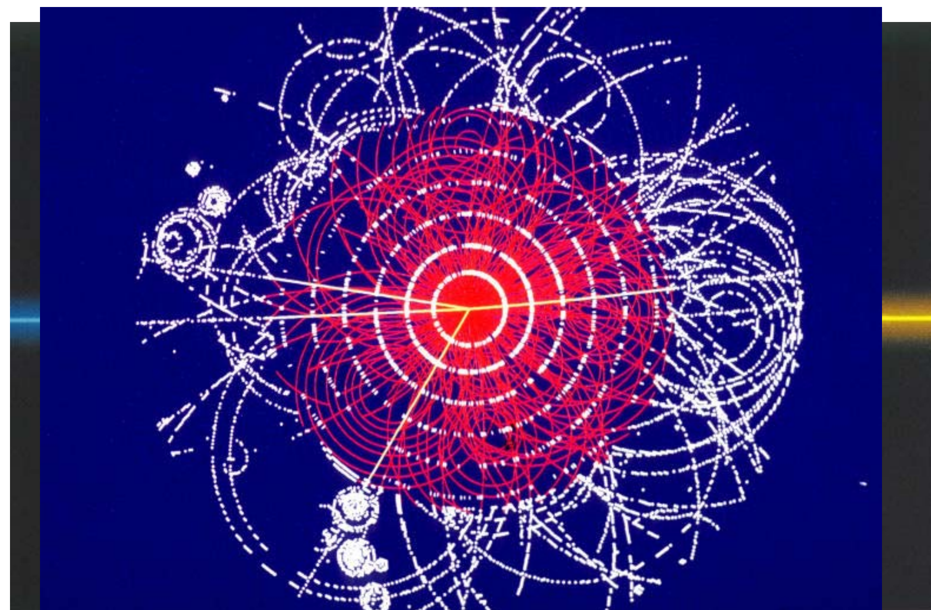
Pixel Detectors for Belle II

Course of Particle Physics & tracking in 2 slides

- e^+e^- , $p\bar{p}$: annihilation (disappearance)
- pp : destruction

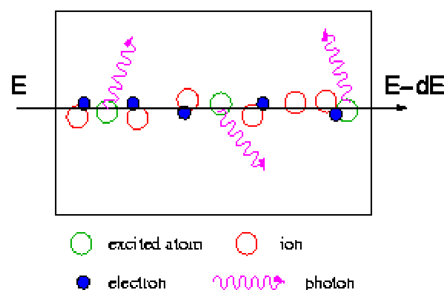
→other energetic particles created (secondaries), charged and neutral, some are short-lived (10^{-13} – 10^{-12} s): decay to another particles (vertex)

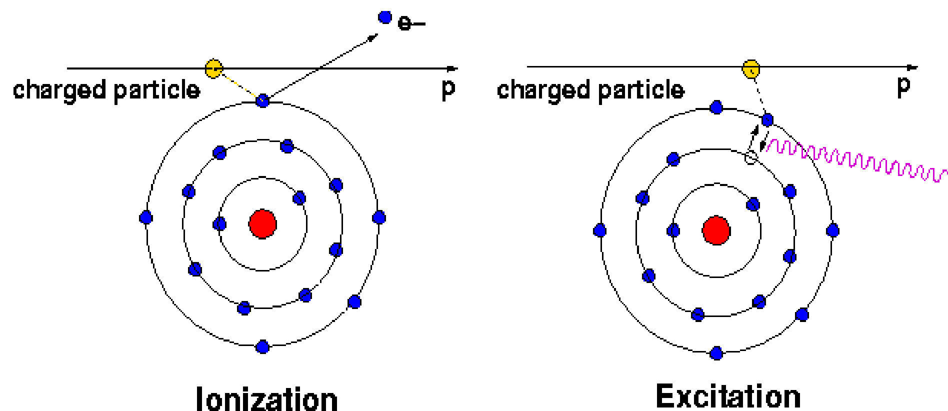


- particles: quantum-mechanical objects (not the balls), no way to see them with human senses (nor microscopes)

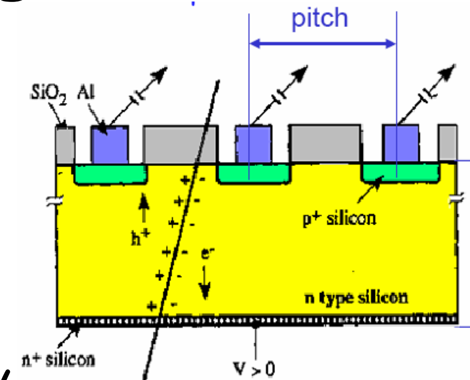
→ observe their trajectories via interactions with matter, e.g. charged particles: ionisation

Ionisation in
-Gas
-Solid state





Course of Particle Physics & tracking in 2 slides



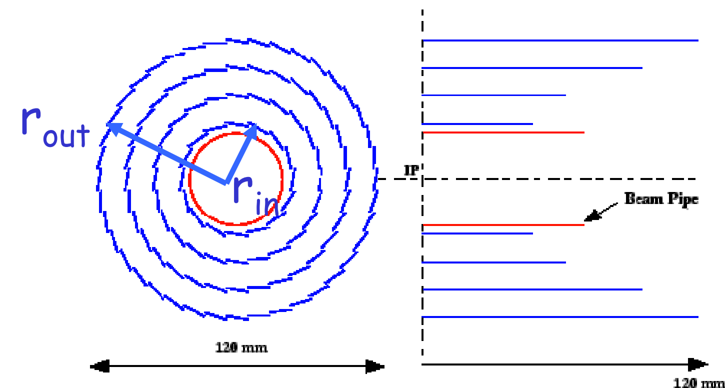
- Intrinsic precision depends on spacing (pitch) of charge collecting 'electrodes': $\sigma_{1p} \leq p/\sqrt{12}$
  → the smaller p the better (fine granulation is also essential at high track densities)

- Precision of the extrapolation of measured trajectory to the point of origin ('impact parameter resolution') approx.:

$$\sigma_b = \frac{\sigma_{in} r_{out}}{r_{out} - r_{in}} \oplus \frac{\sigma_{out} r_{in}}{r_{out} - r_{in}} \oplus \frac{0.014 r_{in}}{p\beta} \sqrt{\frac{X_r}{\sin^3\theta}},$$

~Z,ρ,d

collisions with nuclei



→ r_{in} the smaller the better,
however: severe machine backgrounds close to the beam pipe ('occupancy', radiation damage)

- At present Si detectors are by far the highest precision and radiation resistant trackers

Si:
small band-gap 1.12eV, E(e-h)=3.6eV
dE/dx(m.i.p.)=3.8MeV/cm <>=108e-h/μm
fast charge collection (<10ns)
Rigid structure, VLSI technology

Belle at KEKB

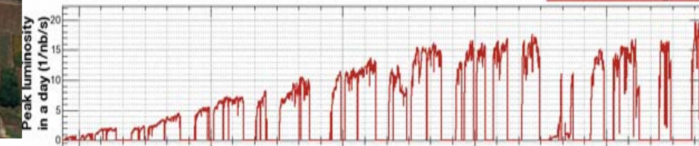
KEKB

Tokyo (40 mins by Tsukuba Exps)

HER: 8.0 GeV
LER: 3.5 GeV
crossing: 22 mrad

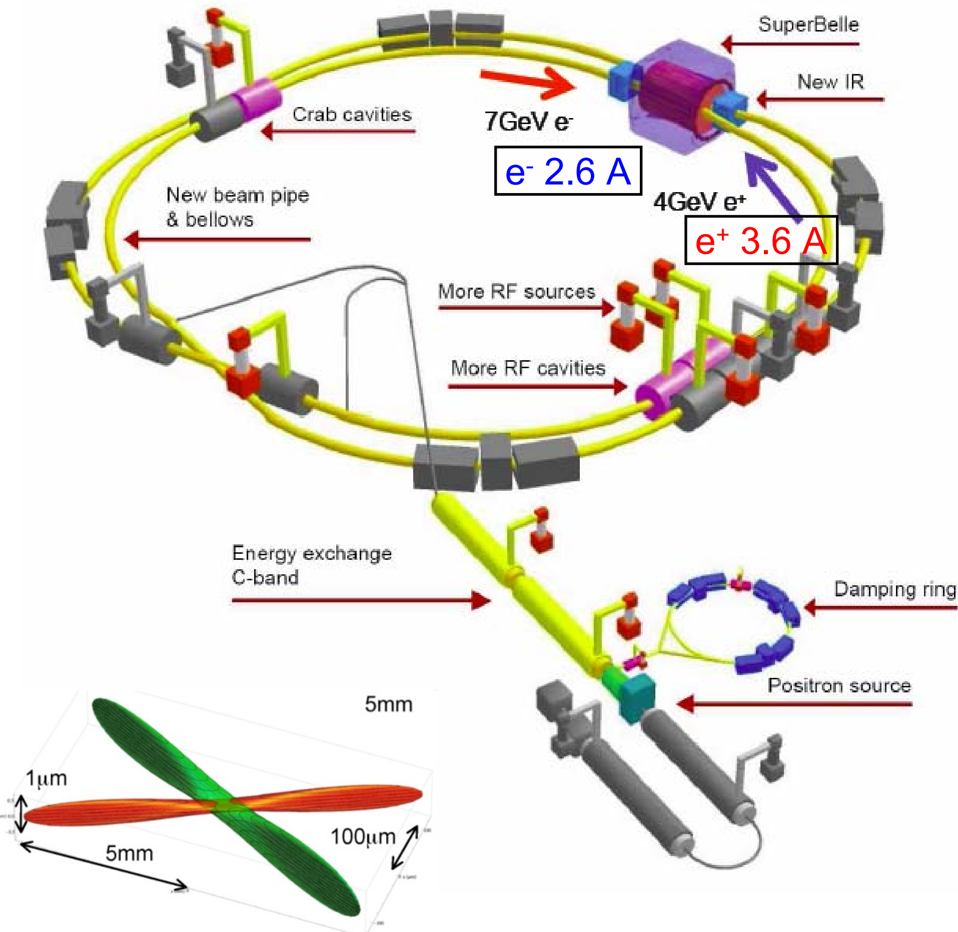
E_{CMS}=M(U(4S))
$\beta\gamma$=0.425
(low momenta phys.
<p>~1 GeV)

2009
$\int \mathbf{L}dt > 1000\ fb^{-1}$
1999



Belle II experiment specifics

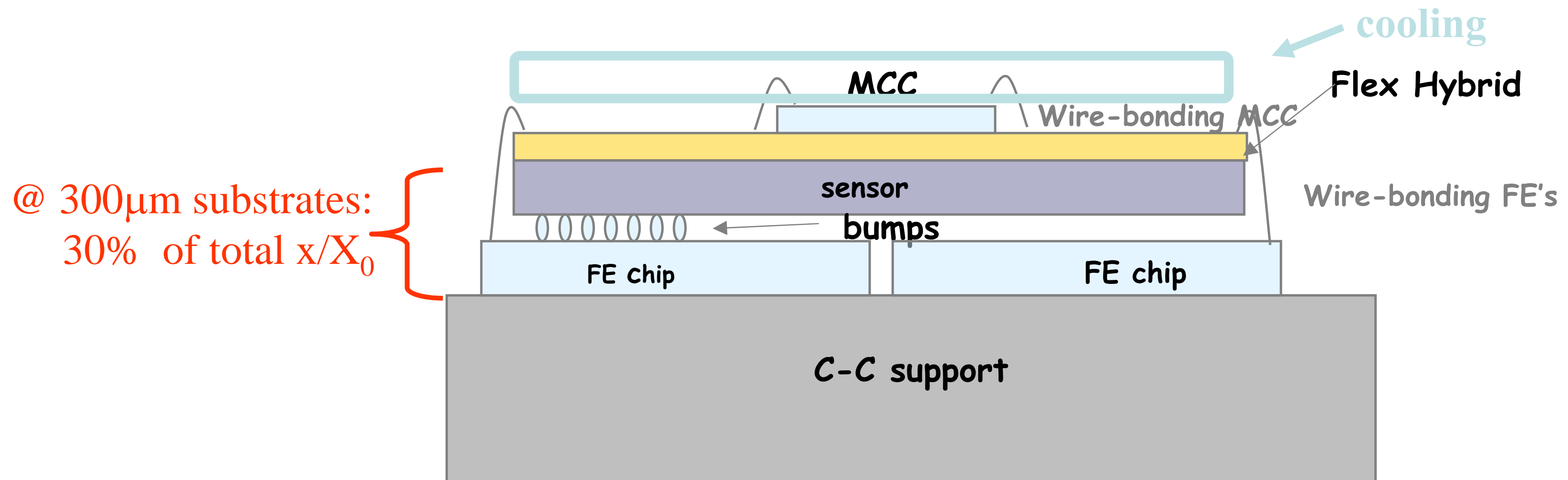
SuperKEKB



- Start 2014
- 'Nano-beam' σ_x~10μm,σ_y~60nm
- 40x higher luminosity (50 ab^{-1} by 2020)
- Continuous injection
- Beam pipe r=1cm
- Machine bkd 1-2MRad/y (edu. guess)
- NIEL ~ 10^{13}/cm^2/y

Hybrid Pixel Detectors

A mature technology (>15 yrs development), radiation resistant
pixel size limmited by RC-size & bonding pitch

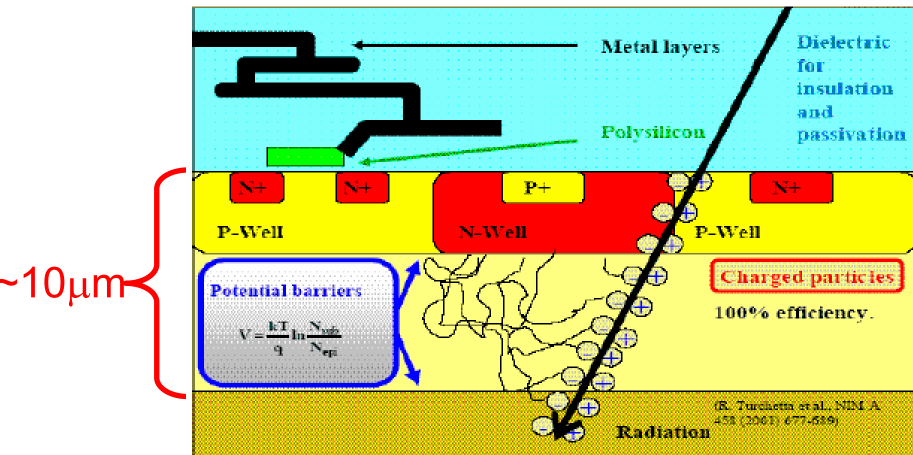


ATLAS: 300x50μm, 400x50μm, binary readout (migrated to DSM CMOS)
CMS: 150x150μm, analog readout (recently migrated to DSM CMOS)
ALICE: 425x50μm, binary readout

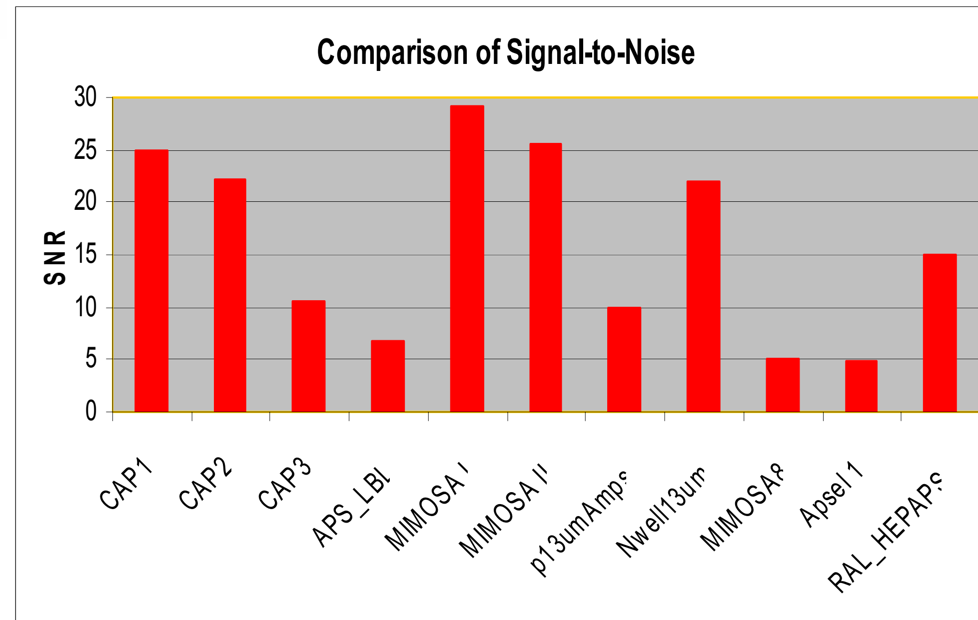
→ No use at B-Factory

CMOS Pixels

1999 (Turchetta), Dulinski (Strasbourg)
(follow-up of visible light imager



N-well/P-epi diode in epitaxial layer
Signal < 1000 e
Charge coll. to small diodes (3x3μm)
via diffusion (~100ns) (no depletion)
Readout: integrated NMOS transistors



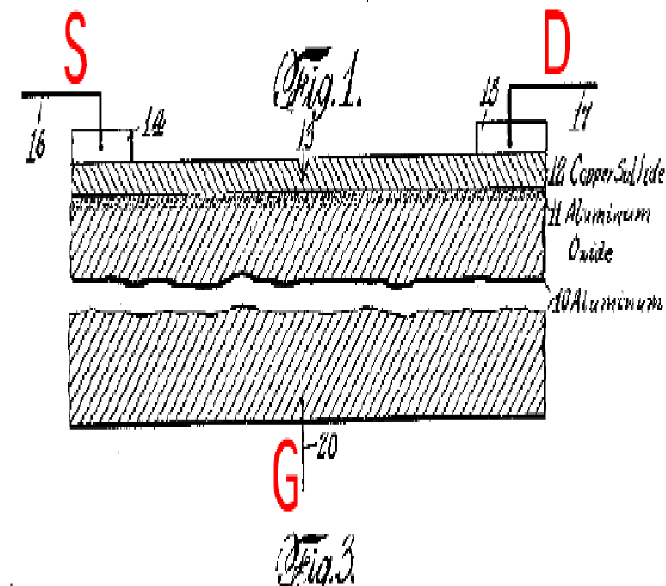
Belle prototyping (2004-08):
Too low S/N (falling with complexity
and chip size

SOI Pixels

SoI technology

J.E. Lilienfeld (1882-1963): Polish, born and educated in Lwów

- Structure:
  - Low-resistivity silicon layer (for MOSFET)
  - Burried oxide layer (BOX)
  - Silicon substrate (support wafer)
- MOS transistors are isolated from the silicon substrate and from each other.
  - Faster operation: Low stray capacitance
  - Latch up free.
  - Rate of "*single event*" effect is reduced.
- Becoming a standard technology in industry.


UNITED STATES PATENT

March 7, 1933. J. E. LILIENFELD 1,900,018

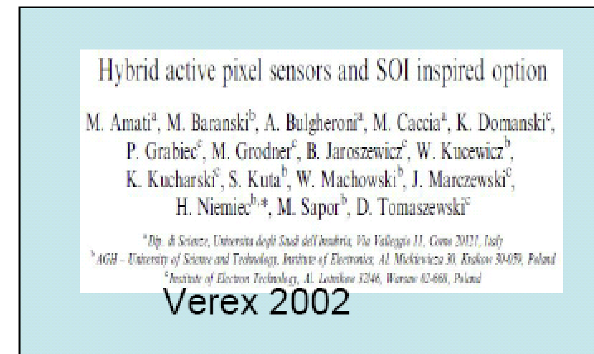
DEVICE FOR CONTROLLING ELECTRIC CURRENT

Filed March 28, 1928 3 Sheets-Sheet 1

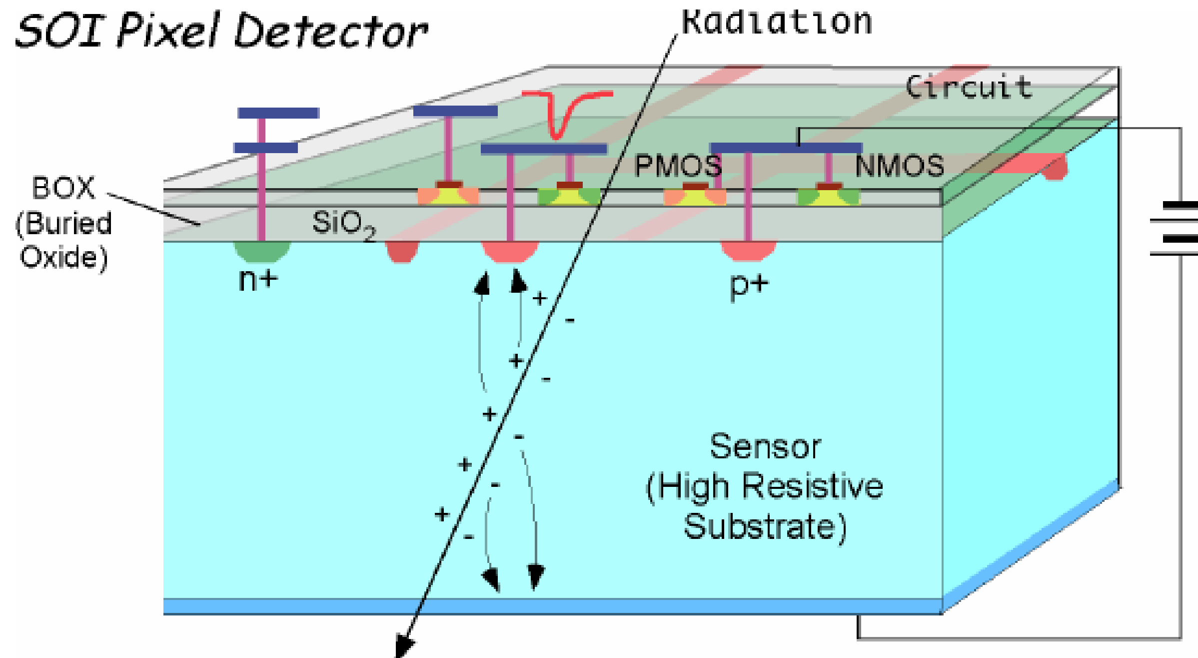
SoI Pixel sensor

Predecessor

- SOI based monolithic pixel sensor
  - High-resistivity (any) silicon can be used as the support silicon.
  - The signal induced in the support silicon is read out by the readout circuit above the BOX.
  - Thicker depletion region than MAPS.



SOI Pixels



Belle R&D since 2006 (OKI Semiconductor Ltd)

PD-SOI vs. FD-SOI

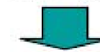
PD-SOI (Partially Depleted)

- ◆Thick SOI thickness (T_{SOI}) ~100-200nm
- ◆Depletion layer < T_{SOI}

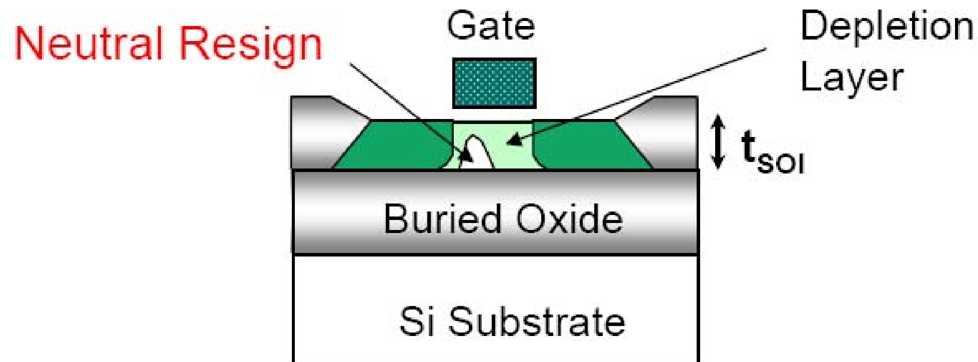
- ◇Large floating body effect
- ◇High drive Current by kink effect
  → High speed application

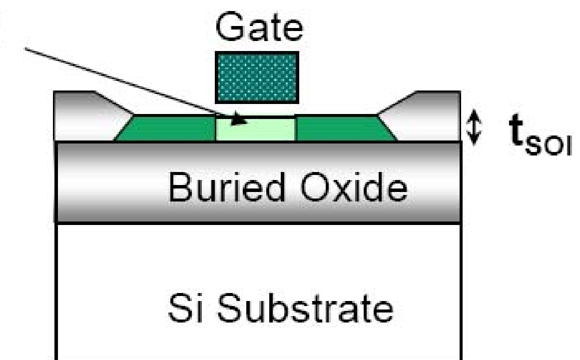
FD-SOI (Fully Depleted)

- ◆Thin SOI thickness (T_{SOI}) < 50nm
- ◆ Depletion layer > T_{SOI}



- ◇Less floating body effect
- ◇Steep subthreshold slopes
  → Low power application





FD-SOI has advantage in performance under very low voltage operation.

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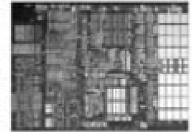
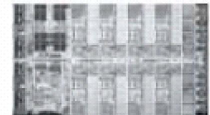
OKI Open up your dreams

Current Status of PD-SOI and FD-SOI



- **PD-SOI (Partially Depleted)**
  High-speed microprocessors
  - IBM: PowerPC , mainframe CPU's, Wii(Nintendo), Xbox
  - Free scale: PowerPC
  - AMD: Athlon processors
  - Sony (with IBM and Toshiba) : Cell, PS3



- **FD-SOI (Fully Depleted)**
  Low-power application
  - Oki: solar cell watch, long-wave RF decoder

Technology Node option beyond 32nm, Next 3D Tr. (R&D)
- Intel, many major companies

At present, only Oki has an experience of mass production of FD-SOI

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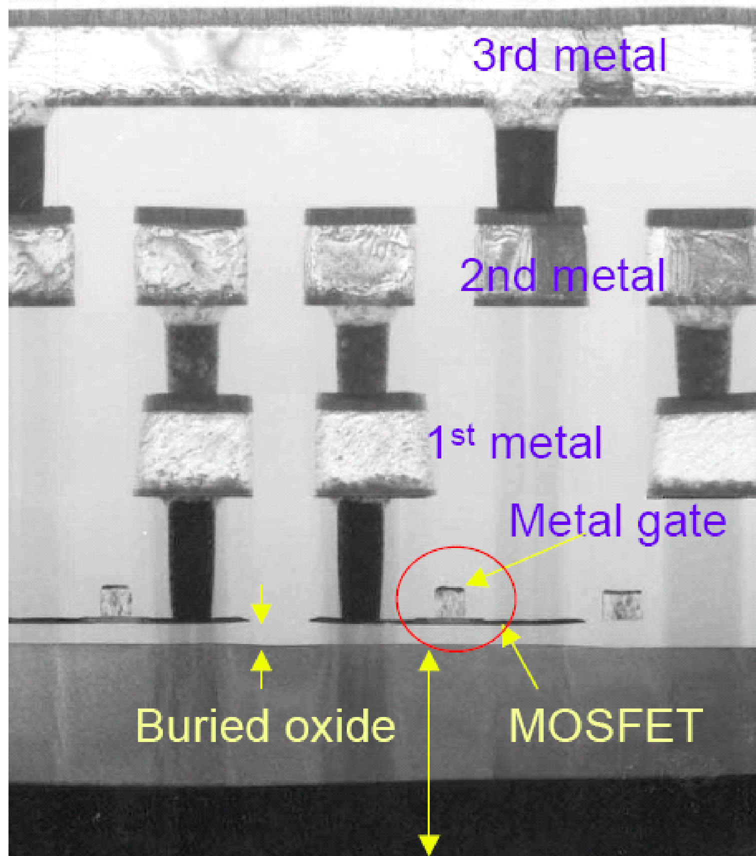
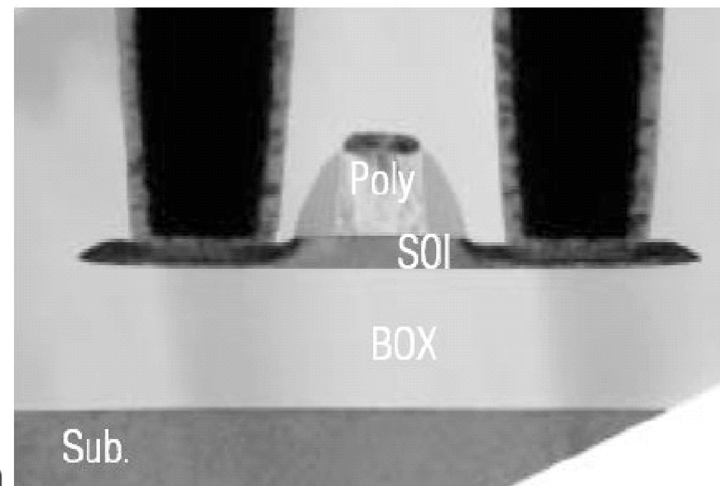
OKI SoI process



http://www.okisemi.com/english/soi.htm

0.20µm

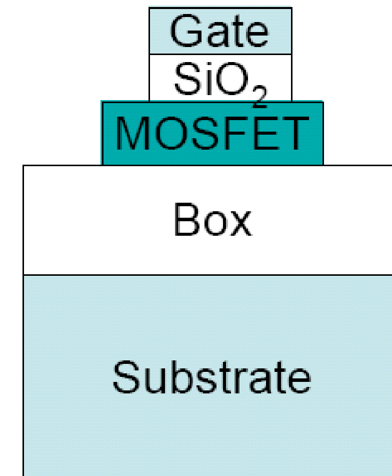
Process	~~0.15µm~~ Fully-Depleted SOI CMOS process, 1 Poly, 5 Metal layers, MIM capacitor
SOI wafer (SOITEC)	Wafer Diameter: 150 mmϕ, Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz>1k Ω-cm, 650 µm thick
Backside	Thinned to 350 µm, plated with Al (200 nm).



SOI: first lesson

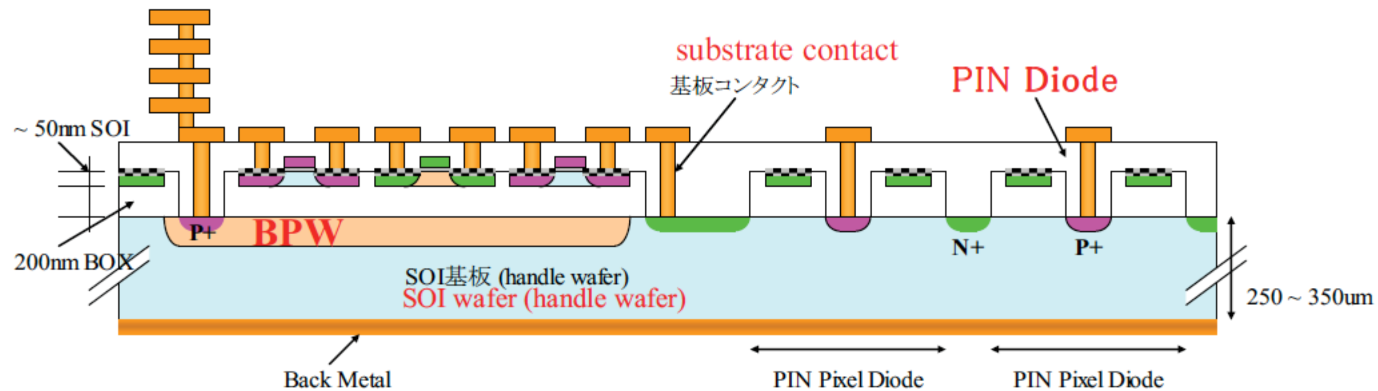
Back gate voltage effect

- Usually, 150nm bulk CMOS are rad-hard.
- SoI: BOX (200 nm SiO_2) below transistors
  - The increase of fixed charge in BOX shifts the transistor threshold.
- The potential of support wafer also causes threshold shift.



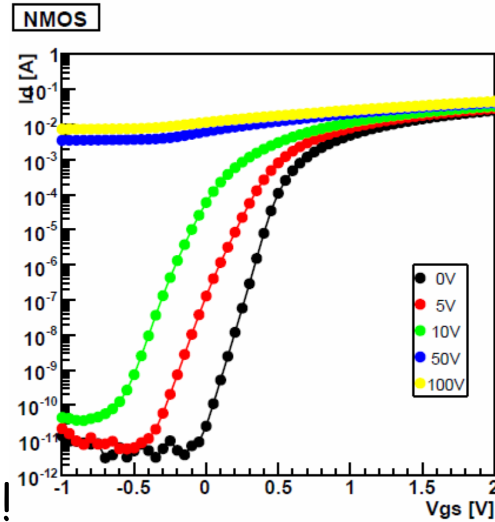
SOI - 2009 run

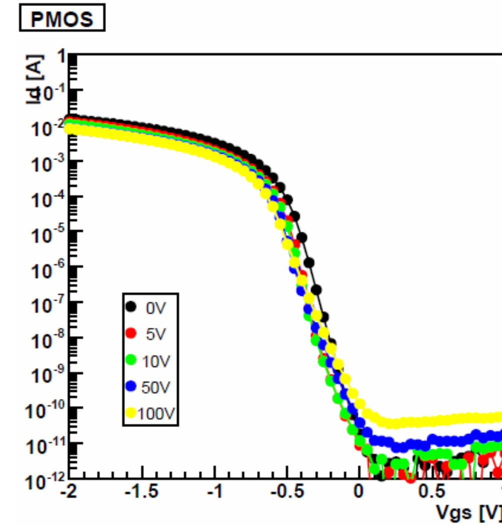
Burried p-well as the remedy for the back-gate effect:

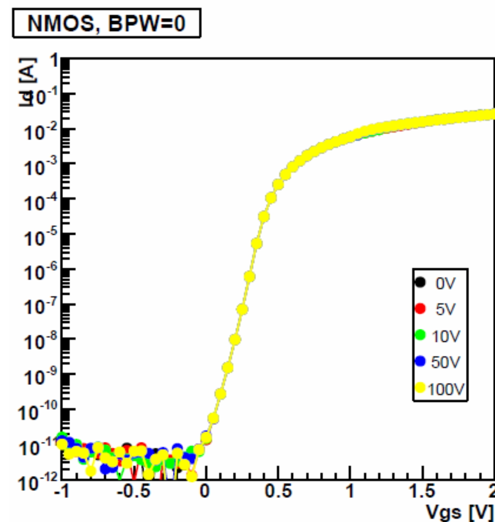


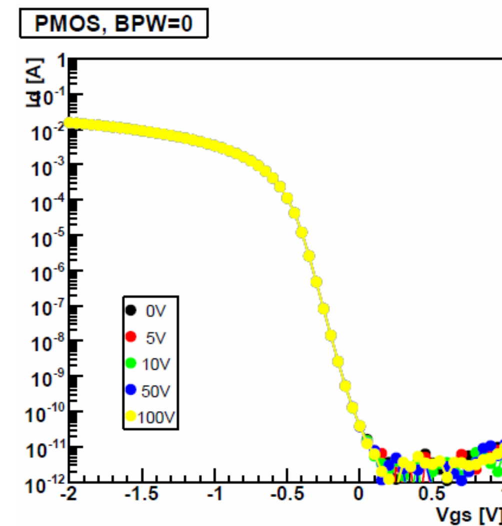
SOI: BPW applied- transistor characteristics

Back gate effect removed! Down to 100V depletion Voltage.
Real breakthrough!



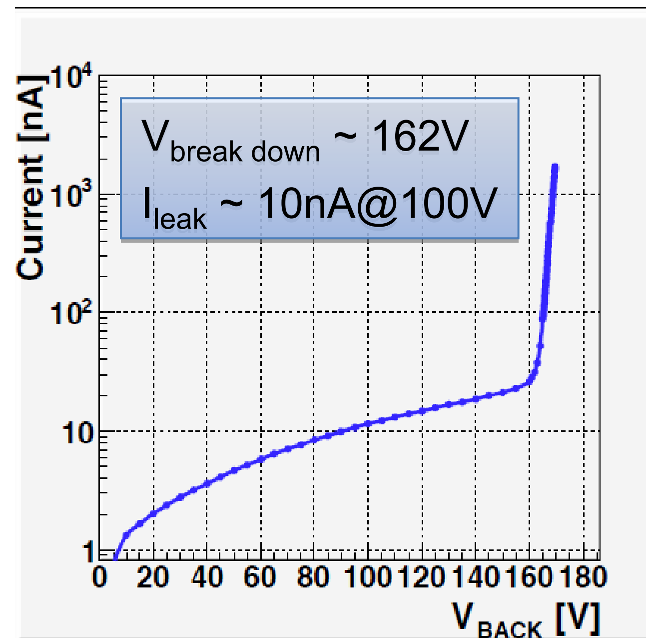


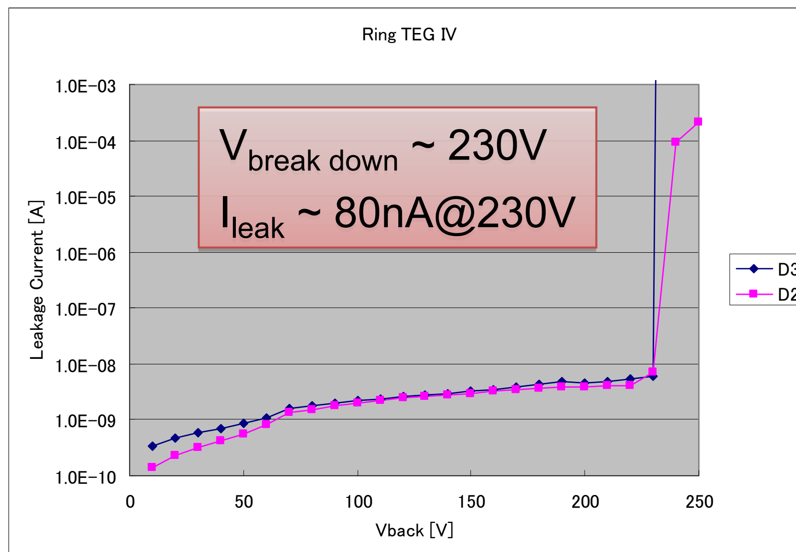




SOI with BPW

INTPIX3 (2.5 x 2.5mm)
Breaks down at > 160 V





Some TEG's even higher !

SOI pixels status

- Implementation of the BPW makes the device promising again

- The detector is ready for X-ray detection applications
  Needs more studies to fully asses its use for charged particles detection
  Radiation hardness to be studied
  Smarter redout electronics to be done
  New development: 3D LSI (vertical integration) just started

- Probably > 3 years R&D to have a mature device

DEPFET

Each pixel is a p-channel FET on a completely depleted bulk

A deep n-implant creates a potential minimum for electrons under the gate ("internal gate")

Signal electrons accumulate in the internal gate and modulate the transistor current (g_q ~ 400 pA/e$^-$)

Accumulated charge can be removed by a clear contact ("reset")

Fully depleted:
⇒large signal, fast signal collection

Low capacitance, internal ampl.:
=> low noise (40e-), can be thin

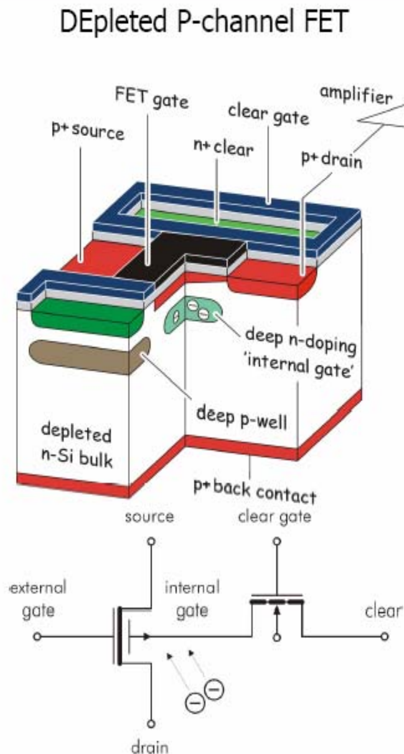
Transistor on only during readout:
=> low power

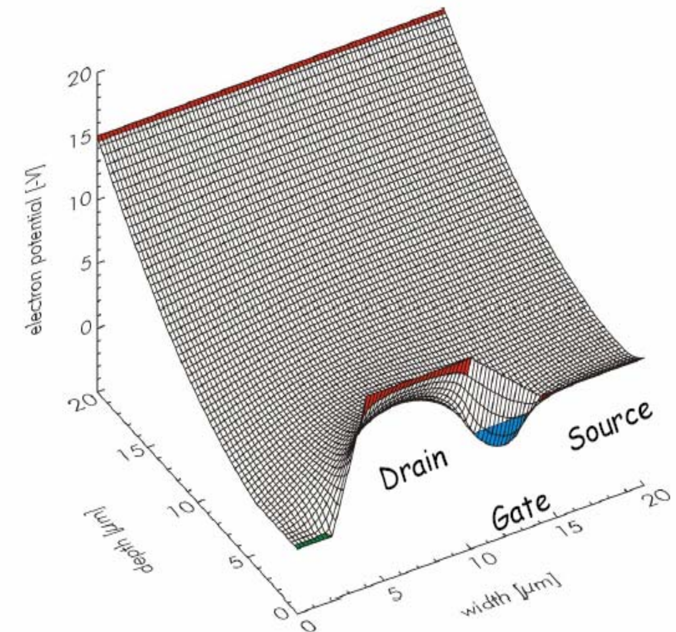
Complete clear:
=> no reset noise

DEPFET Principle

J. Kemmer & G. Lutz, 1987

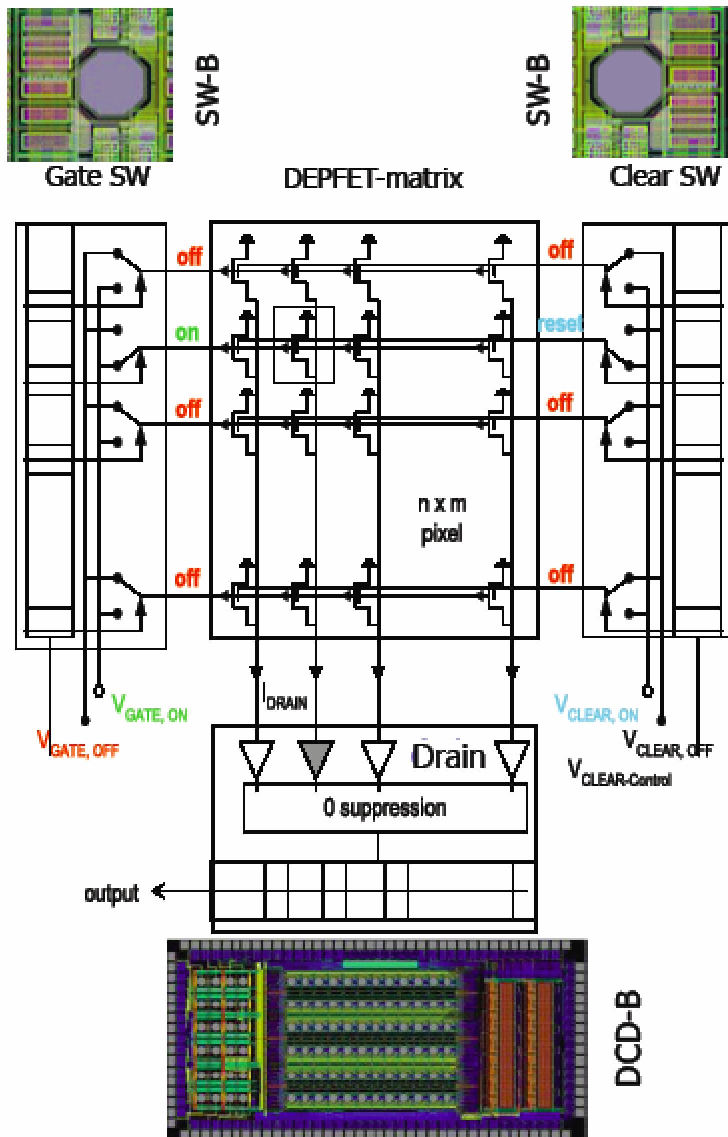
DEpleted P-channel FET





- fully depleted sensitive volume, charge collection by drift
- internal amplification → q-I conversion: 0.5 nA/e, scales with gate length and bias current
- Charge collection in "off" state, read out on demand

DEPFET Readout



Row wise r/o (Rolling Shutter):

- Select row with external gate, read current, clear DEPFET, read current again The difference is the signal
- Low power consumption: Only one row active at a time; Readout on demand (Sensitive all the time, even in OFF state)
- 100 ns readout time per pixel
- Two different auxiliary chips needed: Switchers for gate and clear
- Limited frame rate, but still: 50 kHz readout for 500 kPixel modules

DEPFET: custom technology

MPI Semiconductor Laboratory
(Halbleiterlabor: HLL)

Common project of the:

Max-Planck-Institut fuer Physik (Werner Heisenberg Institut), Munich
Max-Planck-Institut fuer extraterrestrische Physik, Garching

Founded in 1992, since 2000 located in the Siemens plant in Neu-Perlach, Munich

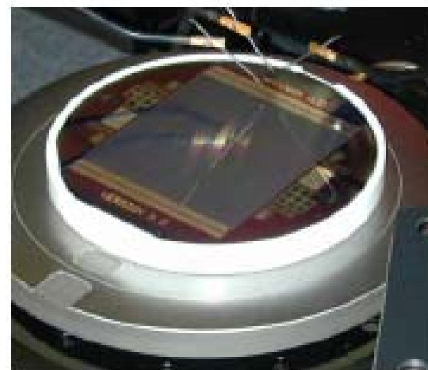
MPI HLL Facilities

800 m² cleanroom up to class 1 ...

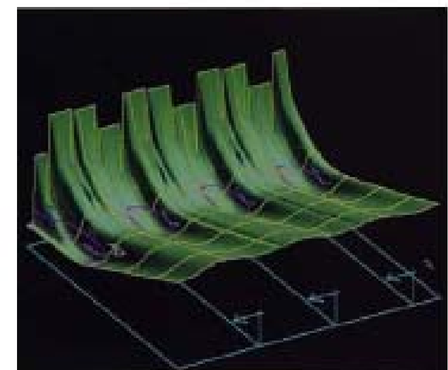
... with modern, custom made equipment ...

... for a full 6" silicon process line

mounting & bonding

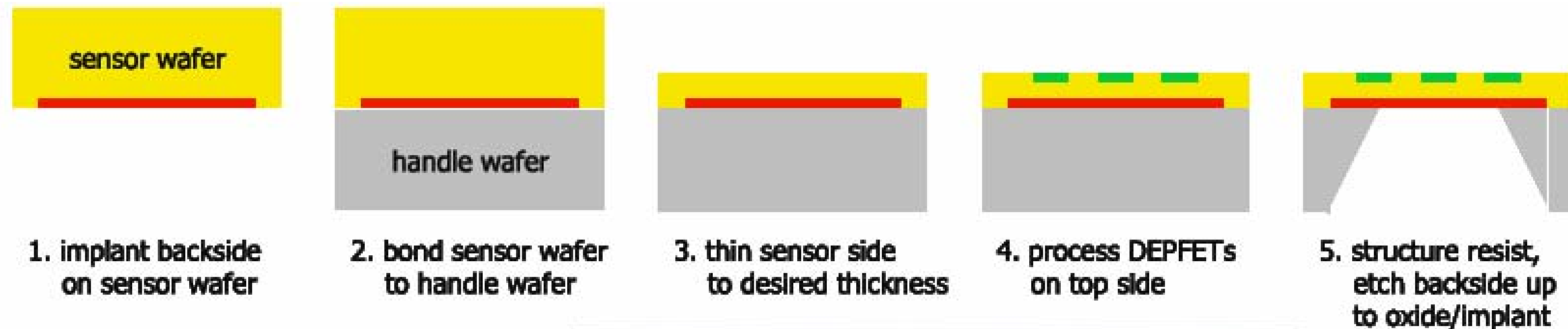


test & qualification

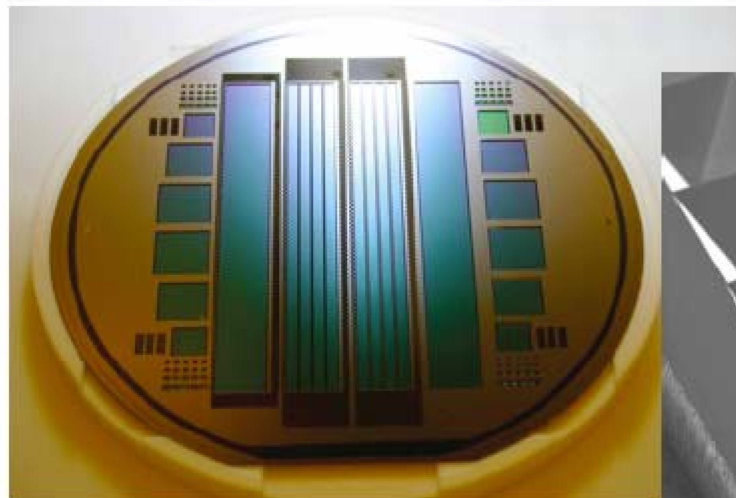


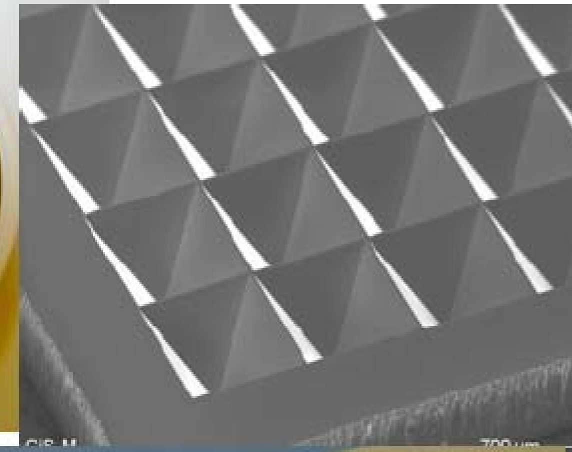
simulation, layout & data analysis

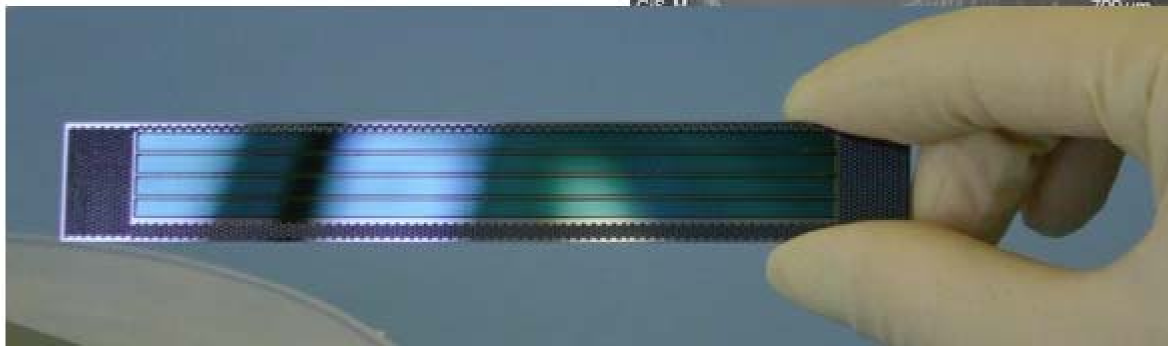
DEPFET Thinning technology



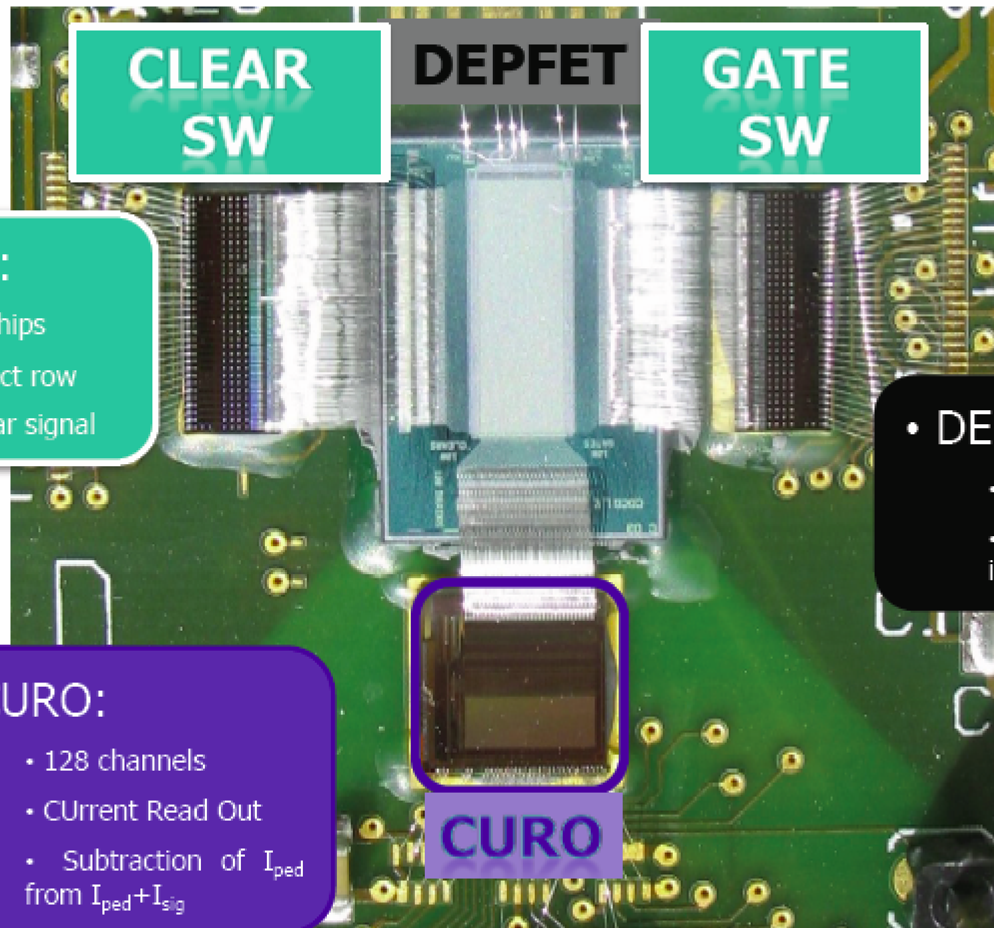
- Multi-step process
- Allows processing of both sides of sensor
- Mechanical support given by silicon structures produced in last etching step







DEPFET Test device

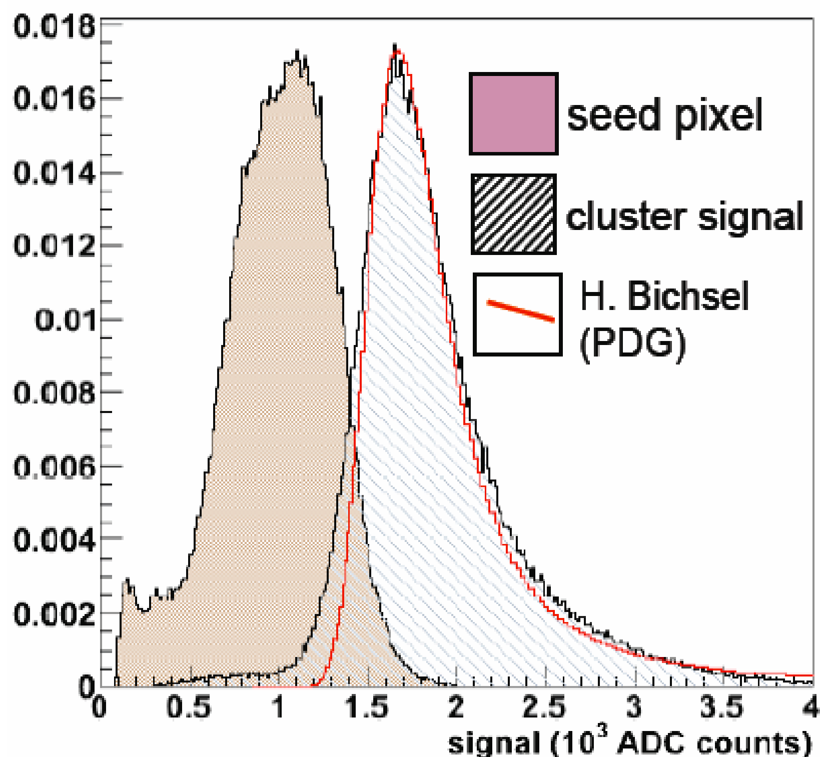


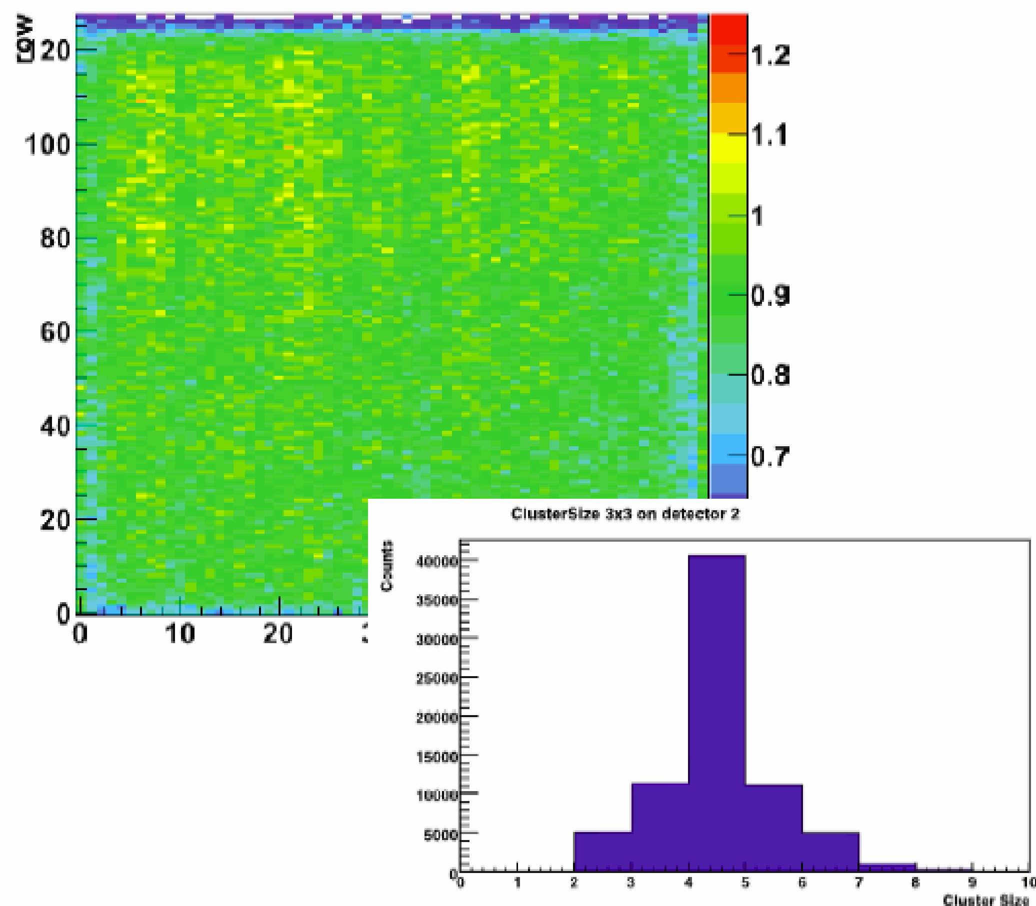
- PXD5 chips tested in 2009

- unthinned devices: Silicon thickness 450 μm
- Production of thinned sensors (thickness 50 μm) in progress: PXD6

DEPFET Test 2008 (EUDET telescope)

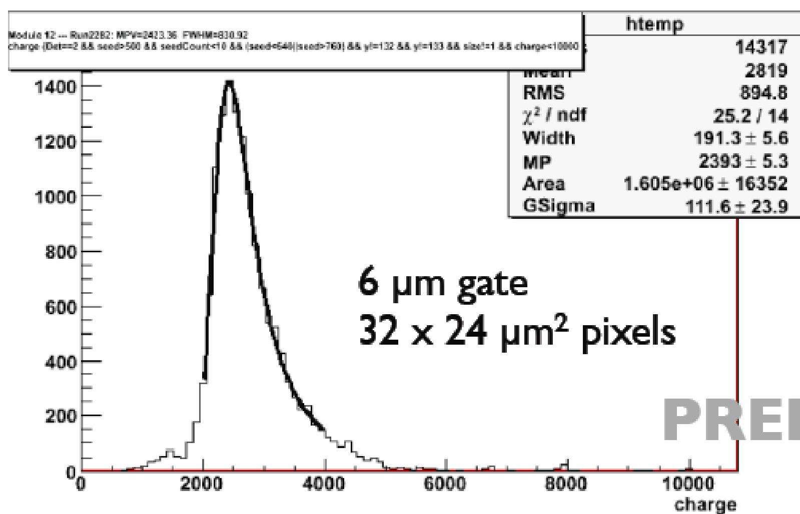
- Excellent performance observed: Clear detection of minimum ionizing particles, uniform response over the active area

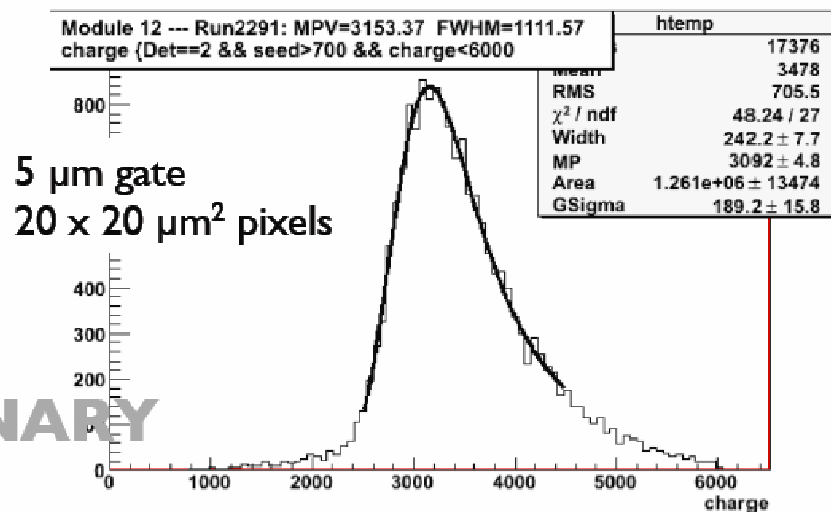




DEPFET Test-beam 2009

- Study of different lenghts of the gate : shorter gate → higher gain

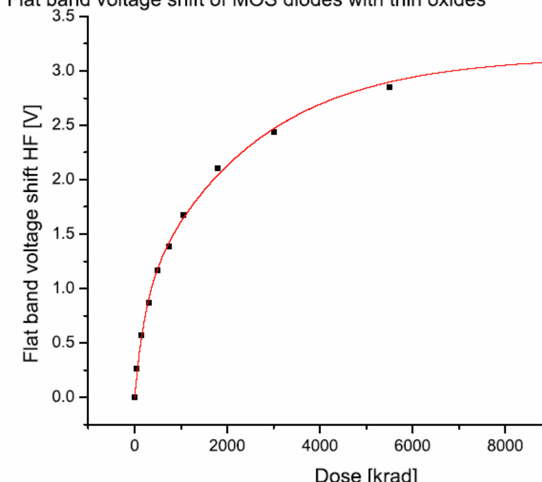




450 μm thick detector

2009: DEPFET = Baseline of Belle II PXD

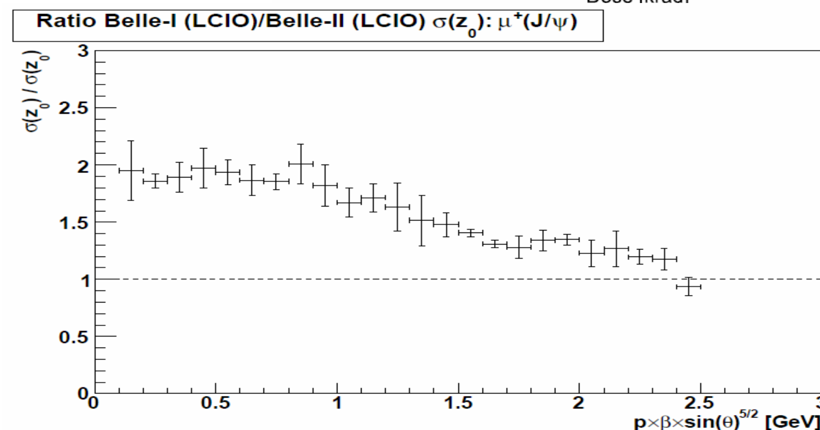
- Pixel size 50μm x 50mμ (inner), 50μm x 75μm (outer)
- Thinned to 75 μm
- Frame readout time 20μs (12.5ns per row of 1600 pixels)
- Low material budget: 0.16% X_0 /layer



- Radiation hardness: tested up to 10 MRad
  transistors thresholds shifts observed,
  but tolerable (device works well)
  Currently: the oxide thickness 200 nm,
  it will be lowered to 100 nm
  The detector should withstand
  first 4 – 5 years of operation

- Production starts in June 2010

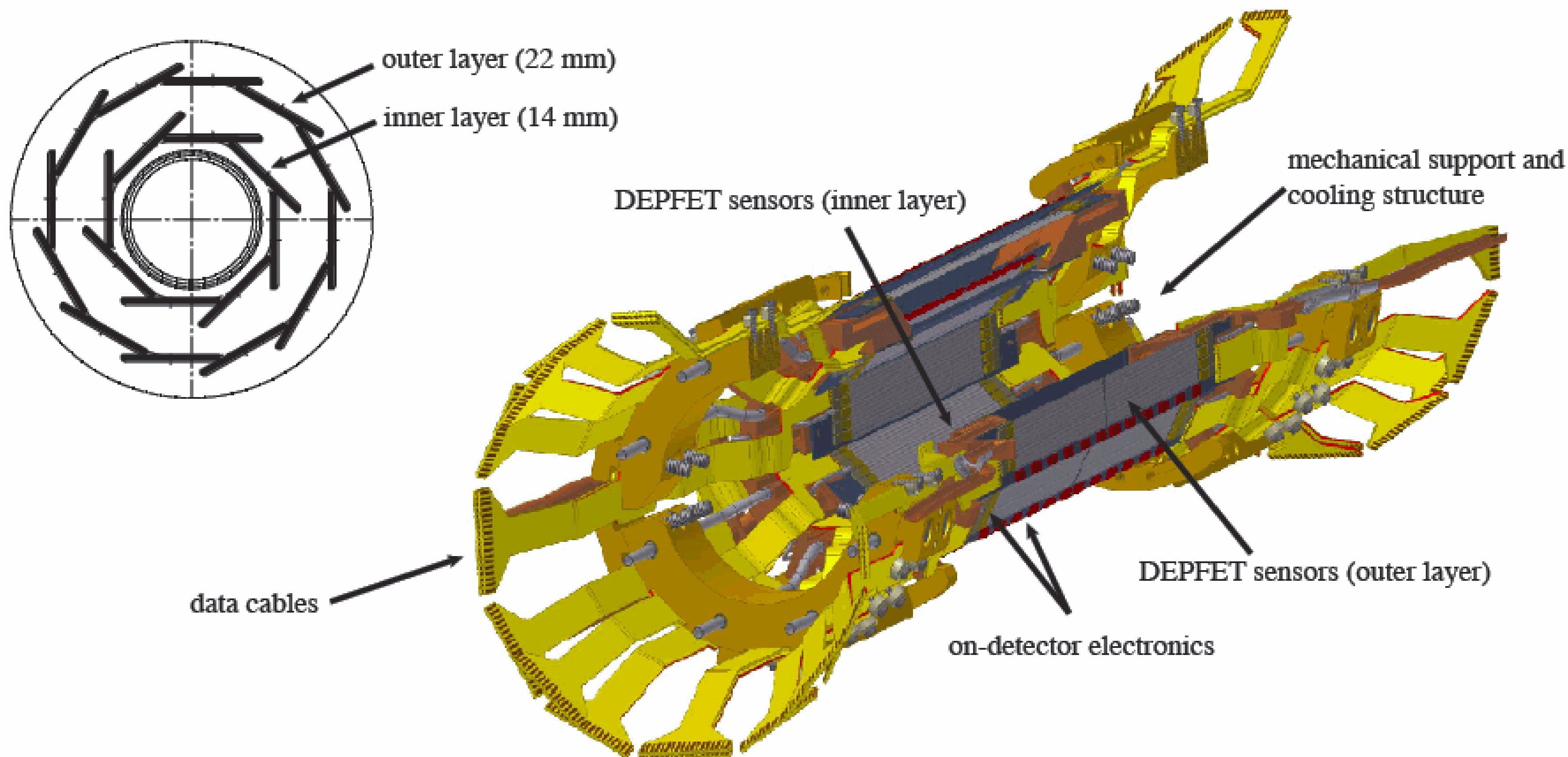
- Expected gain:



Belle II DEPFET PXD

- 250 x 800 pixels per half-ladder
- 12 outer and 8 inner modules
- Total number of pixels 8 M

- 2 layer pixel vertex tracker
  - inner layer at a radius of 14 mm, outer layer at 22 mm (beam pipe inner radius 10 mm, outer radius 12 mm ⇨ getting as close as we can!)



Belle II PXD: sense of scale

Low voltages for DEPFET (a nightmare)

- 18 voltage lines x 40 half-ladders = 720 PS output channels
  1) Can be prohibitive in price (100's k€)
  2) PSs 20-30m away from the ladders
    → difficult (imposible?) to regulate voltage drop at the PS in 2.3A lines
    R= 5mΩ/m * 30m [10 mm^2 cable]
    + $1.72 \cdot 10^{-8}$ Ωm *0.5 m/($17 \cdot 10^{-6}$ m *$3.48 \cdot 10^{-3}$ m)
    = 150 mΩ + 145 mΩ = 295 mΩ
    ΔV = 2.3A * 0.295Ω = 0.68 V (at V_0=1.8V)

→ voltage regulators needed, near to the ladder
then the number of PS output channels/half-ladder can be reduced, naively to 4 (+2.5V, +3.0V,+20V, -20V),
in practice to several channels