AGH University of Science and Technology
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Doctoral dissertation

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Development of novel low-power, submicron CMOS technology based, readout system for luminosity detector in future linear collider

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Declaration of the author of this dissertation:
Aware of legal responsibility for making untrue statements I hereby declare that I have written this dissertation myself and all the contents of the dissertation have been obtained by legal means.

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Declaration of the dissertation Supervisor:
This dissertation is ready to be reviewed.

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Streszczenie

Zrozumienie budowy materii i praw natury rządzących jej składnikami stanowi główny cel współczesnych eksperymentów Fizyki Wysokich Energii. Coraz większa statystyka danych wraz z rosnącą energią zderzeń cząstek na Wielkim Zderzaczu Hadronow LHC (ang. Large Hadron Collider) pozwoli najprawdopodobniej wyjaśnić mechanizm nadawania masy cząstkom elementarnym poprzez bozon Higgsa, którego obecność została potwierdzona niezależnie przez dwa eksperymenty na LHC, ATLAS i CMS, w kwietniu 2013 roku. Obok badań pozwalających na rozszerzenie i uzupełnienie Modelu Standardowego (ang. Standard Model), stanowiącego obecnie podstawowy opis materii, dane uzyskane z współczesnych i przyszłych eksperymentów pozwolą być może sięgnąć jeszcze głębiej w historię wszechświata, ujawniając informacje na temat ciemnej materii i ciemnej energii, będących według współczesnej kosmologii, przeważającymi jego częściami.

Nowo odkrywane zjawiska i związane z nimi procesy fizyczne wymuszają dalszy rozwój eksperymentów na akceleratorach cząstek. Sięgnięcie poza Model Standardowy (ang. Beyond Standard Model) w kierunku Nowej Fizyki (ang. New Physics) wymagać będzie dalszego zwiększenia energii zderzeń zachodzących w akceleratorach. Do precyzyjnego pomiaru własności i parametrów nowych cząstek, takich jak bozon Higgsa, potrzebny będzie ponadto dużo prostszy system zderzeń niż proton-proton, stosowany obecnie na LHC. Takim systemem, umożliwiającym ponadto znacznie precyzyjniejszą rekonstrukcję zdarzeń w obecności niższego tła, może być układ zderzeń dwóch leptonów, a w szczególności pozytonu i elektronu. Współcześnie prowadzone są prace rozwojowe nad dwoma międzynarodowymi projektami zderzacza leptonów: Międzynarodowym Zderzaczem Liniowym ILC (ang. International Linear Collider) i Kompaktowym Zderzaczem Liniowym w CERN CLIC (ang. Compact Linear Collider at CERN). Poza istotnymi różnicami dzielącymi oba projekty, tj. technologią przyspieszania leptonów i maksymalną energią dostępną w centrum masy, założenia systemów detekcyjnych w obu eksperymentach są do siebie zbliżone. Oba projekty bazują na precyzyjnej rekonstrukcji energii i torów tak cząstek pierwotnych jak i wtórnych (ang. particle Flow), stawiając bardzo wysokie wymagania detektorom i systemom odczytowym przyszłych eksperymentów. Niezwykle wysoka precyzja pomiaru położeń cząstek wymagać będzie bardzo wysokiej segmentacji przestrzennej detektorów, zwiększając wielokrotnie liczbę kanałów elektroniki odczytu. Pociąga to za sobą wzrastające wymagania tak na minimalizację poboru mocy elektroniki odczytu jak i wymusza coraz efektywniejsze metody przetwarzania i transmisji sygnałów z detektora.

Głównym celem niniejszej rozprawy jest rozwój systemu odczytowego dla detektora świetlności LumiCal (ang. Luminosity Calorimeter) w przyszłym eksperymencie na zderzaczu liniowym. Detektor, a właściwie kalorymetr ten odpowiedzialny będzie za precyzyjny pomiar świetlności akceleratora, niezbędny do precyzyjnej analizy danych zebranych w eksperymencie. Prace badawczo-rozwojowe (ang. Research and Development) nad detektorem LumiCal prowadzone są w ramach międzynarodowej współpracy FCAL skupiającej wiele instytutów badawczych z różnych krajów i kontynentów, w tym Katedrę Oddziaływań i Detekcji Cząstek na Wydziale Fizyki i Informatyki Stosowanej Akademii Górniczo-Hutniczej w Krakowie. Powyższa rozprawa prezentuje prace przeprowa-

dzone przez autora, tak przy budowie i uruchomieniu prototypu detektora LumiCal, przeprowadzaniu testów na wiązce i analizie ich wyników, jak również przy rozwoju nowatorskiego systemu odczytu dla tego detektora, bazującego na dedykowanych układach scalonych ASIC (ang. Application Specific Integrated Circuit) wykonanych w głęboko submikronowych technologiach CMOS (ang. Complementary Metal Oxide Semiconductor). Większość tekstu rozprawy opisuje prace wykonane przez autora, jednak dla zrozumiałości i zachowania spójności, pokrótce przedstawione zostały ogólne zagadnienia związane z tematyką zderzaczy liniowych, detektora LumiCal oraz istniejącą już pierwszą wersją modułu odczytowego tego detektora.

Pierwszy rozdział rozprawy prezentuje ogólne zagadnienia dotyczące założeń i konstrukcji akceleratorów liniowych, wykonywanych na nich eksperymentów, jak również systemu detektorów tych eksperymentów. Zaczynając od ogólnego przedstawienia obecnego stanu wiedzy, przedstawiona została rola liniowych akceleratorów w zrozumieniu budowy materii, jak i dostarczane przez nie możliwości sięgnięcia w kierunku Nowej Fizyki. Zaprezentowane zostały wymagania stawiane przyszłym eksperymentom na tych zderzaczach, jak i proponowane przez międzynarodowe kolaboracje rozwiązania, czyli eksperymenty ILC i CLIC. Przedstawione zostały również planowane systemy detekcyjne tych eksperymentów, ze szczególnym naciskiem położonym na tzw. detektory „do przodu" (ang. Forward Region) – BeamCal oraz LumiCal. Pierwszy z nich odpowiedzialny jest za szybkie dostarczenie informacji niezbędnych do ciągłego monitorowania i kontrolowania wiązki, podczas gdy drugi, którego system odczytowy stanowi główną tematykę niniejszej rozprawy, odpowiedzialny jest za precyzyjny pomiar świetlności. Przedstawiona została istota pomiaru świetlności i jego znaczenie dla eksperymentu. Na koniec omówione zostały główne założenia systemu odczytowego, jego architektura oraz istniejący prototyp w postaci modułu odczytowego, zawierającego pierwszą generację dedykowanych układów scalonych elektroniki odczytu. Układy te również zostały poglądowo omówione. Dla dopełnienia, poglądowo zaprezentowane zostały także zagadnienia generacji sygnału w detektorze krzemowym i jego przetwarzania w torze elektroniki odczytu.

W rozdziale drugim przedstawione zostały pierwsze pomiary na wiązce wykonane za pomocą wielopłaszczyznowego modułu detektora LumiCal. Rozdział rozpoczyna się opisem wstępnych prac przygotowujących istniejące moduły odczytowe do pracy wielopłaszczyznowej, następnie zaprezentowana jest konstrukcja i architektura modułu detektora, w którego budowie i wstępnych testach autor brał aktywny udział. Omówione zostało również oprzyrządowanie systemu pomiarowego użytego podczas testów na wiązce akceleratora protonów PS (ang. Proton Synchrotron) w CERN. Analiza danych zebranych w czasie testów wymagała przygotowania dedykowanego oprogramowania umożliwiającego ekstrakcję, obróbkę i wieloaspektową analizę otrzymanych danych, tak z modułu detektora LumiCal, jak i ze wspomagającego pomiar detektora mierzącego tory cząstek, tzw. teleskopu. Autor szczegółowo omawia zagadnienia związane z analizą danych z obu detektorów. Przedstawiona i przedyskutowana została procedura znalezienia precyzyjnego położenia płaszczyzn teleskopu (ang. alignment) w celu dokładnej rekonstrukcji torów cząstek. W przypadku detektora LumiCal autor rozważa pełny proces wstępnej obróbki danych, obejmujący w szczególności usunięcie składowych stałych (ang. baseline, pedestal) oraz sygnału wspólnego (ang. common mode) na różnych kanałach odczytowych. Ze względu na użycie pierwszej wersji modułów odczytowych nie projektowanych z myślą o pracy wielopłaszczyznowej, zagadnienie redukcji zakłóceń wspólnych było niezwykle istotnym czynnikiem obróbki danych, umożliwiającym zdecydowaną poprawę finalnego stosunku sygnału do szumu w detektorze. W dalszej kolejności autor przedstawia nowatorską metodę rekonstrukcji sygnału (ładunku) deponowanego w sensorze krzemowym poprzez zaawansowaną procedurę cyfrowej obróbki danych (ang. Digital Signal Processing). Rezultaty uzyskane powyższymi metodami umożliwiły autorowi wykonanie analiz fizycznych zebranych danych, w szczególności pozwoliły na przedstawienie rozwoju kaskady elektromagnetycznej (ang. electromagnetic

shower), jako jednego z podstawowych celów pomiarowych detektora LumiCal. Wyniki analiz zostały zebrane i przedyskutowane na zakończenie rozdziału drugiego.

Równolegle z pracami nad przygotowaniem i przeprowadzeniem testów na wiązce prototypu detektora LumiCal, autor prowadził prace nad koncepcją, rozwojem i testami drugiej generacji dedykowanych układów odczytu detektora LumiCal w głęboko submikronowych technologiach CMOS. Rosnące wymagania na redukcję poboru mocy, zwiększenie odporności radiacyjnej i zwiększenie gęstości upakowania kanałów, wymuszone rosnącymi wymaganiami dla detektorów w przyszłych eksperymentach Fizyki Wysokich Energii, pociągają za sobą konieczność stałego rozwoju układów elektroniki odczytu. W szczególności trudności związane z obróbką, gromadzeniem i transmisją analogowych danych pomiarowych, przy rosnącej ilości kanałów i częstości zdarzeń rejestrowanych w detektorze, wymagają nowatorskiego podejścia do zagadnienia przetwarzania sygnału z sensora. Klasyczny układ analogowego przedwzmacniacza wraz z układem kształtującym (ang. front-end), zwielokrotniony do postaci układu wielokanałowego jest obecnie standardem stosowanym we współczesnych systemach detekcji. Jednakże zastosowanie przetwornika analogowo-cyfrowego (ang. Analog to Digital Converter), indywidualnie w każdym z kanałów, pozostawało dotychczas w strefie rozważań teoretycznych, głównie ze względu na wysoki pobór mocy takich przetworników. Zastosowanie takiego rozwiązania uprościłoby architekturę elektroniki odczytu, przynosząc równocześnie wiele korzyści w dalszej obróbce danych, dostępnych bezpośrednio w cyfrowej postaci. W efekcie mogłaby też istotnie wzrosnąć szybkość przetwarzania cyfrowych już danych, tak ważna i wymagana dla detektorów w przyszłych eksperymentach Fizyki Cząstek.

Nowe generacje głęboko submikronowych technologii CMOS otwierają nowe możliwości dla rozwoju elektroniki odczytu detektorów. Rozpoczynając rozdział trzeci, autor przedstawia podstawową charakteryzację trzech technologii – jednej, wykorzystanej w obecnie istniejącym module odczytowym detektora LumiCal, oraz dwóch bardziej zaawansowanych (o mniejszym rozmiarze charakterystycznym, tj. mniejszej minimalnej długości kanału tranzystora MOS), przeznaczonych dla nowej generacji systemu odczytu. Wykazane zostały zalety nowych submikronowych technologii CMOS, takie jak większa częstotliwość pracy przy jednoczesnym zmniejszeniu poboru mocy, kosztem jednakże zmniejszonego wzmocnienia tranzystorów. Niższe wzmocnienie stanowi wyzwanie dla projektu analogowego przedwzmacniacza ładunkowego (ang. charge preamplifier), koniecznego dla ekstrakcji i kształtowania sygnału z sensora. Opierając się na tych rozważaniach, autor przedstawia założenia i projekt drugiej generacji dedykowanego układu front-end dla detektora LumiCal. Wyniki pomiarów prototypowego układu, wykonanego w technologii CMOS 130 nm, przedstawione w rozdziale trzecim, potwierdzają poprawną i zgodną ze specyfikacją pracę układu.

Najistotniejszą (najtrudniejszą) część rozwoju elektroniki odczytowej stanowi projekt 10-bitowego przetwornika analogowo-cyfrowego (ang. ADC), przystosowanego do integracji wielokanałowej. Autor przedstawia początkowe rozważania nad założeniami i implementacją przetwornika, wykazując wysoki potencjał architektury kolejnych przybliżeń SAR (ang. Successive Approximation Register). Omówiony został wykonany przez autora projekt 10-bitowego przetwornika SAR ADC oraz założenia leżące u podstaw procedury symulacyjno-pomiarowej, niezbędnej tak do weryfikacji projektu w fazie rozwojowej, jak i pomiaru parametrów wykonanego prototypu. Następnie przedstawione zostały wyniki pomiarów trzech prototypów przetwornika, wykonanych w dwóch głęboko submikronowych technologiach CMOS 130 nm. W szczególności trzeci z prototypów wykazał się doskonałymi parametrami, stawiającymi ten projekt wśród najlepszych dostępnych na świecie układów. Uzyskany znikomy, w porównaniu do przetwornika zastosowanego w pierwszej generacji odczytu, pobór mocy umożliwia implementację 10-bitowego przetwornika ADC w każdym z kanałów elektroniki odczytu, wraz z poprzedzającym go układem przedwzmacniacza ładunkowego i układu kształtującego.

Bazując na wykonanych układach elektroniki front-end i ADC, w kolejnym kroku możliwe będzie zaprojektowanie i wykonanie pełnego (integrującego wszystkie funkcjonalności) wielokanałowego układu odczytowego detektora LumiCal. Będzie to następne zadanie autora. Układ taki będzie jednym z pierwszych, o ile nie pierwszym na świecie, wielokanałowych dedykowanych układów odczytu, z szybkim przetwornikiem ADC w każdym kanale.

Wyznaczone cele pracy zostały w pełni przez autora zrealizowane. Przygotowane i wykonane testy na wiązce wielopłaszczyznowego modułu detektora LumiCal dostarczyły danych, których analiza potwierdziła spełnienie bazowych założeń i pokazała dalsze możliwości rozwojowe projektu. Prowadzone równolegle prace nad projektem nowej generacji elektroniki odczytu doprowadziły do powstania w pełni funkcjonalnych dedykowanych układów scalonych w głęboko submikronowych technologiach CMOS. W szczególności projekt 10-bitowego przetwornika ADC otwiera nową drogę dla rozwoju wielokanałowych systemów odczytu detektorów.

Podczas długiej działalności związanej z pracami badawczo-rozwojowymi, autor rozprawy zdobył unikalne doświadczenie przy budowie oraz testowaniu zaawansowanych systemów detekcji promieniowania, w szczególności obejmujące projektowanie i testowanie dedykowanych układów scalonych ASIC. Prace autora związane były ze wszystkimi fazami rozwoju typowego eksperymentu Fizyki Cząstek, od prac koncepcyjnych i konstrukcyjnych rozpoczynając, poprzez rozwój podstawowych składników systemu odczytowego i dedykowanej elektroniki, a następnie przygotowaniu i uczestnictwie w testach na wiązce, kończąc na opracowaniu i analizie uzyskanych danych eksperymentalnych.

Contents

Introduction

Understanding the structure of matter and the basic laws of nature is a major goal of modern High Energy Physics (HEP) experiments. The increasing center-of-mass energy at Large Hadron Collider (LHC) together with continuously growing data statistics should most likely allow to explain how the existing particles acquire their masses through the Higgs field. The existence of quantum of this field, called the Higgs boson, was independently announced by two LHC experiments – A Toroidal LHC Apparatus (ATLAS) and Compact Muon Solenoid (CMS) in April 2013. Though the current research is mainly focused on expanding and complementing the Standard Model (SM), which is currently the basic description of the matter, the data collected in current and future experiments will perhaps allow us to reach even deeper insight into history of the universe, revealing informations about dark matter and dark energy. Even though, according to the modern cosmology, they are overwhelming parts of the universe, their true nature still remains a mystery for the contemporary physics.

The newly discovered phenomena and the related physical processes necessitate further development of experiments and particle accelerators. Reaching Beyond Standard Model (BSM), in the direction of New Physics, will require a further increase in energy of collisions occurring in accelerators. For precise measurement of properties and parameters of the newly discovered particles, such as the Higgs boson, a collision system much simpler than proton-proton, currently utilized by the LHC, is strongly preferred. In order to enable a precise reconstruction of the events in the presence of lower experimental background, a two leptons collision system, a positron and an electron in particular, can be used. The two international lepton collider projects are nowadays under development: International Linear Collider (ILC) and Compact Linear Collider at CERN (CLIC). Beside the significant differences, i.e the leptons accelerating technique and the maximum center-of-mass energy, the basic concept of the detector system in both projects is very similar. A Particle Flow algorithm, based on the precise reconstruction of energy and tracks of all particles (both primary and secondary) generated in the collision, sets a very high demands on detectors and readout systems of these future experiments. The required extremely high precision measurement of particle position enforces a very high spatial segmentation of detectors, increasing significantly the number of readout channels. This entails increasing requirements on the readout electronics power consumption and forces a more efficient methods of processing and transmitting the signals from the detector.

The development of the Luminosity Calorimeter (LumiCal) for the future linear collider is the main objective of this dissertation. This calorimeter will be responsible for the precise measurement of the accelerator luminosity, necessary for accurate analyze of data collected in the experiment. Research and Development (R&D) activities for the LumiCal detector are conducted within the framework of international cooperation, the Forward CALorimetry (FCAL), bringing together many research institutes from different continents and countries, including the Department of Particle Interactions and Detection Techniques at Faculty of Physics and Applied Computer Science, University of Science and Technology in Krakow. This dissertation presents the executed works, starting from the construction and commissioning of the prototype LumiCal detector, through the

testbeam of the LumiCal prototype together with the analysis of collected data. A concurrent development of new generation of innovative readout system for this detector, based on Application Specific Integrated Circuits (ASICs) made in deep-submicron Complementary Metal-Oxide Semiconductor (CMOS) technologies, is a second, essential part of the dissertation. Although the majority of the dissertation contents describes the work done by the author, also other issues related to linear colliders, LumiCal detector and first version of the detector readout, etc., are briefly presented for clarity and consistency.

In the first chapter, the general issues regarding the design and construction of linear accelerators, their experiments and detector systems are presented. Starting with an overview of the current state of art, the role of linear accelerators in understanding the structure of matter, as well as provided opportunities towards the New Physics, are discussed. The requirements for future experiments on these colliders, together with solutions proposed by international collaborations (i.e ILC and CLIC), are presented, including the detector systems foreseen for these experiments. Particular emphasis is placed on so-called Forward Region, comprising two dedicated calorimeters – Beam Calorimeter (BeamCal) and LumiCal. The first one is responsible for a fast, continuous beam monitoring, providing informations necessary for beam controlling and tuning. The second one, which is the main subject of this dissertation, is responsible for a precise measurement of the luminosity. The principia of this measurement, as well as its importance for the whole experiment, are presented. At the end, the main assumptions and architecture of the LumiCal readout system are discussed, and the existing readout module, containing the first generation of dedicated ASICs is presented. These ASICs are also briefly described. To complete, the generation of signal in the silicon sensors and its processing in the readout electronics chain are illustratively discussed.

The second chapter presents the first testbeam measurements of the multi-plane LumiCal detector prototype. The chapter begins with the description of preliminary works on preparation of the existing modules for multi-plane operation. Afterwards, the design and architecture of the detector prototype, its construction and preliminary tests, in which the author was actively involved, are presented. The instrumentation and measurement setup of the testbeam, performed on the Proton Synchrotron (PS) accelerator at Conseil Européen pour la Recherche Nucléaire (CERN), are also described. A dedicated software allowing the extraction, processing and multi-faceted analysis of the data, collected during the testbeam by the LumiCal detector and by the supporting detector measuring the particle tracks, so-called telescope, was developed. The author discusses in detail the issues related to the data analysis from the both detectors. The procedure finding a precise mutual position of the telescope planes, so-called alignment, in order to enable an accurate reconstruction of particle tracks, is presented. For the LumiCal detector, author describes the complete process of initial data processing, including, in particular, the removal of baseline (pedestal) and common mode disturbances. Since the first version of the readout modules was not designed with the aim of multi-plane operation, the common mode reduction was a very important issue in the data processing, enabling a significant improvement in the final Signal-to-Noise Ratio (SNR) of the detector prototype. Next, the author presents an innovative method of reconstruction of charge deposited in silicon sensor, using an advanced Digital Signal Processing (DSP) procedure. The results obtained from the above method, have enabled the author to undertake the physical analysis of the collected data. In particular, the development of electromagnetic shower could be investigated, as one of the main objectives of the LumiCal detector measurements. The results of the analysis are collected and discussed at the end of the second chapter.

In parallel to preparation and carrying out the testbeam of the LumiCal prototype, author worked on the concept, development and testing of the second-generation of readout ASICs, in deep submicron CMOS technologies. The increasing demands for detectors in future HEP experiments tighten

the requirements on power consumption, radiation hardness and density of channels, entailing a continuous development of the readout electronics. In particular, the difficulties associated with processing, collecting, and transmitting of analogue signals, from the increasing number of channels and the growing frequency of events recorded in the detector, require an innovative approach to the signal processing in radiation sensor. The conventional front-end electronics with a preamplifier and a shaping system, integrated into a multi-channel readout, is a standard used in modern detection systems. However, the implementation of Analog-to-Digital Converter (ADC), individually in each readout channel, remained so far in the area of theoretical considerations, mainly due to high ADC power consumption. Such solution would simplify the architecture of readout electronics, bringing also many advantages in further processing. It could also significantly increase the data processing speed, extremely important and required for the detectors at future Particle Physics experiments. The new generation of deep sub-micron CMOS technologies opens up a new possibilities for the development of such advanced detector readout systems.

In the third chapter, author presents the basic characterization of three sub-micron CMOS technologies - one currently used in the existing LumiCal readout module, and two more advanced (with a smaller characteristic size, i.e smaller minimum Metal-Oxide Semiconductor (MOS) transistor channel length), intended for a new generation of the readout system. Based on these considerations, author presents the assumptions and the design of the second generation of dedicated front-end ASIC, fabricated in 130 nm CMOS technology. The measurements results of the prototype, presented in the third chapter, confirm the correct, complying with the specification, operation of the designed ASIC. The most important (most difficult) part of the readout electronics development is the design of ultra-low power 10-bit ADC, prepared for multi-channel integration. The author presents initial considerations on assumptions and architecture of the converter, demonstrating a high potential of the Successive Approximation Register (SAR) architecture. The developed 10-bit SAR ADC is presented in detail, together with the simulations and measurements procedures necessary for the design verification in the development phase. The measurements results of three ADC prototypes, fabricated in two deep sub-micron CMOS 130 nm technologies, are presented. In particular, the third prototype demonstrates excellent performance, placing this project among the best works, currently presented in the world. The achieved power consumption, negligible compared to the first ADC generation, enables the implementation of a 10-bit ADC in each of the readout electronics channels, together with a preceding charge sensitive preamplifier and shaper circuitry.

Chapter 1

Future Linear Colliders and High Energy Physics (HEP) experiments

Since the dawn of time, people have been debating the construction of matter. Even though the impossibility of direct observation, the ancient Greeks guessed that on the macroscopic properties of matter affect their microscopic components, called by them atoms, i.e. non-divisible particles. This supposition remained unconfirmed until the 19th century. One of the first steps to understanding the nature of matter was made by Dmitri Mendeleev who sorted all known then materials by their properties creating the periodic table. He also suggested, that gaps remaining in the table were probably indicating elements undiscovered at that time, which was soon confirmed by the findings of new materials complementing the periodic table. At the end of 19th century, Joseph Thomson discovered a negatively charged electron, the first subatomic particle. During that time, the radioactivity was discovered and studied by Pierre and Marie Curie, while Wilhelm Conrad Röntgen worked on, discovered by himself, the X-ray phenomenon. The discovery of radioactivity allows Ernest Rutherford to experiment with alpha particles scattering. The angle distribution of scattered particles leads him to conclusion that almost the entire atom's mass is concentrated in a very small volume in its geometrical center. This, positively charged, "new particle" was called the atom's nuclei. Very soon, from Rutherford's collision of alpha particles with gases experiments, it becomes clear that atom's nuclei is composed from more fundamental particles, the protons. From simplest nuclei of hydrogen, consisting only of one proton, the nuclei of more complicated atoms are composed from increasing numbers of protons. It was however clear, that the nuclei should consist of something more than just protons. The missing nuclei component, a neutron, was independently discovered by James Chadwick and Walter Bothe at the beginning of the 20th century.

The radioactivity phenomenon research has revealed that some of radioactive elements emit the electron during their decay, called the β-decay. Even before the James Chadwick and Walter Bothe discovery, Wolfgang Pauli hypothesized an undetected particle, called by him a "neutron", emitted from the nucleus together with the electron to explain how β-decay could conserve the energy, momentum, and angular momentum (spin). Since new nuclei component was also named neutron by its discoverers, the two kinds of particles received the same name. To resolve this confusion, Enrico Fermi, who developed the theory of β-decay, called the Pauli's hypothetical particle neutrino. Therefore a β-decay could be explained as decay of neutron into a proton, an electron and an antineutrino. The new Pauli's particles remain undiscovered until the second half of the 20th century. Analogously to a pair of neutrino - antineutrino, the antiparticle of electron, called positron, was proposed by Paul Dirac and verified experimentally in a very short time.

The special theory of relativity, postulated by Albert Einstein, provided a revolutionary postulate of equivalence between mass and energy. It becomes clear that some new particles with a mass higher than the heaviest known particle, a neutron, can be created in collisions providing sufficient energy. Since none of available natural phenomenons, such as radioactive decays, could provide such high amount of energy, the accelerators were built to deliver particles accelerated to high energies. Along with the accelerators development, the collision energy were increased to discover of new particles with different properties. Based on the experience, such as discovery of nuclei components, newly discovered particles were suspected to be built from more elementary components. A new theory was needed to organize the new discoveries and determinate the complete set of elementary particles. From symmetry considerations, a scheme called Standard Model (SM) was proposed. It assumes, that all the particles and phenomenons can be described using only six quarks and six leptons (with their antiparticles) as the only primary constituents of matter. To explain the fundamental interactions (strong, weak and electromagnetic), the gauge bosons (eight gluons for strong, the W^+, W^- and Z^0 for weak and photon for electromagnetic interactions) were introduced into the SM. Since all the elementary particles in SM are assumed as massless, the Higgs boson was proposed by Robert Brout, François Englert, Peter Higgs, Gerald Guralnik, Carl Richard Hagen, and Tom Kibble to explain why the other elementary particles, except the photon and gluon, are massive. In total 61 of primary particles (including their antiparticles) are foreseen. The SM allows to predict many of undiscovered particles and provides the order in already known ones, as it was done for elements in Mendeleev's table. However, it is based on a set of arbitrary chosen parameters which cannot be derived from any fundamentals, which causes that it can not be regarded as a fully-fledged theory. Thanks to the modern accelerators (such like Large Electron Positron Collider (LEP), Hadron-Electron Ring Accelerator (HERA) and Tevatron) development, the precise measurements of all parameters became possible, which allowed to extensively test the SM. Furthermore, the SM describes only three fundamental interactions while the fourth one, the gravity, is missing as well as explanation of origin and parameters of dark energy and matter. To extend the SM or develop some new theory, additional experimental data were, and still are, needed.

To test the predictions of different theories of particle physics and High Energy Physics (HEP), especially the SM, and to prove or disprove the existence of the theorized Higgs boson in particular, the Large Hadron Collider (LHC) was built [1]. It is located at Conseil Européen pour la Recherche Nucléaire (CERN) near Geneva and is the largest and most complex experimental facility ever built. The main synchrotron of the LHC, located in a 27 km long tunnel 50 – 175 meters underground, provides the two counter-rotating beams of protons accelerated to the energy of 6.5 TeV. The beams collide four times in each circulation inside four main experiments: A Toroidal LHC Apparatus (ATLAS), Compact Muon Solenoid (CMS), A Large Ion Collider Experiment (ALICE), and Large Hadron Collider beauty (LHCb). These experiments, besides the already mentioned objectives, should also allow to insight into a new physics, the Beyond Standard Model (BSM) such as supersymmetry.

1.1 Future Linear Colliders

A lot of measurements, also possible on LHC in hadron collisions, can be performed in more precise manner by a lepton-antilepton collisions. In this case, both particles annihilate providing pure energy for new particles creation what results in significantly cleaner and simpler experimental background. As an example one may serve here the W and Z^0 bosons, which were discovered in proton–antiproton collision in Super Proton Synchrotron (SPS), but precise measurements of their properties were possible using the electron–positron collisions in LEP. Therefore, the Research and Development (R&D) on future high energy lepton collider designs has already begun in the HEP community. Since each

charged particle accelerated radially emits electromagnetic radiation, called synchrotron radiation, the energy loss in circular accelerator is one of the major issues. As power radiated (lost) by electron is proportional to its square energy and inversely proportional to the square radius of its track, increasing the energy of particles entails an increase of the accelerator radius. The radius of accelerator able to accelerate an electron to the TeV energy scale would be unreasonably high (above 100 km). Therefore the linear layout, instead of circular, is considered for future lepton accelerators. Currently the two concepts of electron–positron linear accelerators – the International Linear Collider (ILC) [2, 3, 4, 5] and the Compact Linear Collider at CERN (CLIC) [6, 7, 8], are under investigation and will be described in details in the following sections.

1.1.1 Physics at Linear Colliders

Nowadays, one of the most important issues of elementary particle physics is to search for new particles and forces at energies of hundreds or thousands of GeV. This research can fill the gaps in the Standard Model (SM) as well as extensively test it. The equations of the SM are based on a symmetry principle, electroweak symmetry, that forbids the generation of mass for any of its fundamental particles. The asymmetrical force, creating the masses for quarks, leptons, and bosons as well as affecting other properties of the laws of nature, is therefore foreseen as an essential element of the universe. As the source of this force, a field called the Higgs field is postulated in the SM, but does not provide a detailed explanation of its properties. It has to be noted, that putting Higgs field as the only source of asymmetry is still only a guessing from many other possibilities. The quantum of Higgs field, called the Higgs boson, should be therefore founded and precisely measured to prove the accuracy of this idea.

Process	Energy [GeV]	Physics Goal
$e^+e^- \to Z$	91	ultra precision electroweak measurements
$e^+e^- \to WW$	160	ultra precision W mass measurements
$e^+e^- \to Zh$	250	precision Higgs couplings measurements
$e^+e^- \to t\bar{t}$	350–400	top quark mass and couplings measurements
$e^+e^- \to W\bar{W}$		precision W couplings measurements
$e^+e^- \to \nu\bar{\nu}h$		precision Higgs couplings measurements
$e^+e^- \to f\bar{f}$	500	precision search for Z'
$e^+e^- \to t\bar{t}h$		Higgs coupling to top quark measurements
$e^+e^- \to Zhh$		Higgs self-coupling measurements
$e^+e^- \to \tilde{\chi}\tilde{\chi}$		search for supersymmetry
$e^+e^- \to AH, H^+, H^-$		search for extended Higgs states
$e^+e^- \to \nu\bar{\nu}hh$	700–1000	Higgs self-coupling measurements
$e^+e^- \to \nu\bar{\nu}VV$		composite Higgs sector
$e^+e^- \to \nu\bar{\nu}t\bar{t}$		composite Higgs and top quark
$e^+e^- \to \tilde{t}\tilde{t}^*$		search for supersymmetry

Table 1.1: Major physics processes at ILC at various energies [9].

The challenge in hadron colliders is a Quantum Chromodynamics (QCD) background affecting the experimental environment while the background processes of electron-positron collisions are many orders of magnitude smaller. In addition, the linear lepton colliders allow to precisely measure and control the center-of-mass energy and initial state polarization. Therefore the very rich linear colliders physics program can cover precise measurements of the properties of Higgs field and the

interactions of top quarks, gauge bosons and new particles, and can reach beyond the SM into a New Physics. The major physics processes that are foreseen to be studied by lepton colliders are shown in Table 1.1.

In July 2012, a new particle with many properties of the Higgs boson postulated by SM, including a mass of 125 GeV, was announced by the ATLAS and CMS experiments at LHC. The possibility that the Higgs boson has higher mass (up to masses beyond 600 GeV, close to the theoretical upper bound) was also excluded by these experiments. The fundamental properties of this particle, such like mass, spin and parity quantum numbers, the couplings to the fermions and gauge bosons as well as its self-coupling, should be precisely measured. This study should allow to reconstruct the scalar potential of the Higgs field and explain the electroweak symmetry breaking. The initial ILC energy of 250 GeV will results in peak cross section for the reaction $e^+e^- \rightarrow Zh$ for the 125 GeV Higgs boson. The precision measurement of the rates of decay of the Higgs boson to the various types of quarks, leptons, and bosons will give evidence on whether the Higgs field operates alone to create the masses of these particles. The Higgs boson study can be extended by additional essential elements at higher energies. The process $e^+e^- \rightarrow t\bar{t}h$ will give the absolute normalization of the underlying Higgs coupling strengths at center-of-mass energy of 500 GeV, the target value of ILC. Raising the energy further will allow to make precise measurements of the Higgs boson coupling to top quarks and to determine the strength of the Higgs boson's nonlinear self-interaction. Since Higgs boson is responsible for particles masses, the coupling strength between Higgs and various particles should be proportional to their masses. The measurement of this strength can verify its relationship with particles masses, while the detailed study should provide enough information to distinguish the correct Higgs model.

The heaviest fundamental fermion observed by now, the top quark, affects the predictions of many SM parameters like Higgs mass and the W and Z bosons coupling. Since high mass of the top quark should result in especially strong coupling to the Higgs field, the detailed measurements of the electroweak couplings of the top quark should disclose the presence of composite structure in the Higgs particle. A crucial input to particle physics calculations can be provided by direct, high precision study of the top quark mass, possible at lepton colliders in direct measurements in contrast to hadron colliders, where systematic effects lower the measurement precision.

Table 1.1 give some examples of the ability of the lepton colliders to follow up the discovery of new particles with precision measurements of their properties. It becomes clear, mainly from astronomical measurements, that beside a visible matter, a major fraction of the matter in the universe is a dark matter. A charge-less, massive, Weakly Interacting Massive Particle (WIMP) χ, which interacts with approximately weak gauge force, seems to be ideal candidate as a base component of the dark matter. The searches for the dark matter at LHC as well as linear colliders are mostly based on a missing energy signature in cascade decays of parent particles. The missing energy should be taken away in such process by a stable dark matter particle being a one of decay products. However, this signature is strongly dependent on the theory parameters and its connection with the couplings of χ particle is very weak. More model-independent measurements could be possible via $f\bar{f} \rightarrow \chi\chi\gamma$ process, but the LHC experiments sensitivity to it is limited due to a large background. Since lepton colliders environment will be orders of magnitude clearer, the major properties of dark matter particle candidate can be revealed.

Aside the searches of dark matter, the linear colliders can reach Beyond Standard Model (BSM) and support the Supersymmetry (SUSY) theory. A many indications that the SM is not valid up to the Planck scale are well known, like the gauge hierarchy problem or the instability of the weak scale against quantum corrections to fundamental scalar fields. The SM, in fact, does not contain any explanation of Charge Parity (CP) violation and, therefore, does not describe the source of baryo-

genesis. In addition, the three gauge couplings of the SM do not unify when extrapolated to high energies and the quantum gravity is not incorporated into SM in any clear way. This results in major problems with extrapolation the SM to the very small distances and into Grand Unified Theory (GUT) scales. These problems can be addressed by the SUSY theory, a quantum spacetime symmetry which predicts a correspondence between bosonic and fermionic fields [10, 11]. SUSY provides a connection between the Standard Model and ideas of GUT as well as string theory, and provides a route to unification with gravity or supergravity theories. The precise study of many of properties, such as masses, spins and couplings to the SM particles, of new scalars and fermions predicted by the SUSY theory, should be possible at the future linear colliders. In addition, the lepton colliders may support the measurements of strongly interacting super-partner masses at LHC by providing the precise measurement of the electroweak super-partner masses. These combined results may verify the principles for SUSY breaking as well as provide the access to a high-scale (e.g. GUT) structure of the theory.

1.1.2 International Linear Collider (ILC)

The ILC project unites the efforts of many institutes around the world, focused on electron–positron linear accelerators design over the past two decades. The schematic view of the proposed layout of ILC is shown in Figure 1.1. The ILC is going to provide a 500 GeV center-of-mass energy together with high beam luminosity. An energy enlargement up to 1 TeV is also considered as a possible machine upgrade. The main accelerating part (main liniac for both, electrons and positrons) is based on 1.3 GHz Superconducting Radio Frequency (SCRF) accelerating cavities, the effect of a decade of pioneering work by the TESLA collaboration. The beam is produced in electron source, located on the positron side near the damping rings, by a laser illuminating a strained GaAs photocathode in a Direct Current (DC) gun, providing the necessary bunch train with 90 % polarization. The electron beam is then pre-accelerated to 76 MeV using normal conducting structures and provided to the main electron liniac which accelerates it up to 5 GeV. This beam is used for positron creation in positron source located at the end of main electron liniac. Accelerated electron beam is transported through a 147 m superconducting helical undulator generating photons with maximum energies in range 10 MeV up to 30 MeV, depending on the electron beam energy. Photons separated from electron

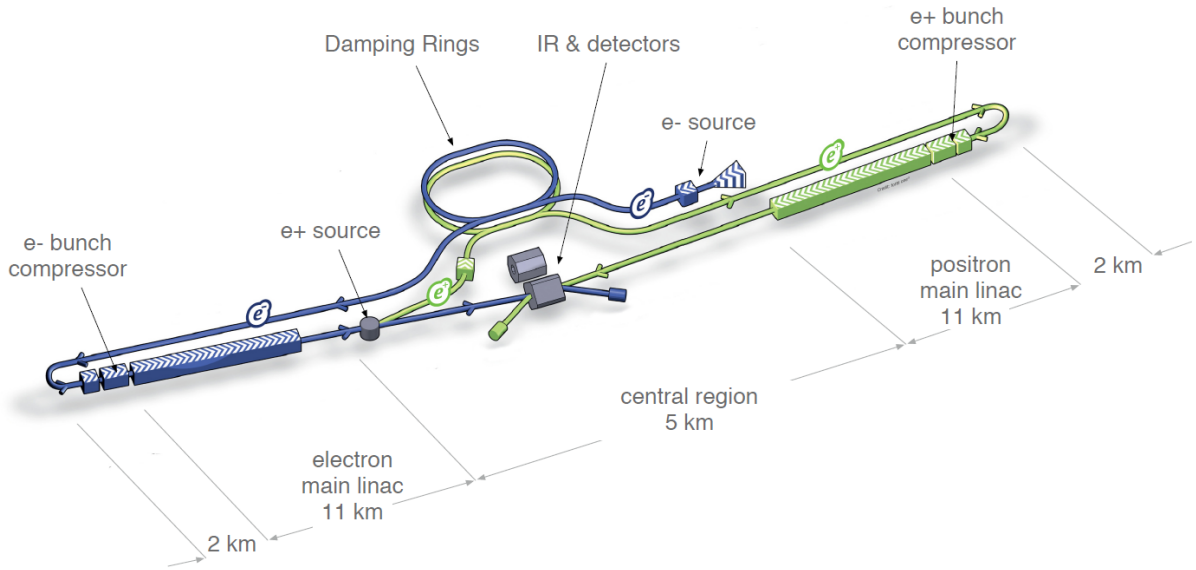


Figure 1.1: Schematic layout of the International Linear Collider (ILC) [9].

beam are directed onto a rotating Ti-alloy target, producing a beam of electron-positron pairs. This beam is accelerated to 125 MeV before electrons and remaining photons are separated and dumped. The pure positron beam is pre-accelerated to 400 MeV using normal conducting structures and, similarly to the electron beam, provided to the main liniac accelerating it to the energy of 5 GeV. Before injection the beams into the damping ring, superconducting solenoids rotate the spin vector into the vertical.

The aim of damping rings is to suppress the large transverse and longitudinal emittances of input particles to the low emittances required for luminosity production. Two rings, electron and positron one, are housed in a single tunnel located in the central region, horizontally offset from the interaction region by approximately 100 m to avoid the detector hall, with one ring positioned directly above the other. The superconducting Radio Frequency (RF) system is operated in Continuous–Wave (CW) mode at 650 MHz. The highly stable beam structure is formed in damping rings by both, suppressing the emittance as well as reducing the incoming beam jitter (transverse and longitudinal). Before extraction from damping rings, the polarization is rotated once again, from vertical to arbitrary chosen angle.

From the damping rings, the formed beams are transported through Ring to Main Liniac (RTML) system to the main liniacs. The RTML comprising a five subsystems: around 15 km long 5 GeV transport line, betatron and energy collimation systems, a 180° turn-around which enables feed-forward beam stabilization, spin rotators to orient the beam polarization to the desired direction, and a two-stage bunch compressor to compress the beam bunch length from several millimeters to a few hundred microns. The last one system includes the acceleration of particles, based on SCRF cavities same as used in the main liniac, from 5 GeV to 15 GeV in order to keep the increase in relative energy spread associated with bunch compression small. One of main targets for RTML system is to keep the beam low emittance achieved in damping rings along the whole road to the upstream end of liniacs.

The beam is accelerated from 15 GeV to the maximum energy of 250 GeV in two main liniacs, each one comprising approximately 7 400 one meter long superconducting niobium cavities. To achieve the target temperature of 2 K, the cavities are assembled into around 850 12.65 m long cryomodules. The RF power for accelerating cavities is provided by 1.3 GHz, 10 MW Multi-Beam

Parameter	Unit	Baseline 500 GeV Machine	1 TeV update
Center-of-mass energy	GeV	500	1000
Pulse rate	Hz	5	4
Bunch separation	ns	554	366
Pulse current	mA	5.8	7.6
Number of bunches per pulse		1312	2450
Particles per bunch		2×10^{10}	1.74×10^{10}
Luminosity	$cm^{-2}s^{-1}$	1.8×10^{34}	3.6×10^{34}
Luminosity (in 1% of energy)	$cm^{-2}s^{-1}$	1×10^{34}	2.1×10^{34}
Crossing angle at Interaction Point (IP)	mrad	14	14
RMS of beam size at IP (h × v)	nm	474 × 5.9	481 × 2.8
Main liniac average gradient	MV/m	31.5	38.2
RF frequency	GHz	1.3	1.3
Estimated AC Power consumption	MW	163	300

Table 1.2: Basic design parameters for ILC [9].

Klystrons (MBK), each driven by a 120 kV Marx modulator. The obtained average accelerating gradient of the cavities is around 31.5 MV/m with random cavity-to-cavity spread of ±20 %. At nominal beam current of 5.8 mA, the optimal loaded cavity quality factor Q_L corresponds to a cavity fill time of 925 μs, which combined with 727 μs beam pulse width results in total RF pulse time length of 1.65 ms.

After acceleration in main liniacs, the beam is transported to the IP and finally focused to meet the sizes required by the ILC luminosity goals by the Beam Delivery System (BDS). The beam halo from the liniac is also removed by this system to minimize background in detectors and all the key beam parameters, such as emittance, are measured and monitored. The single IP, with a 14 mrad total crossing angle provides space for separate extraction lines but requires crab cavities to rotate the bunches in the horizontal plane for effective head-on collisions. Two detectors in a push-pull configuration are located in a common interaction region around IP. After beams collision, the heavily disrupted beams are transported from the IP by the extraction line, part of the BDS, to main beam dumps.

The total length of the ILC for the standard 500 GeV center-of-mass energy is around 31 km. Extending the energy to the 1 TeV will result in an increase in length of the main liniac and RTML system by another 11 km each. The main parameters of the ILC accelerator are presented in Table 1.2.

1.1.3 Compact Linear Collider at CERN (CLIC)

Beside the ILC, the second lepton linear collider design, called CLIC, is currently developed by CERN. Its layout, shown in Figure 1.2, is in general quite similar to the one proposed for ILC. One of the main differences is almost three times higher accelerating gradient of around 100 MV/m, proposed in order to reach 3 GeV center-of-mass energy with similar total main liniac length as ILC. To achieve such high gradient with conventional accelerating mechanism, significantly higher frequency for RF main liniac system of 12 GHz needs to be used. The second difference between both designs

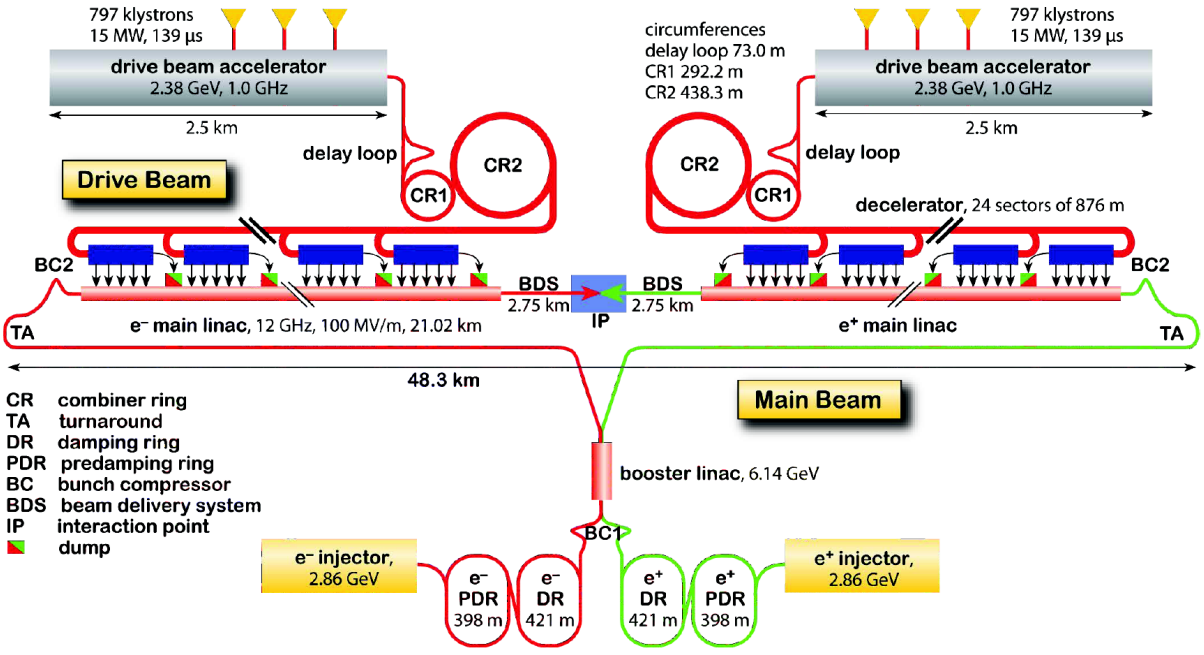


Figure 1.2: Schematic layout of the CLIC at 3 TeV center-of-mass energy [12].

is an innovative method for RF power generation for bunches acceleration foreseen for CLIC. The accelerating power is extracted by a specially designed decelerating structures from high-intensity, low-energy electron drive beams running in parallel to the main beam. This two beam concept allows to met extremely demanding RF peak-power requirement of 200 MW/m, needed to obtain high accelerating gradient. In addition, since the RF power is accumulated in the electron beam, it can be transported over long distances without significant losses. This novel method of main beam acceleration and higher accelerating gradient results in total length of the whole machine of around 48 km, 1.5 times more than ILC, for the center-of-mass energy of 3 TeV, six times higher than 500 GeV ILC energy. Since, in general, the machine is optimized for given center-of-mass energy, decreasing this energy (in order to address some of processes listed in Table 1.1) will result in the luminosity decrease. Moreover, at fixed machine design, the bunch charge have to be reduced with decreasing energy and the beam stability considerations induce even more limitations. Due to these reasons, a several stages before reaching the target 3 TeV center-of-mass energy are foreseen, allowing to operate the CLIC accelerator at 500 GeV, 1.5 TeV and, finally, 3 TeV with comparable for each stage, high beam luminosity. The main parameters for the two boundary center-of-mass energy values are listed in Table 1.3.

Parameter	Unit	Initial 500 GeV	Target 3 TeV
Center-of-mass energy	GeV	500	3000
Pulse rate	Hz	50	50
Bunch separation	ns	0.5	0.5
Number of bunches per pulse		354	312
Particles per bunch		6.8×10^9	3.7×10^9
Luminosity	$cm^{-2}s^{-1}$	2.3×10^{34}	5.9×10^{34}
Luminosity (in 1% of energy)	$cm^{-2}s^{-1}$	1.4×10^{34}	2×10^{34}
Crossing angle at IP	mrad	18.6	20
RMS of beam size at IP (h × v)	nm	202 × 2.3	45 × 1.0
Main liniac average gradient	MV/m	80	100
RF frequency	GHz	12	12
Estimated AC Power consumption	MW	271	582

Table 1.3: Basic design parameters for CLIC [12].

Another main difference between ILC and CLIC is the beam structure. At the ILC the separation between bunches is equal to 330 ns, leaving a lot of time for processing each bunch crossing separately without pile-ups. The 0.5 ns bunch separation at CLIC will result in significantly higher demands on the readout electronics. The CLIC detector system will have to handle with signals from particles generated in very frequent bunch crossings, requiring a time-tagging technique to relate the registered signals with particular collision. Since the pile-ups from subsequent bunch crossings are highly more probable at CLIC, the pile-up rejection capabilities of readout electronics is highly required. Due to the higher energy and smaller beam size, a more severe experimental background is expected at CLIC than at ILC. Despite these differences, the detector R&D currently carried out for the ILC are most relevant also for CLIC.

The CLIC beam pre-acceleration and delivery system is a little more elaborate than the ILC one, described in details in previous section, but the main idea remains unchanged. A separated electron and positrons sources are foreseen for CLIC in opposite to ILC. The CLIC polarized electron source consists of DC gun (a laser illuminating a strained GaAs photocathode), a 1 GHz bunching system, and a 2 GHz accelerator providing a 200 MeV pre-acceleration of electron beam before

injection into the common injector liniac. The electron source produces spin-polarized electrons with a degree of polarization as high as 80%. The positron source contains a typical electron DC gun and the primary liniac accelerating the electrons to the 5 GeV. Accelerated electrons are converted into photons on thin tungsten crystal target and directed onto amorphous tungsten target where positrons are generated in an electromagnetic shower. Analogously to the electron beam, the positron beam is pre-accelerated to 200 MeV. Both beams are provided to the common injector liniac accelerating it to 2.86 GeV and injected into pre-damping and damping ring complex. Similar to the ILC, the main purpose of the damping rings complex is to damp the incoming electron and positron beams to the very low emittances. From the damping rings the beam is transported and finally formed by a RTML system. It matches beam properties like bunch length and energy from the values delivered by the damping rings to the values required by the main liniacs. The particles are accelerated in booster liniac, part of the RTML, to the energy of 9 GeV. The booster liniac is shared between positrons and electrons since the two incoming bunch trains are shifted in time. After acceleration the beams are separated and transported through a 21 km long transfer lines to the upstream side of main liniacs. Before injections the bunches are finally compressed to their final length of 44 μm. The two main liniacs, identical for electrons and positrons, accelerate the beams to the final value of 1.5 TeV. Each liniac is around 21 km long, almost two times longer than ILC ones. The CLIC BDS system transports accelerated electron and positron bunches focusing them to the size required by CLIC luminosity and brings them to the collision at IP. The post-collision line from the IP to the main beam dump must transport both the un-collided beam as well as highly corrupted collided beam with its increased momentum spread and angular divergence. The post-collision line is also optimized to produce minimum losses, and thus minimum background contributions to the detector at the IP. The CLIC main dump is based on the ILC pressurized water beam dump.

The choice between the two proposed linear collider designs, the ILC and CLIC, will mainly base on the physics results obtained by the current LHC experiments. The discovery of Higgs boson with mass of 125 GeV suggests that the ILC can be a proper choice, especially in light of the severity of its R&D and availability of the selected technologies. On the other hand, researches targeted on new physics, such as SUSY, will require a center-of-mass energy around or above 1 TeV. For this case, the CLIC seems to be the only option right now.

1.2 Overview of the detector system

In order to accomplish the very reach physics program, the future linear collider detectors face challenges requiring significant advances in detector performance. The requirements for future detector system differ significantly from the current state-of-art systems developed for LHC experiments, since a substantially lower event rates, radiation doses and environment background are foreseen for future linear collider experiments. On the other hand, some of the physics processes described in section 1.1.1 require a very precise energy measurements and particle identification with track reconstruction (tracking), which leads to very high demands placed on the detector systems.

The future linear collider provides a wide range of physics capabilities, for which the detector systems have to be prepared, like Higgs Factory, Giga-Z, Top Yukawa couplings, di-boson production, SUSY and a majority of new physics of BSM processes [13]. Each of these processes makes its own set of requirements and the detector system should be capable to address all of them in general. Especially the new physics study is considerably focused on high multiplicity jet final states, multi-jet final states, missing energy signatures, heavy flavor production or exotic final states. Consequently, the calorimetry system must advance beyond the current state-of-art designs requiring a high granu-

larity particle flow calorimetry in opposite to separate energy and particle flows successfully used in the present collider experiments. A more precise detector will lower the systematic errors in many measurements, extending the new physics reach. It will also allow a more efficient usage of the luminosity provided by the collider, reducing the total operation time needed to obtain the demanded measurements accuracy.

The decay of short lived products of electron-positron collision results in high energy jets. Around 65 % of their energy is carried by charged particles, around 25 % by photons and remaining 10 % by a long-lived neutral hadrons. The tracks of charged particles, precisely measured by the tracker, are the base of Particle Flow reconstruction Algorithm (PFA) used for reconstruction of the four-vectors of all detectable particles. Separation of deposits from charged particles and those generated in the calorimeter by neutral particles (photons and neutral hadrons) results in a much better energy measurement of jets. A calorimetry system that is able to isolate and independently measure the energy deposits contribution from individual particles, will rise the overall precision of the system by enabling the combination of the energy deposits from neutral particles with the deposits from the charged ones measured by a tracker. Since the main limit for such system will arise from uncertainty distinction between particles in calorimetry, a high granularity of the electromagnetic and hadron calorimeters is strongly desirable. The detector system developed for the future linear collider together with a PFA should provide a precision of 3 to 4 percent for 100 GeV jets to allow the separation of W and Z bosons di-jet final states. The tracker system requirements are driven by a Higgs-strahlung process, one of the base processes for Higgs study, in which the recoiling Higgs is reconstructed from the associated Z boson decaying into a lepton pair. Since a very accurate charged track momentum resolution measurements are needed, a high field magnets together with high precision and low mass trackers are developed for future linear collider detector system. Beyond the significant majority of the detector system, a single exception to the low radiation doses and clean environment background assumptions appears in the very forward region. In this region calorimetry have to contend the high backgrounds primarily from the soft positron-electron pairs that are guided through the detector. A frequently bunch crossings, every few hundred nanoseconds at ILC and three orders of magnitude more frequent at CLIC, will result in a high radiation loads and complicate the very forward calorimeter design.

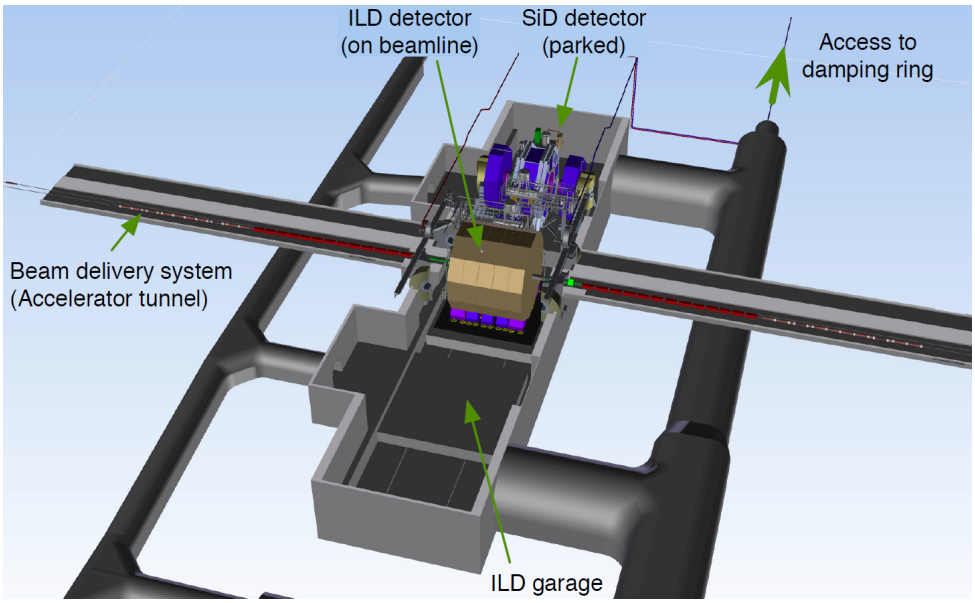
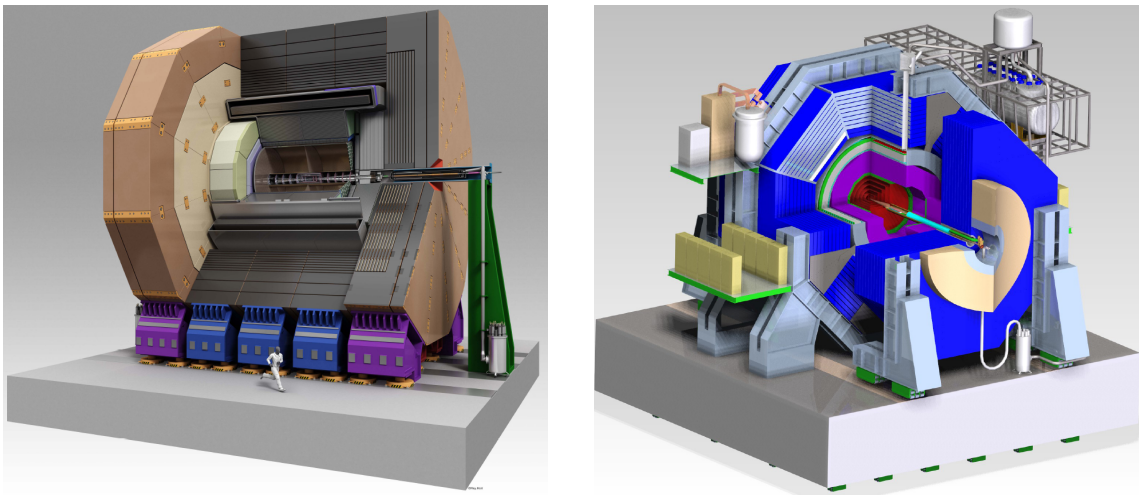


Figure 1.3: Example layout of the detector hall [9].

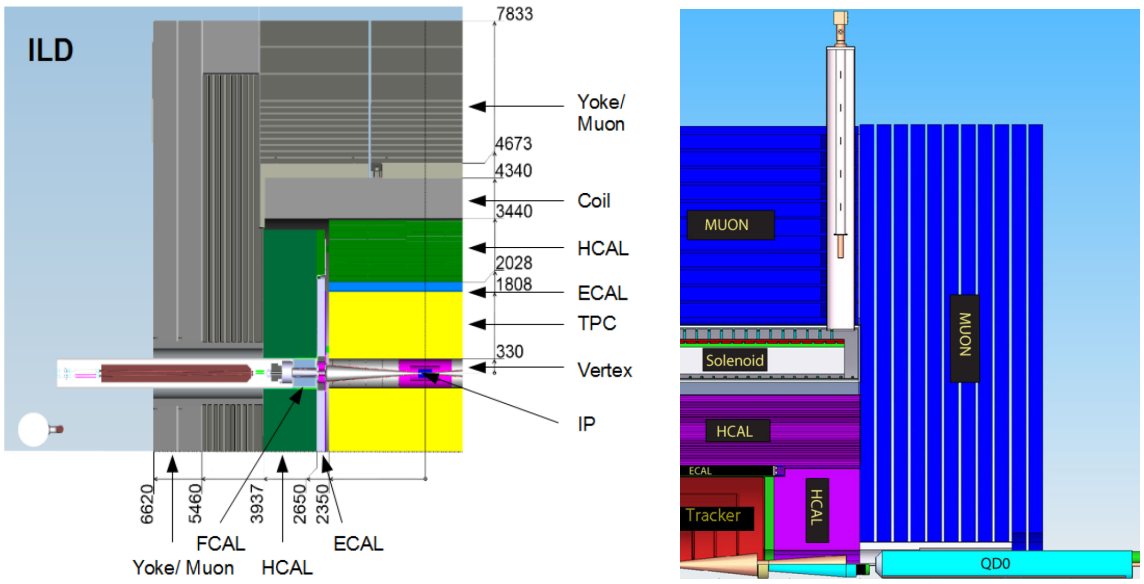
The scientific productivity of collider facilities, such as the Tevatron, LEP, HERA, and the LHC, has benefited from independent operation of multiple experiments. The independent designs and methodologies provide invaluable benefits from confirmation of results originating in these systems working in complementary conditions. A numerous historical examples where this complementarity was essential can be provided, therefore a multiple number of detector systems is predicted for the future linear collider. A circular layout of accelerator, such as LHC, allows to obtain a multiple IPs, while the linear collider design provide only a single one. Therefore a two detector system in a push-pull configuration, sharing the same IP region, is foreseen for the future linear collider. An example implementation of this system is shown in Figure 1.3. For the ILC, the two concepts of general purpose detector are currently under R&D: the International Large Detector (ILD) [14] and the Silicon Detector (SiD) [15]. An overview of both detectors is shown in Figure 1.4. Since the CLIC target center-of-mass energy is significantly higher than the ILC one, detector concepts developed for the ILC cannot be directly used. However, since the staged approach is foreseen for the CLIC development, the initial center-of-mass energy will be comparable to the ILC one, the minimum requirements for the CLIC detector system is the same as for the ILC. To allow the future energy upgrade, two detector systems derived from the ILC ones, the CLIC_ILD and CLIC_SiD, are under development for the CLIC [7].



a) ILD detector b) SiD detector

Figure 1.4: Overview of two detectors for future linear collider [9].

All four detectors, both for ILC and CLIC, utilize a very similar construction comprising a powerful pixel vertex detector, providing a high precision vertex reconstruction, a sophisticated tracking system optimized for both, track reconstruction efficiency and high momentum resolution, and a silicon-tungsten Electromagnetic Calorimeter (ECAL) and highly segmented Hadronic Calorimeter (HCAL). The quality of these two calorimeters is crucial for the physics measurements point of view, as it was discussed earlier. Both calorimeters are surrounded by solenoids providing a high (3–5 T) magnetic field. The most outer region of each detector is occupied by a muon system designed to identify muons from the interaction point with high efficiency and to reject almost all hadrons (primarily pions and kaons). The detail longitudinal cross sections of ILD and SiD are shown in Figure 1.5a and Figure 1.5b respectively. Since the design of all detectors is very similar, a detailed description is presented on the example of ILD detector. At last, but not least, the two specialized calorimeters, the Luminosity Calorimeter (LumiCal) and the Beam Calorimeter (BeamCal), are lo-



a) ILD detector b) SiD detector

Figure 1.5: Longitudinal cross section of two detectors for future linear collider [9].

cated in the very forward region of all detector systems. Since the development of the LumiCal calorimeter is a main subject of this dissertation, it will be described in details in Section 1.3.3.

The particle flow reconstruction algorithm, the PFA, results in a detector design with high demands on a topological reconstruction of events. A detector system which can separate efficiently charged and neutral particles, even inside jets, is needed to meet these requirements. To boost the spatial resolution of overall detector system, a highly granular calorimeter system is combined in ILD with an efficient and redundant central tracker. The whole system is immersed in a strong magnetic field of 3.5 T and surrounded by a muon detector and tail catcher calorimeter.

1.2.1 Vertex detectors

For the future linear collider physics program, an identification of heavy quarks and tau leptons, as well as reconstruction of decay vertices of short lived particles, such as D or B mesons, is crucial. The vertices are tracked back by reconstructing the trajectory of the short lived particles decay products. The required precision demands a primary and a secondary vertex reconstruction with very high spatial resolution together with minimum multiple scattering introduced by the detector itself. In addition, a full geometrical coverage extended to a low polar angles is required as well. To achieve the reconstruction resolution required by ILC physics program, the ILD vertex detector should meet the following specifications: spatial resolution near the IP should not be worse than 3 μm, material budget should remain below 0.15 % of radiation length per detector layer, first layer should be located at a radius of around 1.6 cm from the IP, pixel occupancy should not exceed a few percents, and power consumption should be minimized to reduce the material budget of the detector cooling system [13].

The Vertex Detector (VTX) is realized as a multi-layer pixel silicon detector. Its baseline design comprises a three concentric, nearly cylindrical layers of double-sided ladders. As an alternative solution, a five single-sided layers design is foreseen. In either case the detector has a pure barrel

geometry. To obtain the best secondary vertex reconstruction, the VTX has to be located in the center of experiment, as close as possible to the beam pipe. To minimize the occupancy from background hits, the first layer is only half as long as the remaining ones. Despite this, the innermost layer will be affected by radiation damages arising from the beam related background. An annual total ionizing dose of around 1 kGy and fluence of 10^{11} cm^{-2} equivalent neutrons are expected. Each ladder of the detector is equipped with thin (around 50 μm) pixel sensors. For the baseline design of three double-sided ladders, a six impact positions for each particle traversing the detector will be obtained. The three sensor technology options are currently under investigation for the VTX: the Complementary Metal-Oxide Semiconductor (CMOS) Pixel Sensors (CPS) [16, 17, 18], Fine Pixel Charge-Coupled Device (CCD) (FPCCD) [19, 20] and DEPleted Field Effect Transistor (DEPFET) [21, 22]. Although the detector technology has not yet been decided, the VTX is optimized for point resolution and minimum material thickness. The main VTX parameters like geometrical dimensions, spatial resolution and readout period are shown in Table 1.4.

Layer no.	Ladder no.	Radius R [mm]	Length $\lvert z\rvert$ [mm]	Polar angle coverage $\lvert\cos\Theta\rvert$	Spatial resolution σ [μm]	Readout period [μs]
1	1	16	62.5	0.97	2.8	50
	2	18	62.5	0.96	6	10
2	3	37	125	0.96	4	100
	4	39	125	0.95	4	100
3	5	58	125	0.91	4	100
	6	60	125	0.90	4	100

Table 1.4: Basic parameters for the VTX at ILD [13].

The design of VTX detector gives a lot of possibilities for future upgrades or replacements. With evolution of the sensors technologies, the performance of the detector can be efficiently increased. An upgrade of center-of-mass energy to 1 TeV will increase a radiation hardness demands, since the beam related background is expected to be significantly higher after collision energy upgrade. The ongoing sensor R&D concentrates also on improvement of readout speed in order to improve the reconstruction of low momentum tracks [13].

1.2.2 Tracking system

To provide a high resolution momentum measurements of charged particles, a very sophisticated tracking system is needed in both future linear colliders. It is especially crucial for the Higgs mass measurements based on Higgs-strahlung process. The precision of the lepton pair from the associated Z boson decay mass distribution measurement is, however, limited by a beam energy spread rather than detector performance. For this reason, the average momentum resolution should be at least $\sigma_{p_T}/p_T^2 \lesssim 5 \times 10^{-5}$ GeV^{-1} for ILC and $\sigma_{p_T}/p_T^2 \lesssim 2 \times 10^{-5}$ GeV^{-1} for CLIC.

The tracking system should cover the entire solid angle keeping the material budget as low as possible to avoid a multiple scattering affecting the momentum resolution, similarly to the VTX. A different approach for momentum measurements is foreseen for the two detector concepts. The Time Projection Chamber (TPC) together with supporting silicon strip and pixel detectors is developed for the ILD, while the SiD will utilize an entirely silicon detector. The TPC enables the continuous and highly redundant tracking with a very low material budget. In addition, an efficient particle dE/dx identification is possible using the TPC. On the other side, for the dense jets and high occupancy, the track recognition and separation is very difficult without any external information. To provide it, a

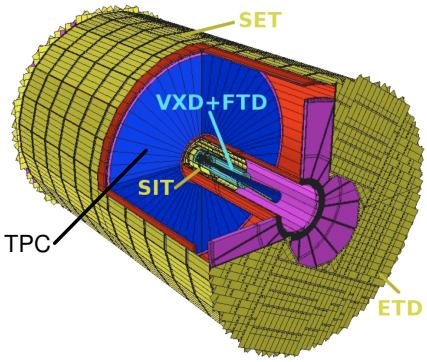


Figure 1.6: Overview of the ILD tracker detector system [13].

four detectors need to be added to the tracking system at ILD. The overview of the whole tracking system is shown in Figure 1.6. In the ILD barrel, two layers of silicon strip detectors are arranged as Silicon Inner Tracker (SIT) to bridge the gap between the VTX and the TPC. Outside the TPC next silicon strip detector systems are located: Silicon External Tracker (SET) at the periphery and End-cap of TPC Detector (ETD) at the end-caps. All three of them provide precise space points before and after the TPC, increasing the overall momentum resolution. In the forward region, a system of two silicon-pixel disks and five silicon-strip disks Forward Tracker Detector (FTD) provides low angle tracking coverage. The FTD is supported by a complementary silicon strip detector system SET placed between the TPC and the ECAL to provide additional high precision tracking. The main tracking system of the ILD detector is a large volume TPC with up to 224 points per track. The design of the TPC is optimized for 3-dimensional point resolution and minimum material budged. Since the whole tracking system is situated in strong magnetic field, a point resolution of better than 100 μm for the complete drift and a double hit resolution below 2 mm are obtainable. The mechanical design of the TPC comprise an end-plate supporting around 10^6 signal pads with readout electronics and a field-cage made from advanced composite materials to lower the overall material budget. The Micromegas and Gas Electron Multiplier (GEM) are considered as possible gas amplification systems, and both of them are under extensive and advanced tests.

In opposite to the TPC used in ILD, an all-silicon tracer is proposed for the SiD detector. The main benefits from silicon detectors compared to the TPC are time stamping capabilities due to fast charge collection time and very accurate space point resolution. This solution is also not subjected to the track recognition and separation for dense jets and high occupancy events. However, all of this is achieved at the expense of significantly higher material density. In addition, the redundancy and particle dE/dx recognition is strongly limited in a fully-silicon solution. The simulations and model tests show that both designs meet the ILC specifications while their complementarity can provide invaluable benefits from comparison of results obtained with two different approaches.

1.2.3 Calorimetry system

The both detectors predicted for future linear colliders, the ILD and SiD, are based on the Particle Flow reconstruction Algorithm (PFA) approach. The signatures of the multi-fermion final states are given by a few jets per each collision. Since these jets arise from the decay of heavy bosons, like W, Z and Higgs, they need to be precisely measured in order to reconstruct the decay channel. To optimize the jet energy measurement, the highly accurate data from the tracking system have to be combined with an information provided by the calorimetry system. The PFA requires the abil-

ity to identify individual particles in each jet, demanding from the calorimetry system a particular capability to distinguish between charged hadrons and photons depositions. To meet the Particle Flow reconstruction Algorithm (PFA) approach requirements, a two dedicated subsystems, an Electromagnetic Calorimeter (ECAL) and a Hadronic Calorimeter (HCAL), both with a fine segmentation, are mandatory. In the forward region of detector system additional two specialized electromagnetic calorimeters, the LumiCal and BeamCal, are foreseen. The purpose of these calorimeters is different than ECAL, since they should provide a beam luminosity measurements (LumiCal) and beam parameters monitoring needed for fast tuning (BeamCal), so they are not regarded as a part of the ECAL, although all three are based on the electromagnetic shower processes. The principia of this physical process are discussed in details in the following section.

Electromagnetic shower theory

The calorimetry aims in measurement of the total energy of the particle traversing the detector. To perform this type of measurement, the calorimeter should contain a material which fully absorbs the particles transforming its energy to a measurable quantity, such as charge deposition. The interaction of primary particle with the calorimeter's absorber results in a shower of secondary particles with gradually decreasing energy. The entire energy of the shower may be measured by its transformation to the measurable quantity, or it may be sampled. In the first approach the shower particles have to be absorbed by a material able to produce the signal proportional to the absorbed energy, e.g. a silicon sensors. For a TeV energy scale of primary particles, the total volume of silicon required for a full shower absorption is completely beyond considerable boundary, mainly due to the calorimeter size and cost. Therefore a sampling calorimeter, where the shower develops in a material that does not provide a readable signal, separated by a thin layers of active medium sampling the energy of shower particles, is mainly used. The longitudinal segmentation of the sampling calorimeter provides an additional information about the profile of the shower development, allowing the identification of the primary particle. The transverse segmentation enables the tracking abilities of calorimeter by providing the information about the direction of the primary particle derived from the shower transverse profile. Based on the type of measured particles, the calorimeters can be divided into hadronic and electromagnetic calorimeters. Since the second ones are based on electromagnetic interactions (mainly the bremsstrahlung and pair production) of primary particles, they are suitable for electrons, positrons and photons measurements.

The interactions between leptons and photons with an absorber material can be described on the example of lead absorber. The fractional energy lost in lead by electrons and positrons as a function of their energy is shown in Figure 1.7. The particular energy value, called a critical energy E_C, can be found in Figure 1.7 dividing the fractional energy lost into two regions. This energy is usually defined as an energy for which the energy loss due to ionization and bremsstrahlung, an electromagnetic radiation produced by decelerated charged particle, deflected usually by another charged particle (an electron or an atomic nucleus), processes are equal. Below the critical energy (of around 10 MeV for lead), the ionization dominates in the energy loss processes, although the scattering (Møller for electrons and Bhabha for positrons) and positron annihilation processes contribute as well. Above it, the electrons and positrons lose the energy mainly due to the bremsstrahlung process. At high energies, above 1 GeV, the energy loss becomes independent of the particles energy. A similar considerations can be provided for the photons: below the critical energy the energy losses are dominated by scattering (both Compton like Rayleigh), photoelectric effect and photo-nuclear absorption. In the energy range above the critical, the photons interact with matter mainly through the pair creation process.

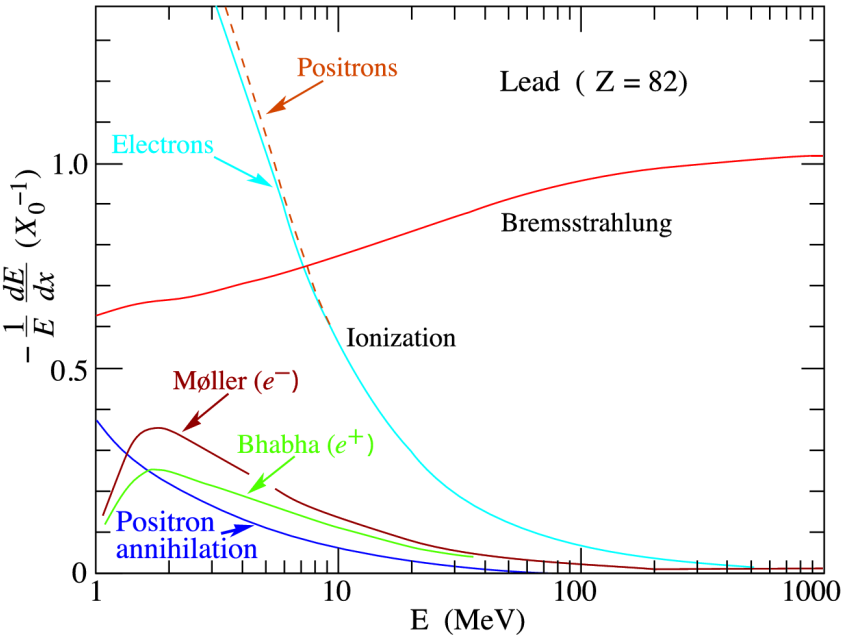


Figure 1.7: Fractional energy lost in lead by an electrons and positrons as a function of their energy [23].

The high energy primary particle (electron or positron) entering the calorimeter creates most likely the high energy photons by a bremsstrahlung process. These photons, through the pair creation process, produce the secondary electrons and positrons. This process repeats consecutively, resulting in exponentially increasing number of particles, until their energy drops below the critical energy. Since then the energy is dissipated mainly by ionization and excitation processes. The shower maximum, with the largest number of particles, is reached when the average energy per particle becomes low enough to stop further multiplication. From this point the shower decays slowly through ionization losses for electrons and positrons, or by Compton scattering for photons. The particular energy loss of high energy, electromagnetic-interacting particles allows to characterize the absorber material. The mean distance in absorber, over which an electron energy drops to $1/e$ of its initial value due to bremsstrahlung process, is called the radiation length X_0. A similar definition can be provided for a high-energy photons as a $7/9$ of the mean free path for pair production. Since the electromagnetic shower develops exponentially and depends on the energy of primary particle, the total length of the calorimeter required for the full absorption of the shower is proportional to the logarithm of the initial energy. For a material consisting of a single type of nuclei, the radiation length can be expressed as follows [24]:

$$X_0 = \frac{716.4A}{Z(Z+1)\ln\left(\frac{287}{\sqrt{Z}}\right)} \qquad \left[\frac{g}{cm^2}\right]. \tag{1.1}$$

Therefore, a high-Z materials should be used as an absorber to reduce the overall size of the calorimeter. In the sampling calorimeter, a thin active medium absorbs only a small amount of energy dissipated mainly in high-Z absorber. In order to determinate the total energy of particles, the integrated energy deposited in active material have to be multiplied by a calibration factor dependent on absorber material and overall calorimeter geometry.

The shower has been considered so far as a one dimensional process developing longitudinally in the calorimeter volume. Since the momentum of secondary particles is oriented almost in parallel with the primary particle, this approach is roughly correct. The typical angle of secondary particles

in electromagnetic shower is proportional to the ratio of their mass and energy. At an early stage of shower development, the typical angles are in order of milliradians while at the shower maximum, where the average particles energy is equal to the critical energy E_C, the shower becomes more isotropic, since the angels of particles are proportional to m_e/E_C. For example, the pair production angle in lead at shower maximum is about 4°. In fact, the dominating effect in transverse shower development is the multiple scattering of electrons and positrons. A characteristic energy E_S is defined for multiple scattering in relation to the electron mass and the electromagnetic coupling constant α as follows [25]:

$$E_S = \sqrt{\frac{4\pi}{\alpha}}\left(mc^2\right) \cong 21 \qquad [MeV]\,. \tag{1.2}$$

A characteristic constant R_M of a material giving the scale of the transverse dimension of the fully contained electromagnetic showers initiated by an incident high energy electron or photon is traditionally defined as [25]:

$$R_M = X_0 \frac{E_S}{E_C} \tag{1.3}$$

and called a Molière radius. On average, the 90 % of electromagnetic shower energy is contained inside the cylinder with radius R_M, and 95 % inside $2 \cdot R_M$. For most of materials, with typical ratio $A/Z \approx 2$, the Molière radius is fairly constant and equal to around 14 g/cm^2 [25].

Electromagnetic Calorimeter (ECAL)

The fundamental role of the ECAL is identification, and precise energy measurements of the photons, electrons, and positrons. To enable the accurate jet reconstruction, the ability to separate the deposits from individual primary particles and photons, and to distinguish between them and a nearby hadrons is obligatory. In addition, the early parts of showers initiated by hadrons should be also identified and measured. The separation between showers originating from very closely spaced primary particles requires a very fine segmentation. The ECAL provides up to 30 samples in depth and a small transverse cell size. The tungsten have been chosen as absorber, while the silicon sensors or scintillator strips are considered as active material. The SiD will utilize a non-magnetic tungsten alloy, with radiation length of 3.9 mm and Molière radius of 9.7 mm. The 30 layers are foreseen in total, first 20 with absorber thickness of 2.5 mm (0.64 X_0) and the last ten with thicker, 5 mm (1.3 X_0) absorber. In each layer a 1.25 mm gap is provided for the sensors. For the ILD a similar layout is predicted, aside pure tungsten, with radiation length of 3.5 mm and Molière radius of 9.0 mm, used as absorber. To keep the shower maximally contained, it is crucial to keep the distance between the tungsten absorber layers minimum possible. The effective Molière radius, taking into account the shower spreading, can be estimated using the factor expressed as the relative ratio of readout gap to the absorber thickness. For the crucial first 20 layers of ECAL in SiD, this factor can be calculated as $(2.50 + 1.25)/2.5 = 1.5$, resulting in effective Molière radius of 14 mm.

As the baseline design, silicon sensors segmented into hexagonal pixels are foreseen for the ECAL [13]. Each of the pixels is individually read out over the full range of charge depositions via a dedicated Application Specific Integrated Circuit (ASIC), KPiX for SiD and SKIROC for ILD. As an alternative option a sensitive layer based on scintillator strips coupled to the photon sensors could be used. Since an individual scintillator tile of size comparable to the silicon pixel size is very difficult from technological point of view, the two layers of scintillating strips, arranged in alternative directions, could be used. This approach, however, will complicate the shower reconstruction, in particular for dense jets case.

Hadronic Calorimeter (HCAL)

The main role of the HCAL is the measurement of the energy deposited by charged particles and the measurement of energy associated with neutral hadrons. Their contribution to the jet energy of around 10 % on average, fluctuates over a wide range from event to event. The accuracy of the measurement is the dominant contribution to the PFA resolution for jet energies up to about 100 GeV. The basic idea of hadronic calorimeter is similar to the electromagnetic one, although hadronic shower development is significantly more complex. The stainless steel is used as the absorber medium, allowing fine longitudinal sampling with a reasonable number of layers due to moderate ratio between the hadronic interaction length ($\lambda_I = 17$ cm) to the electromagnetic radiation length 1.8 cm. The mechanical properties of the steel are also important, since a self-supporting construction can be used resulting in more compact design without dead regions caused by auxiliary supports. Similarly to the ECAL, the HCAL requires a very fine longitudinal and transverse segmentation of active layers, for which two options are considered. One option uses scintillator tiles with transverse segmentation of 3×3 cm^2, read out by an analogue dedicated electronics based on a novel, multi-pixel Geiger mode silicon photo-diodes, so-called Silicon Photo Multipliers (SiPMs). The second uses a gas-based detectors called Resistive Plate Chamber (RPC), which allow a 1×1 cm^2 segmentation with a binary or semi-digital readout of each cell. The total volume of HCAL is in order of 10^2 m^3 with $4 \cdot 10^7$ number of readout channels in total.

1.2.4 Muon system

A stable, highly efficient muon identification system with excellent hadron rejection is an important requirement to meet the physics goals of the linear collider detector system. The muon system supplements the measurements taken with the tracker and the calorimetry system, identifying the muons and acting as a tail catcher. The second function is very important since it complements the calorimetry measurements recovering the energy leaking out of the calorimeter. For proper muon reconstruction, the tracks created in the inner systems have to be precisely connected with the ones from the muon system. The muon system is located in the outermost region of detector system, outside the magnetic field created by a solenoid placed between the HCAL and the yoke. An iron yoke, instrumented with scintillator strips or RPCs, returns the magnetic flux of the solenoid, and, at the same time, serves as a muon filter, a muon detector and a tail catcher calorimeter. The first section of the system provides ten relatively closely (around 14 cm) spaced layers, to act as a calorimeter for the tails. At the rear of the muon system, the distance between active layers increases up to 60 cm, since they only need to act as a muon tracker. As a sensitive layers, the scintillator strips equipped with wavelength shifting fibers, read out by SiPMs or RPCs, are foreseen. The active layers have the transverse segmentation of 40×30 mm^2 for the scintillator case and a single 1×2 m chambers with orthogonal readout strips for the RPC. Almost 99 % detection efficiency is predicted for isolated muons with energies greater than 7.5 GeV and polar angles above 10 mrad from the Monte Carlo (MC) simulations.

1.3 Forward region of International Large Detector (ILD)

The three specialized calorimeters, the Luminosity Calorimeter (LumiCal), Beam Calorimeter (BeamCal) and Luminosity Hadronic CALorimeter (LHCAL), are foreseen in the very forward region of the detector system. The BeamCal provides a fast estimation of beam luminosity and other beam pa-

rameters for the beam tuning instrumentation [26]. The main purpose of LumiCal is to accurately measure the beam luminosity which allows to reduce the systematic uncertainties in measurements of physical processes. The LHCAL is foreseen for the neutral hadrons luminosity measurement. In addition, all three detectors extend the acceptance range of the whole detector system to very small polar angles, i.e. significantly increase its hermeticity. Moreover, these three calorimeters provide an additional shielding for the inner tracker system from a back-scattered particles induced by collisions of beamstrahlung pairs with downstream machine instrumentation (beam pipe, magnets, etc.). The R&D and development of the forward region detectors for future linear collider is performed by a worldwide Forward CALorimetry (FCAL) collaboration. The author of this dissertation is also a member of this collaboration.

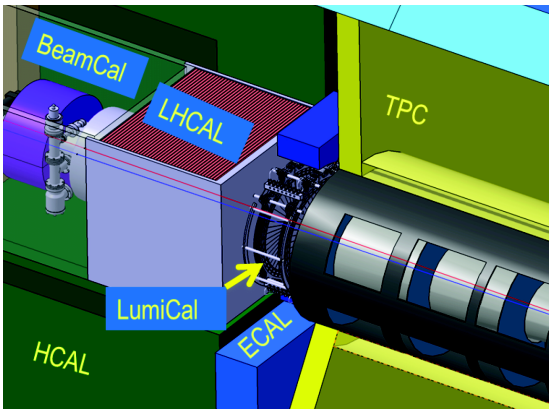


Figure 1.8: Very forward region of the ILD [13].

The very forward region of the ILD detector system is shown in Figure 1.8 with the IP located behind the right edge of the figure. Besides the three forward calorimeters, a part of tracking system, the TPC, as well as both main calorimeters, ECAL and HCAL, are shown. The study on LHCAL still remains in conceptual phase and no detailed implementation was proposed by now. Therefore, only the LumiCal and BeamCal designs will be discussed in details. Both calorimeters are a cylindrical sampling calorimeters, with a tungsten absorber and a semiconductor sensors as active layers. The calorimeters are centered on the outgoing beam on each side of IP to allow the precise measurement of the polar angle of scattered electrons. One should note that Figure 1.8 presents only one side of the detector system, which will be reflected on the opposite side of IP. To allow the installation around the beam pipe, both LumiCal and BeamCal are built as a two half-cylinders. The main geometrical parameters of both forward calorimeters in ILC and CLIC are shown in Table 1.5 and Table 1.6, for the LumiCal and BeamCal, respectively.

Collider	Geometrical acceptance [mrad]	Z location (start) [mm]	Numbers of layers (absorber + active)
ILC	31–77	2450	30
CLIC	38–110	2654	40

Table 1.5: Basic geometrical parameters for the LumiCal.

In both calorimeters an efficient electron and photon shower measurement is essential. Therefore, a small effective Molière radius is preferable for both designs. For the BeamCal, a small effective Molière radius enables the veto capabilities even at the small polar angles, while in the LumiCal it is essential for precise measurement of the shower development, necessary for the primary particle

Collider	Geometrical acceptance [mrad]	Z location (start) [mm]	Numbers of layers (absorber + active)
ILC	5–40	3600	30
CLIC	10–40	3281	40

Table 1.6: Basic geometrical parameters for the BeamCal.

polar angle reconstruction. As it was shown in section 1.2.3, the Molière radius of homogeneous tungsten alloy increases due to shower spreading in the readout gaps of sampling calorimeter. In order to keep the effective Molière radius as close as possible to the ideal one, possible only for fully homogeneous tungsten, the gap between absorber layers required for active medium should be minimized. The designs of both calorimeters utilize a 3.5 mm thick tungsten alloy absorbers, which corresponds to approximately one radiation length per absorber layer. A 1 mm readout gap for active sensors is foreseen. Since the Molière radius of the proposed homogeneous alloy is around 9.3 mm (depending on the exact alloy composition), the effective Molière radius, calculated using geometrical factor $(3.5 + 1.0)/3.5 \approx 1.29$, remains around 12 mm. For the ILC, both calorimeters are composed of 30 layers of absorber intersected by the sensors. Since at the CLIC the maximum beam energy is higher than the ILC one, the number of layers was increased to 40.

1.3.1 Principia of luminosity measurements

In HEP experiments, the energy available for the production of new particles is the most important parameter. The quantity that measures the ability of an accelerator to produce the required number of interactions is called luminosity $\mathscr{L}$. The luminosity is defined as a proportionality factor between the number of events per second dN_{ev}/dt created in particular physics process and the cross section σ of this process:

$$\frac{dN_{ev}}{dt} = \mathscr{L} \cdot \sigma \qquad \left[\frac{1}{cm^2 s}\right]. \tag{1.4}$$

The final figure-of-merit characterizing particular accelerator (e.g. provided in Tables 1.2 and 1.3), is so-called integrated luminosity $\mathscr{L}_{int}$, defined as:

$$\mathscr{L}_{int} = \int_0^T \mathscr{L}(\tau) d\tau \qquad \left[\frac{1}{cm^2}\right]. \tag{1.5}$$

This quantity is directly related to the total number of events N_{ev} observed in time T as follows:

$$N_{ev} = \mathscr{L}_{int} \cdot \sigma. \tag{1.6}$$

The accelerator luminosity is related to the beam parameters. As an example of this relation, a formula based on the TESLA accelerator study can be presented [27]:

$$\mathscr{L} = \frac{1}{4\pi r_e^{3/2}} \frac{P_b}{E_{cm}} \left(\frac{\pi \delta_E}{\gamma \epsilon_y}\right)^{1/2} H_D, \tag{1.7}$$

where P_b is total power of both colliding beams, E_{cm} – their center-of-mass energy, r_e is classical radius of electron, γ is relativistic Lorentz factor and ϵ_y is normalized transverse emittance. The δ_E represents the spread in collision energy introduced by beamstrahlung, and H_D, represents the enhancement of the luminosity due to the pinch effect.

Pinch effect and beamstrahlung

As can be seen from equation 1.7, the luminosity is directly proportional to the total power of colliding beams and inversely to the center-of-mass energy. To maintain the high luminosity with increasing energy, the bunch population and, as a result, the overall bunch charge have to be also increased in future linear collider designs. Moreover, the bunch size should be also minimized in order to increase the luminosity. These two effects, increased bunch population and decreased size, introduce a strong beam-beam interactions near IP [28, 29, 30].

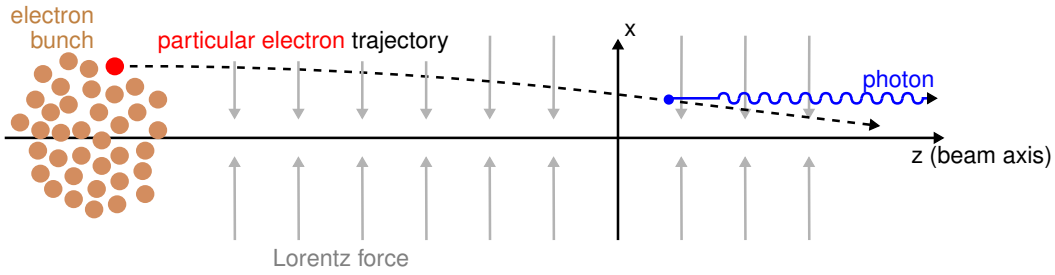


Figure 1.9: Schematic of pinch effect and beamstrahlung [31].

Since the electric charge of incoming bunches is opposite (as one contains electrons and the second – positrons), when the bunches approach each other in the IP, electric charges are approximately compensated. Therefore, the induced electric field is roughly canceled, but the magnetic fields sums up since the beams directions are opposite. This magnetic field introduces a strong Lorentz force onto ongoing particles perpendicular to the beam axis, as can be seen in Figure 1.9 for arbitrary chosen electron. For uniformly distributed charge densities, the Lorenz force is proportional to the distance of the particle from the beam axis. This results in bunch compression in the perpendicular to the beam axis z plane xy, the so-called pinch effect, since all particles located away from the beam axis are deflected to it.

Since the deflection process is equivalent to the radial acceleration of charged particle, the synchrotron radiation process takes place in parallel to the pinch effect. Since the bunch particles radiate photons mostly collinearly to the beam axis, and the radiation is forced by a self-induced magnetic field (unlike the classical synchrotron radiation, where an external magnetic field is provided), this phenomenon is called a beamstrahlung. The photons created in this process are generating electron-positron pairs in the strong electromagnetic field of the bunches. The coherent pair creation, caused by interaction of beamstrahlung photons with a collective electromagnetic field of the opposite beam, increases the overall number of colliding particles. The interaction of photons with the individual particles results in incoherent pair creation. Although most of the pairs are produced at an angle below 10 mrad, respectively to the beam axis, a fraction of particles created in incoherent process may reach beyond the beam pipe becoming a possible source of detector background.

Bhabha scattering

The luminosity $\mathscr{L}$ in an accelerator can be estimated using formula 1.7. However, due to energy spread of the beams, continuous beam tuning as well as beam-beam effects, the precise calculations of the differential luminosity for each bunch crossing can be very difficult, if possible at all. While the beam energy spread can be measured by a dedicated calorimeter located upstream the IP, the energy loss due to beamstrahlung, determining exact value of the luminosity at the IP, can be calculated from the beam parameters only by a Quantum ElectroDynamics (QED). These parameters, such as beams

relative positions offset, angular rotation and the particles distribution in a bunch are continuously changing due to beam tuning, and cannot be directly measured. The exact value of luminosity allows to calculate the physical process cross section σ from the measured number of its occurrences N_{ev}. Therefore, any uncertainty in the luminosity increases the systematic error of all measurements of physical processes, so the luminosity have to be precisely measured.

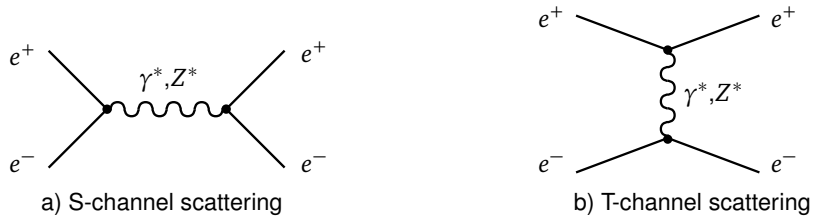


Figure 1.10: Feynman diagrams of an elastic Bhabha scattering.

To measure the luminosity $\mathscr{L}$, the method for determining the cross section of a studied physical process can be reversed, i.e. a number of occurrences of well-understood phenomenon, for which the cross section is well-known and precisely calculated, can be measured to enable the accurate luminosity calculation from equation 1.6. For electron-positron colliders, an elastic Bhabha scattering $e^-e^+ \rightarrow e^-e^+$ was chosen as a gauge process of luminosity measurements. The Feynman diagrams of this process are shown in Figure 1.10. The differential cross section $d\sigma_B/d\theta$ of Bhabha scattering is precisely calculated from theory [32, 33, 34, 35] and can be expressed as follows:

$$\frac{d\sigma_B}{d\theta} = \frac{2\pi\alpha_{em}^2}{s}\frac{\sin\theta}{sin^4\left(\frac{\theta}{2}\right)} \approx \frac{32\pi\alpha_{em}^2}{s}\frac{1}{\theta^3}, \tag{1.8}$$

where α_{em} is a fine-structure constant and θ is a polar angle of the scattered electron respectively to beam axis. For a fixed θ range, the differential cross section can be integrated as follows:

$$\sigma_B = \int_{\theta_{min}}^{\theta_{max}} \frac{d\sigma_B}{d\theta} d\theta \approx \frac{\pi\alpha_{em}^2}{s}\frac{1}{\theta_{min}^2}, \tag{1.9}$$

where final approximation was derived by neglecting the θ_{max} dependence. Hence, the integrated luminosity $\mathscr{L}_{int}$ can be calculated from the number of detected Bhabha events N_B as:

$$\mathscr{L}_{int} = \frac{N_B}{\sigma_B}. \tag{1.10}$$

As can be seen from formula 1.8, the cross section for Bhabha scattering is inversely proportional to θ^3. The shower development reconstruction precision requirement is therefore driven by this dependence.

1.3.2 Overview of Beam Calorimeter (BeamCal)

As it was described in section 1.3.1, for a high energy lepton beams the photons are created in a beamstrahlung process. A fraction of these photons creates a low energy electron-positron pairs in the electromagnetic field induced by a beam current density. Some of these pairs, transported outside the beam pipe, will deposit their energy in the BeamCal, the beam monitoring calorimeter.

The spatial distribution of these pairs can be used to estimate the beam parameters for every bunch crossing. In addition, a rough assessment of beam luminosity is also possible from this process. The equally important role of the BeamCal is to provide the veto mechanism for a new physics searches by a high energy electrons detection at the very small polar angles.

To fully meet the objectives, the minimum polar angle θ_{min} of the BeamCal acceptance range has to be minimized. However, this means that a large energy depositions, especially in the region located close to the beam pipe (at lowest polar angles), are foreseen. These depositions lead to huge radiation doses, in order of 1 MGy and fluence 0.4×10^{12} neutrons per mm^2 per year. Therefore, a radiation hard sensors are strongly required for the BeamCal. Several sensor materials have been studied by FCAL collaboration with irradiations performed using a 10 MeV electron beam at the S-DALINAC accelerator [36] with the dose rate varied between 20 and 200 kGy/h. As a possible candidate, the Chemical Vapor Deposition (CVD) diamond sensors, capable to operate properly up to 7 MGy of radiation dose, were proposed [37]. However, due to the overall cost of large area CVD sensors, a GaAs sensors can be used in the outer regions [38], where the expected radiation doses are substantially lower. The GaAs sensors radiation hardness up to 1.2 MGy was confirmed [39].

As the transverse segmentation of the BeamCal sensors, the 8×8 mm^2 pads were proposed, resulting in maximum electron detection efficiency. Due to the large occupancy expected for the BeamCal, each sensor has to be read out after each bunch crossing to avoid the pile-ups. A BeamCal dedicated ASIC [40] is under development.

1.3.3 Overview of Luminosity Calorimeter (LumiCal)

The luminosity calorimeter, LumiCal, is developed for precise luminosity measurements through the Bhabha elastic scattering as a gauge process. The experimental signature of the Bhabha event is a coincidence of scattered electron and positron, with energies larger than 0.8 of nominal beam energy, in back-to-back topology, as it is schematically shown in Figure 1.11. The showers developed by coinciding particles have to be fully contained within the acceptance volume of the calorimeter, which allows to reconstruct primary electron (positron) energy. The relative reconstruction accuracy better than 10^{-3} is required at a nominal 500 GeV center-of-mass energy, while the possible upgrade to 1 TeV will tighten this requirement to 10^{-4}. Since the uncertainties are determined by the measurements at the lowest polar angles, a highly precise design is required for the LumiCal. The LumiCal energy resolution σ_E/E can be expressed as:

$$\frac{\sigma_E}{E} = \frac{a_{res}}{\sqrt{E_{beam}}}, \tag{1.11}$$

where E is a most probable value of the deposited energy distribution, with standard deviation given by σ_E, for beam of electrons with energy E_{beam} and $a_{res} = (0.21 \pm 0.02)\ \sqrt{\text{GeV}}$ [13].

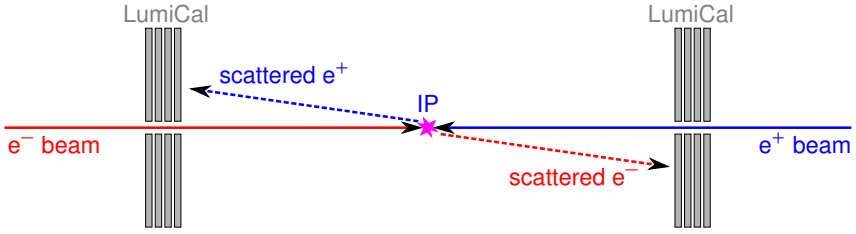
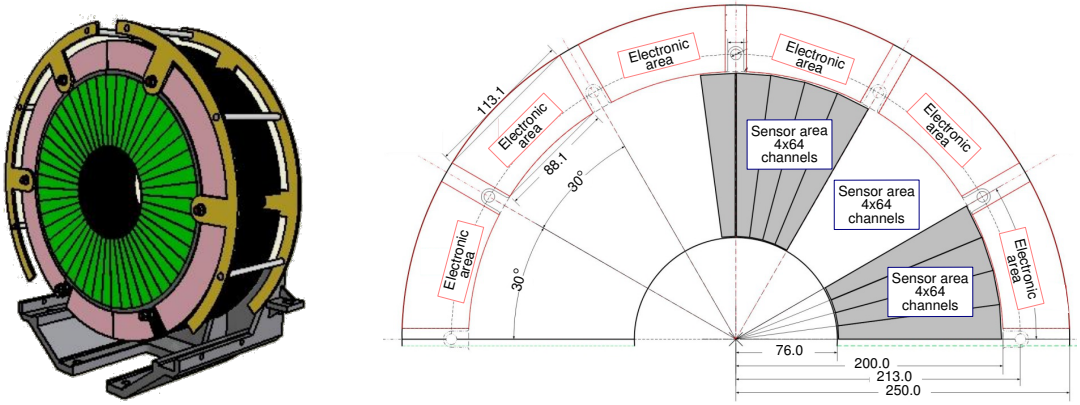


Figure 1.11: Simplified diagram of coincidence between scattered particles in Bhabha event detection.



a) Overview of the LumiCal barrel

b) Half-plane layout of the LumiCal layer

Figure 1.12: Schematic drawings of the LumiCal detector at the ILC [41, 42].

The overview of mechanical structure of the LumiCal barrel, proposed for the ILC, is shown in Figure 1.12a [41]. The detector is composed of 30 layers of tungsten alloy absorber intersected by active silicon sensors. The mechanical support is provided by a steel rods. The half-plane layout of a single LumiCal layer is shown in Figure 1.12b [42]. To provide a required spatial resolution, a single layer contains 12 sensor tiles, each divided into 4 azimuthal sectors. Thus each layer comprises 48 sectors, each divided radially into 64 pads. Prototypes of LumiCal n-type silicon, 320 μm thick, sensors have been designed and manufactured by Hamamatsu Photonics. The photograph of the silicon sensor is presented in Figure 1.13a. This segmentation results in 3072 channels per each layer and 92,160 channels in entire barrel. The CLIC design comprising 40, instead of 30, layers will increase this number up to 122,880. The sensor pad size was chosen to obtain sufficient polar angle resolution and to keep the polar angle measurement bias small for fully contained electron shower.

a) Silicon sensor tile

b) Sensor with a kapton fanout, mounted on a prototype Printed Circuit Board (PCB)

Figure 1.13: Photographs of a LumiCal sensor comprising 4 azimuthal segments, 64 radial pads each.

The expected charge deposition ranges from 4 fC, related to Minimum Ionizing Particle (MIP) depositions, up to 6000 fC, estimated for electromagnetic showers generated by 250 GeV electrons [43]. The radial pitch of sensors pads is 1.8 mm with 0.1 mm gap. Due to large spread of pads angular length, the pads capacitance varies from 8 pF, for the innermost, up to 25 pF for the outermost ones [44]. The signals from sensors, mounted on the tungsten absorber, are coupled to the front-end electronics via kapton fanout, shown in Figure 1.13b. The readout electronics is located at the outer region of the barrel, as shown in Figure 1.12b. To maintain the large number of readout channels, a dedicated multichannel ASICs are needed to process the signals from silicon sensors.

The developing shower is sampled in each active sensor layer. The energy deposited in each individual pad is recorded by the readout electronics allowing to reconstruct the shower and, finally, the energy and polar angle of the primary particle. To determinate this angle, the direction of shower development has to be reconstructed from individual depositions. The shower polar angle $< \theta >$ in each plane can be calculated using the pads polar angles θ_i and a weights W_i as [43]:

$$< \theta >= \frac{\sum_i \theta_i \cdot W_i}{\sum_i W_i} . \tag{1.12}$$

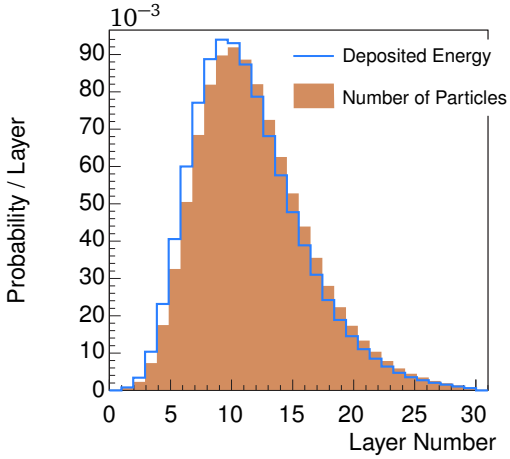
Using the reconstructed total shower energy E_{tot}, the weight W_i of a particular pad can be calculated from its energy E_i deposition as:

$$W_i = max\left\{0, \xi + \ln\left(\frac{E_i}{E_{tot}}\right)\right\}, \tag{1.13}$$

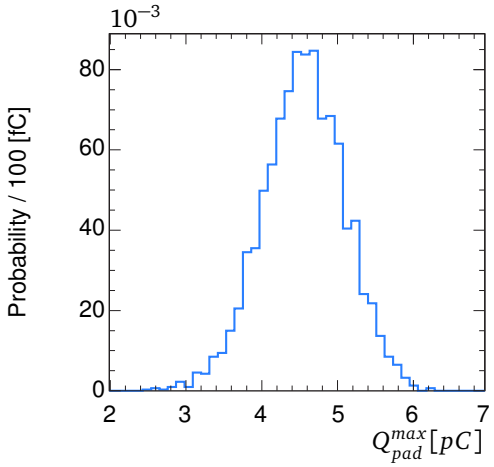
where ξ is a free parameter [45]. The first function of this parameter, is to define a threshold on the fraction of the total shower energy which has to be exceeded in order to include the pad in the position weighting. Secondly, this parameter sets the relative importance of the tails of the shower in the position weighting. Since, as the signature of Bhabha event, the coincidence between two tracks in two LumiCal barrels located at opposite sides of IP has to be found, their mutual position have to be very precisely controlled. The uncertainties of distance between the two barrels and their position with respect to the beam axis should be lower than 500 μm. Keeping in mind that the distance between the two barrels is equal to 4,900 mm at ILC, a precision of 0.01 % is required. Therefore, a dedicated laser-based positioning system is required.

The proposed LumiCal design was implemented and simulated using the GEANT4 simulations framework in order to optimize the detector geometry [26, 46]. The two normalized distributions for shower development simulated for the 250 GeV primary electrons are shown in Figure 1.14a. The first distribution in Figure 1.14a presents the overall energy deposited in each layer while the second – the number of shower particles. The maximum of both distributions is located around the 10th layer and almost all the energy of the primary particle is absorbed in the detector comprising 30 absorber layers. The normalized probability distribution of maximum charge Q_{pad}^{max} collected in a single pad for a 250 GeV electrons shower is shown in Figure 1.14b. The maximum of the distribution slightly exceeds 6 pC, while the 95 % of distribution remains below 5.4 pC. The most probable value of the maximum charge deposit is around 4.7 pC.

Although the expected occurrences are smaller than the ones foreseen for the BeamCal, a dedicated readout electronics capable to read all channels after each bunch crossing, in order to avoid the pile-ups, is needed for the LumiCal. The development of a dedicated ASIC, as well as the testbeam verification of the whole readout system, is the main subject of this dissertation.



a) Normalized distributions of the number of shower particles and of the energy deposited in the silicon sensors of LumiCal as a function of the layer for primary electron energy of 250 GeV



b) Normalized distribution of the maximum charge collected in a single pad per shower, Q_{pad}^{max}, for 250 GeV electron showers

Figure 1.14: MC simulations of shower development in LumiCal [47, 26].

1.4 Development of the LumiCal readout system

In order to meet the LumiCal and BeamCal readout requirements, a system capable to read individually each channel between subsequent bunch crossings is needed. Since the total number of channels in LumiCal for ILD reaches 10^5 per barrel, both the area occupied by the readout electronics as well as its power consumption have to be reduced as much as possible. Therefore, a dedicated ASIC, comprising a complete analogue readout together with a digitizer and some key Digital Signal Processing (DSP) components, has to be designed, verified, and tested. Also, a dedicated Printed Circuit Board (PCB) comprising all necessary sub-circuits required by the ASICs, a complete Data Acquisition System (DAQ) and a back-end software, has to be developed, verified, and tested. The whole process of development of detector readout can, and even has to, be divided into phases which will allow to test extensively each of the readout component as well as to simplify the design process. As a first phase of the development of the considered LumiCal detector readout system, a single readout plane was designed and extensively tested [48] as it is described in details in this section. Taking a step forward, the multi-plane (four) detector prototype was prepared, utilizing the existing single-plane modules, and tested. The multi-plane prototype setup and its testbeam results are presented in details in chapter 2. Since the main purpose of the existing detector readout module was proving the basic assumptions and widely testing the first ASIC generation in a single-plane mode, it introduced a significant limitations for the multi-plane detector module.

1.4.1 LumiCal readout architecture

The proposed LumiCal spectrometric readout chain, presented in Figure 1.15, comprises a silicon radiation sensor, a fast front-end (a charge preamplifier followed by a signal conditioning circuit - a shaper), a 10-bit Analog-to-Digital Converter (ADC) and a DSP block. In the existing readout module, these functionalities are distributed between two prototype ASICs, designed and fabricated in the AMS 350 nm technology, and an on-board Field-Programmable Gate Array (FPGA), the part of the DAQ system. The front-end ASIC [49] comprises the charge preamplifier and the shaper

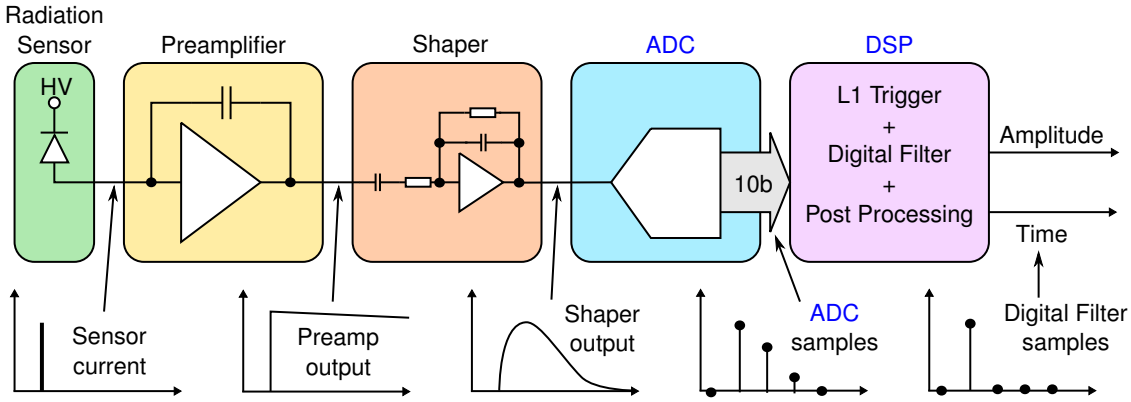


Figure 1.15: Block diagram of the proposed LumiCal readout chain.

circuit. The analog-to-digital conversion is provided by the 10-bit pipeline ADC [50]. The FPGA-based embedded system provides a primary DSP functionality enabling the data selection by a first-level trigger (external or internally event-driven), the data serialization and transmission. The data post-processing (pedestal subtraction, Common Mode Subtraction (CMS)) as well as deconvolution process are done off-line by a dedicated software, described in Section 2.2.

Silicon radiation sensors

The radiation sensors allow to detect the charged particles by absorbing and converting their energy into electric signal which can be read and precisely measured. A moderately relativistic charged particles traversing the silicon sensor lose energy primarily by ionization process, creating the electron-hole pairs. The mean rate of energy loss due to the interactions in a medium with thickness δx is called the stopping power (dE/dx)δx and can be derived from a relativistic version of Bethe-Bloch equation [51]. The behavior of electrons inside the sensor volume is quite complicated to describe because of quantum mechanical interferences with final state electrons. However, their properties in general are similar to other charged particles. The stopping power (-dE/dx) for electrons in silicon in function of their momentum is shown in Figure 1.16. The electron with kinetic energy slightly higher than 1 MeV, for which the stopping power reaches the minimum value of around 15 MeV per radiation length, is called the Minimum Ionizing Particle (MIP). For higher energies the energy

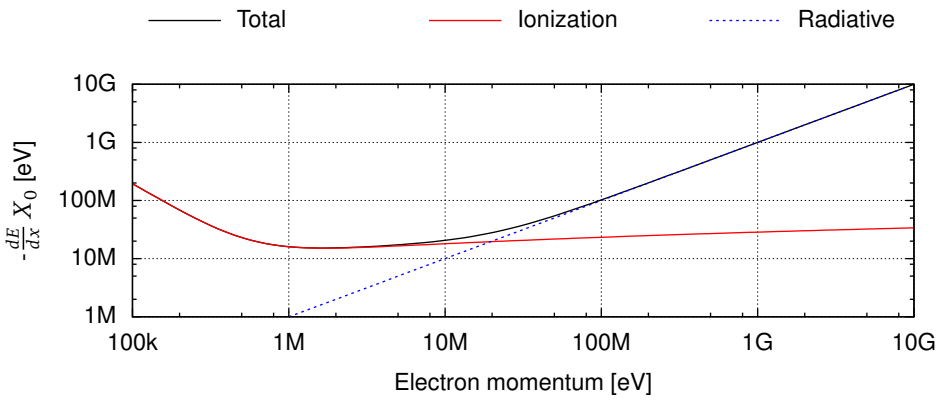


Figure 1.16: Stopping power (-dE/dx) for electrons in silicon [52].

dependence is very weak and reaches around 30 MeV per radiation length for very high energy electrons.

Since the ionization process has a statistical nature, the total energy loss ΔE of charged particle traversing the sensor volume fluctuates. Since the average number of electron-hole pairs N can be expressed as:

$$N = \frac{\Delta E}{P}, \tag{1.14}$$

this number also fluctuates. The proportionality factor P, equals 3.68 eV for silicon [53], is assumed to be constant for a given material, although this assumption was never proven theoretically. The energy loss distribution f(ΔE), also called the straggling function, for a finite silicon thickness, is given by the Landau distribution [54] as follows:

$$\begin{gathered} f(\Delta E, d_s) = \frac{1}{\xi}\varphi(\lambda), \\ \varphi(\lambda) = \frac{1}{2\pi i}\int_{-\infty}^{+\infty} e^{u\ln u+\lambda u}du, \quad \xi = \frac{z^2e^2}{2r_e\beta^2}\frac{N_A}{A}\rho Z d_s, \quad \lambda = \Delta E - \xi(\ln\xi + 1 - \gamma_E), \end{gathered} \tag{1.15}$$

where γ_E is Euler constant and ξ is average energy loss of a particle of energy E_0 penetrating an absorber of thickness d_s. For a thick sensor, this distribution approaches Gaussian distribution. For finite silicon thickness, a small number of collisions with high energy transfers results in large fluctuations skewing the distribution toward higher values. Some more improved distributions were proposed by Vavilov [55] and Bichsel [53]. Since the signal from silicon sensor is processed by the readout electronics, the noise introduced by it has to be also taken into account. All these corrections results in observed energy spectrum which can be represented as a convolution of Landau and normal distributions. It has to be noted, that the number of electron-hole pairs created in silicon sensor and, hence, the signal depends on the energy deposited in sensor volume, and not on the energy lost by the charged particle. As can be seen from Figure 1.16, the radiation losses come along with ionization. The photons created in beamstrahlung processes can leave the sensor material without any interaction, carrying out some part of energy. Also the secondary δ electrons, created from the interactions of primary particle, can leave the sensor. Due to the energy carried out by secondary particles, the energy deposited in the sensor material is smaller than the energy lost by the primary particle. The detailed MC simulations of energy deposition for 500 GeV electrons (treated as MIPs) in 300 μm thick silicon sensor give the Most Probable Value (MPV) of the distribution of around 4.1fC [46].

The operation of silicon sensors (like other ionization sensors) is based on the movement of free charge (electron and holes) created in ionization processes. In order to avoid immediate recombination of created carriers, a sufficiently high electric field is usually applied across the sensor volume. The silicon sensors in general utilize a reversely biased p^+-n junction creating a semiconductor diode junction. The electric field generated by a voltage source (HV in Figure 1.15) creates the depletion (mobile charge carrier-free) zone across the whole sensor volume. The charge carriers created in ionization processes drift in electric field towards the biasing electrodes causing a current signal received by the charge preamplifier of the front-end electronics. The simplified model of sensor and preamplifier is presented in Figure 1.17. Since the depleted region between the top and bottom contacts is mobile charge carrier-free, it forms a capacitor with capacitance approximated by following formula [56]:

$$C_{det} = A_J\sqrt{\frac{\epsilon\epsilon_0 eN_d}{2(V_{build}+V_{HV})}}\ , \tag{1.16}$$

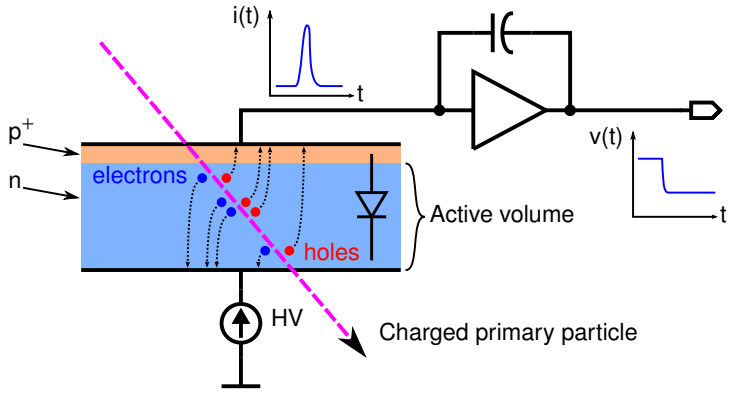


Figure 1.17: Simplified model of silicon radiation sensor and amplifier.

where N_d is donor doping concentrations, V_{build} is built-in voltage, V_{HV} is external bias voltage, A_J is junction area, ϵ_0 is vacuum dielectric constant, ϵ is silicon dielectric constant, and e is electron charge. The formula 1.16 is derived for highly asymmetrical junction, as shown in Figure 1.17. The thickness of depletion zone depends on the value of external bias voltage V_{HV}. In order to extend this zone to the whole silicon sensor volume, the bias voltage has to be at least equal to the, so called, full depletion voltage V_{dep}. For sensor thickness w, this voltage can be expressed as [56]:

$$V_{dep} = \frac{qN_d w^2}{2\epsilon\epsilon_0} \quad . \tag{1.17}$$

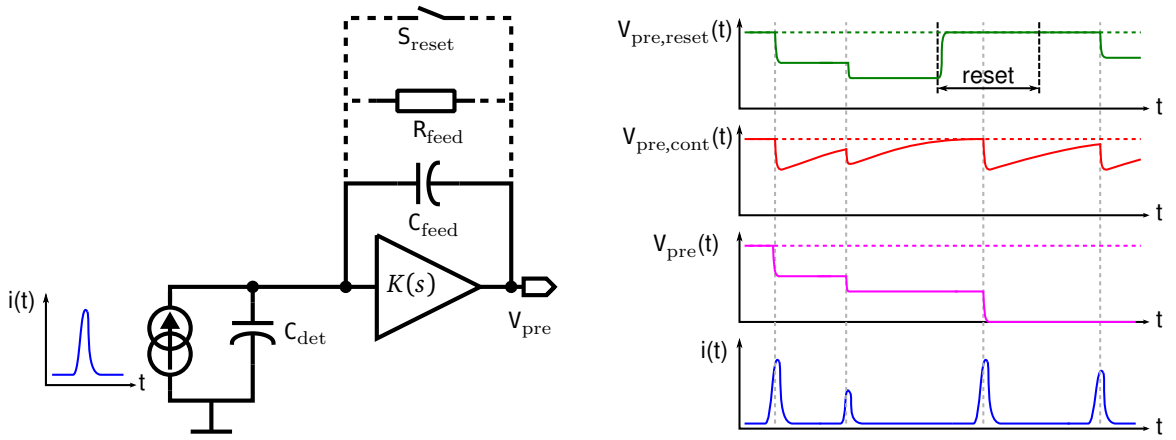
Under the condition of $V_{HV} \geq V_{dep}$, the junction capacitance depends only on its geometrical dimensions – thickness w and area A_J as follows:

$$C_{det} = A_J \frac{\epsilon\epsilon_0}{w} \quad . \tag{1.18}$$

The movement of the generated charge carriers inside the sensor volume induces a current $i(t)$. Its exact value can be determined from the Ramo theorem [57, 58]. The shape, maximum value and duration of current pulse depend on particle type, its trajectory inside the active volume and distribution of generated charge carrier pairs. However, for spectrometry, the most important information is given by the time integral of the current pulse. This integral is equal to the total charge deposited q_{dep} inside the sensor, and hence, the number of created charge carrier pairs and the energy deposited in sensor by the primary particle. Therefore, the exact current pulse shape is irrelevant for spectrometry as long as its duration time is significantly shorter than any other time constant in the readout circuit, and it can be approximated as delta function. This condition in modern, thin silicon sensors is usually met, unlike for some of the gas detectors where long charge collection time may extend the slope of current pulse.

Charge preamplifier

The preamplifier for spectrometry usually works in charge sensitive mode, as shown in Figure 1.18a. In this mode the preamplifier, together with feedback capacitance $\mathrm{C_{feed}}$, works as an integrator providing voltage steps at its output $\mathrm{V_{pre}}$ proportional to the overall charge of the input current pulses, and therefore, to the energy deposited in the sensor volume. The input charge $\mathrm{q_{in}}$ is distributed between the detector capacitance $\mathrm{C_{det}}$ and the effective preamplifier input capacitance $\approx K(s)\cdot\mathrm{C_{feed}}$.



a) Schematic diagram of charge sensitive preamplifier

b) Responses of the charge sensitive preamplifier for different feedback circuits

Figure 1.18: Charge sensitive mode of preamplifier.

Hence, the value of output voltage step V_{step} can be determined as:

$$V_{step} = -\frac{1}{C_{feed} + \frac{C_{feed}+C_{det}}{K(s)}} \cdot q_{in} \overset{K(s)\gg 1}{\simeq} -\frac{q_{in}}{C_{feed}} \quad . \tag{1.19}$$

As can be seen from equation 1.19, to make the response independent of the detector capacitance, the voltage gain $K(s)$ of the preamplifier has to be sufficiently high. Then, the value of the output voltage step V_{step} depends only on the feedback capacitance C_{feed} and the input charge q_{in}. The simplified response V_{pre} of charge sensitive preamplifier, containing only capacitance C_{feed} in the feedback circuit, is shown in Figure 1.18b. Since all input current pulses are positive, all output steps are negative and, in the presented example, the preamplifier output saturates after three impulses (three particles traversing the sensor), and is unable to produce any further responses. To avoid saturation, the feedback capacitance C_{feed} has to be discharged, either periodically by the reset switch S_{reset}, or continuously by the parallel resistance R_{feed}.

The simplified response $V_{pre,reset}$ of preamplifier with reset, also known as gated amplifier, is shown in Figure 1.18b. The reset phase can be performed periodically or triggered by internal circuit detecting the saturation at preamplifier output. In both cases, during the reset phase – called dead time, the preamplifier is insensitive to input signals. In the presented example, the third current pulse, occurring during the preamplifier dead time, was not reproduced at the output. For the asynchronous case (i.e. particles generated in radioactive decay) the time of input pulse occurrence cannot be determined and some fraction of events are lost during the reset phase.

To avoid the dead time during the reset phase, the feedback capacitance C_{feed} can be continuously discharged by the parallel resistance R_{feed}. An example response of continuously discharged preamplifier $V_{pre,cont}$ is shown in Figure 1.18b. After each step caused by the input current pulse, the preamplifier output response returns exponentially to the baseline value with time constant $\tau_{feed} = R_{feed}C_{feed}$. This leads to a long tail appearing at the preamplifier output and disturbing the baseline value. To resolve this problem, a pole-zero cancellation circuit can be added between the preamplifier and the shaper. The second drawback of continuous discharge is an additional current noise source introduced by the feedback resistance R_{feed}. Since the spectral density of resistive current noise is described by $4kT/R$, to minimize this effect the feedback resistance has to be sufficiently large. Unlike the gated preamplifier, for which the voltage response remains constant

between pulses, the response of continuously discharged preamplifier is constantly changing. The energy deposited by a particle is therefore proportional only to the maximum of each pulse. As can be seen from Figure 1.18b, in order to precisely determinate the pulse maximum, the exact value of the previous pulse tail at the next pulse occurrence has to be known. This effect is called a pile-up. A next stage, a shaper, is used to minimize the pile-up effect.

The feedback capacitance C_{feed} has to be carefully chosen. To achieve a reasonable Signal-to-Noise Ratio (SNR) even for MIP, a relatively small capacitance is needed in order to obtain high charge gain. From the other side, a large charge deposition will lead in such case to the preamplifier saturation. Increasing the feedback capacitance decreases the probability of saturation for the large depositions, but limits the MIP detection capability. Therefore, the exact value of the feedback capacitance is a trade off between good SNR for small signals and upper limit of charge depositions. A more sophisticated solution can be used with the gated preamplifier, where the feedback capacitance can be dynamically switched in order to achieve a dynamic charge gain.

Shaper

The signal from the preamplifier has to be processed (shaped) in order to improve the overall Signal-to-Noise Ratio (SNR) and to increase the maximum pulse rate by shortening the pulse length. Since the signal at the preamplifier output is already high, the noise introduced by the following signal processing stages is usually negligible. Therefore, a conventional band-pass filters, called $CR-(RC)^n$ or semi-Gaussian, are commonly used as the shaper circuit. A simplified schematic of $CR-(RC)^n$ filter is shown in Figure 1.19. The first stage of the filter provides the differentiator $C_{diff}R_{diff}$, filtering the low frequency noise and determining the pulse duration, and the first integrator $R_{int}C_{int}$. The first stage is followed by $(n-1)$ integrating stages, resulting, in combination with the first stage, in $(RC)^n$ integrator which filters the high frequency noise and determines the pulse rise time. Assuming that $R_{diff}C_{diff} = R_{int}C_{int} = \tau_{sh}$, the transfer function of n-order semi-Gaussian filter can be written as:

$$H(s) = (-1)^n \frac{s\tau_{sh}^n}{(1+s\tau_{sh})^{n+1}} . \tag{1.20}$$

A step response of the filter in time domain can be expressed as:

$$|V_{out}(t)| = \frac{1}{n!}\left(\frac{t}{\tau_{sh}}\right)^n e^{-\frac{t}{\tau_{sh}}} . \tag{1.21}$$

The time response of the $CR-(RC)^n$ semi-Gaussian filter reaches the maximum value for $t = T_{peak}$, so-called peaking time. For n-stage filter, the peaking time is n times longer than the filter time

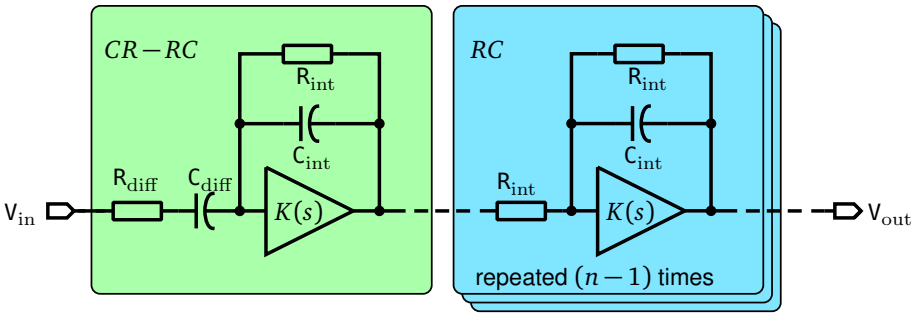


Figure 1.19: Simplified schematic of a $CR-(RC)^n$ semi-Gaussian filter.

constant τ_{sh}, i.e. $T_{peak} = n \cdot \tau_{\mathrm{sh}}$. The maximum amplitude can be derived as:

$$\mathrm{V}_{\max} = \mathrm{V}_{\mathrm{out}}(T_{peak}) = \frac{1}{n!}\left(\frac{n\tau_{\mathrm{sh}}}{\tau_{\mathrm{sh}}}\right)^n e^{-\frac{n\tau_{\mathrm{sh}}}{\tau_{\mathrm{sh}}}} = \frac{1}{n!}\left(\frac{n}{e}\right)^n . \tag{1.22}$$

The normalized time response of semi-Gaussian $CR-(RC)^n$ filter for different order n at constant peaking time equal to 50 ns (i.e. with proportionally scaled time constant τ_{sh}/n) is presented in Figure 1.20. It can be clearly seen, that with increasing filter order the time response becomes shorter improving the immunity to pile-up effects, what allows to increase the maximum event rate. For the presented 9th order filter, $CR-(RC)^9$, the pulse response becomes close to Gaussian function, although starting from the fourth order filter, $CR-(RC)^4$, further increasing of the filter order does not provide substantial shortening of the pulse. With the increasing filter order the number of integrating stages (and, as a result, the power consumption and overall shaper complexity) increases proportionally.

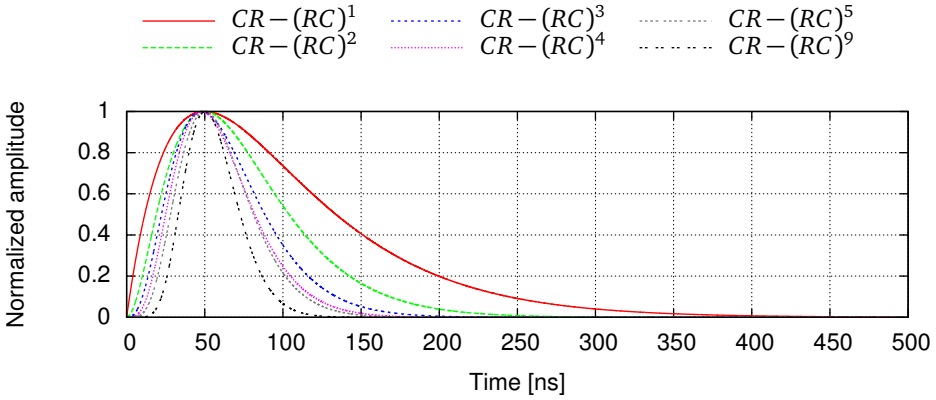


Figure 1.20: Normalized time response of semi-Gaussian $CR-(RC)^n$ filter for different order n at peaking time 50 ns.

The main role of the shaper circuit is to improve the SNR by reducing the bandwidth of the whole preamplifier-shaper chain what results in effective reduction of noise level. To compare the effect of various order $CR-(RC)^n$ filtering on noise performance, the relative noise (serial and parallel) levels for the first three order filters in function of peaking time T_{peak} are presented in Figure 1.21 [59]. The

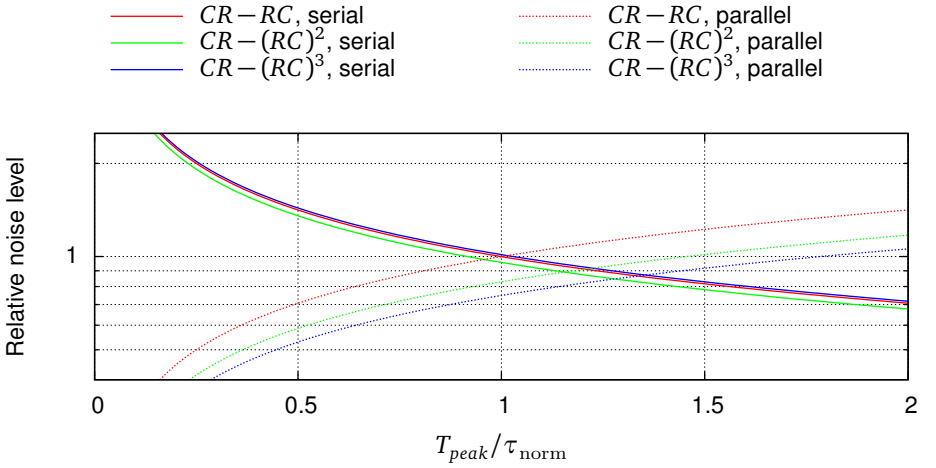


Figure 1.21: Relative serial and parallel noise levels as a function of peaking time for various filter order n.

noise levels are normalized (separately, serial and parallel) to the noise level at the output of $CR{-}RC$ filter with peaking time equal to τ_{norm}. The serial noise is inversely proportional to the square root of peaking time. Therefore, increasing the T_{peak} reduces the serial noise component, however the parallel noise component increases at the same time, since it is directly proportional to $\sqrt{T_{peak}}$. The increasing filter order improves the serial noise performance, while for the parallel noise the $CR-(RC)^2$ is an optimal filter. In order to achieve the best noise filtering, the filter peaking time should be set to the value for which the serial and parallel noise components are equal. However, additional requirements on the pulse duration impose the peaking time different from the optimal one in many applications. The trade off between circuit complexity, power consumption and other requirements (like pulse shape required by the reconstruction method proposed for particular readout) also leads to the selection of non-optimal for noise filter order.

Amplitude measurements

In many applications (like tracking) the spatial and the timing information about incoming particles ares sufficient and the exact energy deposition is not necessary. In such case, a so-called binary readout is commonly used. It comprises a comparator with arbitrary chosen discrimination level, providing a binary (zero-one) information which indicates the occurrence of charge deposition exceeding the discrimination threshold. For calorimetry applications, in order to allow the exact shower development reconstruction, the charge deposited in the sensor volume has to be precisely measured.

The time response $\mathrm{V}_{\mathrm{front-end}}(t)$ of the complete preamplifier-shaper chain is given by the time-domain convolution of the preamplifier 1.19 and shaper 1.21 step response and can be expressed as follows:

$$|\mathrm{V}_{\mathrm{front-end}}(t)| = \frac{\mathrm{q_{in}}}{\mathrm{C_{feed}}}\frac{1}{n!}\left(\frac{t}{\tau_{\mathrm{sh}}}\right)^n e^{-\frac{t}{\tau_{\mathrm{sh}}}} . \tag{1.23}$$

The pulse maximum at peaking time T_{peak} can be therefore calculated as:

$$\mathrm{V}^{\mathrm{max}}_{\mathrm{front-end}} = \mathrm{V}_{\mathrm{front-end}}(T_{peak}) = \frac{\mathrm{q_{in}}}{\mathrm{C_{feed}}}\frac{1}{n!}\left(\frac{n}{e}\right)^n = \mathrm{q_{in}}\cdot\alpha_{\mathrm{design}} , \tag{1.24}$$

where proportionality factor α_{design} depends only on the design constrains (shaper order, preamplifier feedback capacitance) and can be treated as constant for a given readout. The measurement of pulse amplitude $\mathrm{V}^{\mathrm{max}}_{\mathrm{front-end}}$ provides direct information about the charge $\mathrm{q_{in}}$ deposited in the sensor volume by the particle. Depending on the characteristic of the radiation source, two general cases can be considered. In the first one, the radiation is generated periodically (e.g. in beam-beam collision in the accelerator experiment). In such case a single sample (i.e. a single measurement) can be taken directly at the peaking time providing the exact information about the pulse maximum value. In the second case, the radiation is generated asynchronously, e.g. by a radioactive source or by a continuous beam. In that case, the time position of each pulse maximum cannot be known and the synchronous sampling is not applicable.

A commonly used method which allows to measure the pulse maximum in the asynchronous case is a peak detector circuit comprising a sampling capacitance charged through a semiconductor diode (ideally one-directional switch). On the rising edge of the output pulse the sampling capacitance is charged through the forward-biased diode. When the output pulse passes the maximum value, the diode becomes reversely biased, preventing the sampling capacitance from discharge. The sampled maximum value is therefore stored on the sampling capacitance and can be measured by the appropriate circuitry. After that, the sampling capacitance has to be discharged by an additional reset circuit in order to enable the next pulse peak detection. This means, that the dead time is introduced

into the readout system, similarly as it is in the case of the gated preamplifier. The semiconductor diode, essential for the peak detection, is not available in many modern CMOS technologies. Nevertheless the basic idea has been kept, but the practical realization has been elaborated and is realized in more precise way by more complex CMOS circuitry.

The second approach to the asynchronously generated radiation measurements utilizes a continuous sampling with arbitrary chosen period. An example of such sampling performed with period equal to the front-end peaking time of 50 ns is presented in Figure 1.22. In this case none of the samples directly represents the pulse maximum. The pulse reconstruction algorithm has to be applied in the signal post-processing in order to reconstruct the maximum value which corresponds to the deposited energy. In the most basic approach, a theoretical pulse shape, given by formula 1.23, can be fitted to the registered samples, e.g. using the least squares method. A more sophisticated algorithm, the deconvolution, is proposed for the LumiCal readout and is described in details in the following chapter.

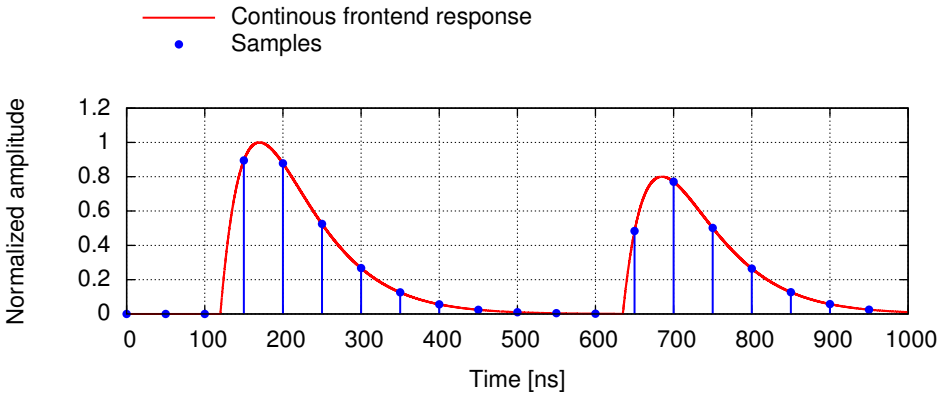


Figure 1.22: Example of continuous sampling of front-end response to the asynchronously generated radiation.

In the more advanced readout, the sampled analogue values (both in synchronous and asynchronous cases) are converted into the digital form in order to simplify the data transmitting, storing and processing. The Analog-to-Digital Converter (ADC) is used to perform this operation. Various ADC architectures are used, depending on the required resolution and conversion rate. In the past, the Wilkinson ADC [60] was widely used in detector readout systems since it offers a very good linearity. The sample rate of Wilkinson architecture is quite limited (reaching single kSps), therefore it is not suitable for modern designs with higher sampling rates or with continuous sampling of asynchronously generated radiation. In order to achieve a higher conversion rates (a several tens of MSps), a faster ADC architectures, e.g. flash, pipeline or Successive Approximation Register (SAR), can be used in the readout chain.

1.4.2 First LumiCal readout prototype

In order to verify basic concepts and assumptions adopted for the LumiCal detector, the prototype needs to be built and experimentally tested. The target prototype should comprise 30 layers of tungsten absorber with at least one tile (256 readout channels) of active sensor, constructed accordingly to the assumed detector geometry. As the first step in the detector prototype development, a single layer prototype comprising a silicon sensor and a dedicated readout was designed and fabricated. The extensive tests were performed on the continuous electron beam at DESY II accelerator in Deutsches Elektronen-Synchrotron (DESY) [48]. The photograph of the single layer readout board together

Figure 1.23: Photograph of the single layer LumiCal detector readout module.

with the silicon sensor is presented in Figure 1.23. The readout comprises four pairs of 8-channel ASICs, the front-end and pipeline ADC ones, providing 32 readout channels coupled to the silicon sensor. The on-board FPGA controls the ASICs and provides the data processing chain comprising data buffering, required in order to apply the first level triggering, data serialization and transmission to Personal Computer (PC) through the Universal Asynchronous Receiver/Transmitter (UART) to Universal Serial Bus (USB) converter. Since the readout is capable to read only 32 sensor pads, the sensor region coupled to the readout electronics had to be carefully chosen. As it was shown in Section 1.3, the effective Molière radius expected for the LumiCal is around 12 mm. With respect to that, the topmost pads (the widest ones) in two neighboring central sensor sectors were chosen, as it is shown in Figure 1.24. Due to the mistake made in the PCB design phase, 14 pads from the left

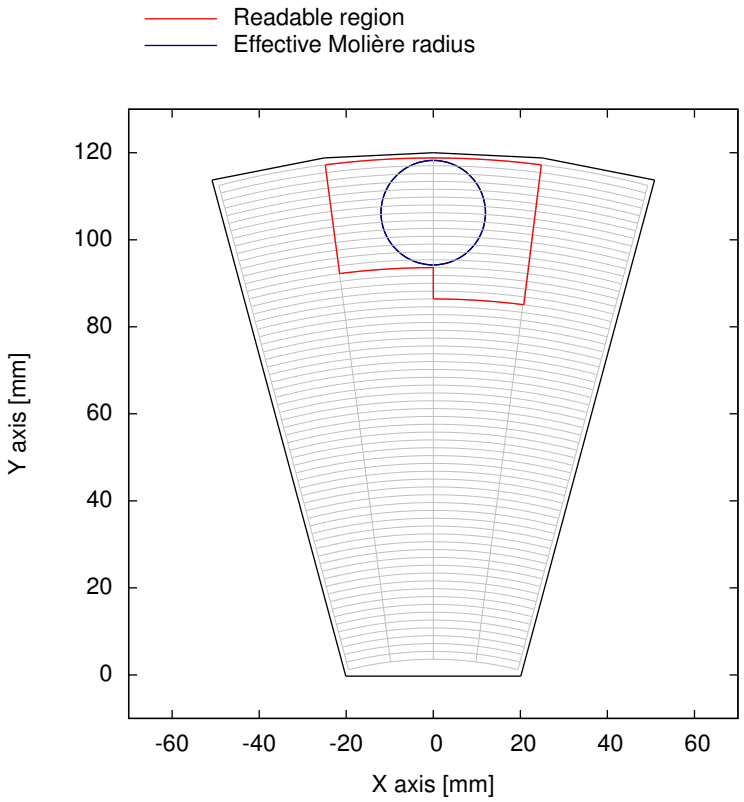


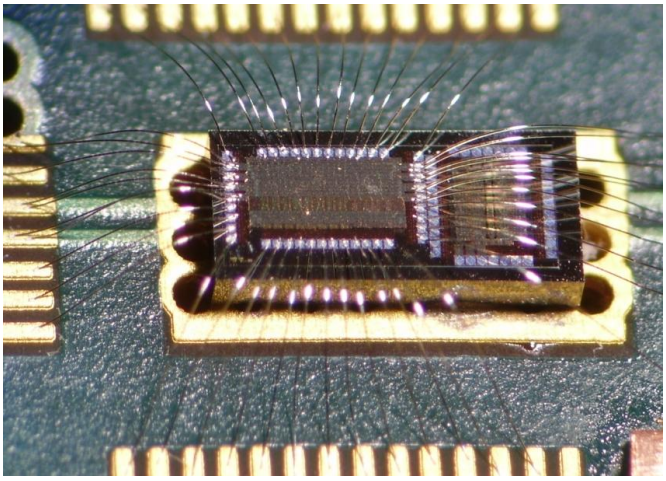
Figure 1.24: Readable region of the sensor at single layer LumiCal readout prototype.

sector and 18 pads from the right one were connected to the front-end electronics. Despite that, the readable region still covers the whole effective Molière radius.

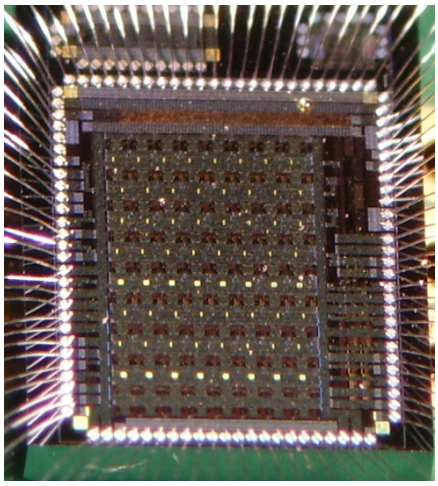
Front-end and ADC ASICs

The sensor signal processing chain, presented in Figure 1.15, was split between two separate ASICs, the front-end and ADC ones, in order to improve the testability and to simplify the design process. Both ASICs were designed and fabricated in AMS 350 nm technology. The photographs of the glued and bonded to PCB front-end and ADC ASICs are presented in Figures 1.25a and 1.25b, respectively.

The chosen front-end architecture comprises a charge sensitive amplifier, a Pole-Zero Cancellation (PZC) circuit, and a $CR-RC$ shaper [49]. Since the architecture is almost identical to the one chosen for the next prototype, and described in details in Section 3.2, only the basic information and differences between the prototypes will be presented. To cover a very wide input charge dynamic range (MIP sensitivity for the muon calibration and up to 6 pC of charge deposition in the shower maximum), two presetable preamplifier gains were implemented, similarly as in the second prototype. The amplifiers were designed as folded cascodes [61] with active loads, followed by source followers. The shaper time constant was set to 60 ns and the measured peaking time is slightly below 70 ns. The front-end ASIC comprises 8 channels divided into two groups. First of them utilizes passive resistances in the preamplifier feedback and PZC circuits, while the second one uses Metal-Oxide Semiconductor (MOS) transistors working in a triode region [62]. The passive feedback resistance in calibration mode reaches 1.5 MΩ, while the MOS transistor drain-source resistance provides a



a) Photograph of prototype front-end ASIC



b) Photograph of prototype ADC ASIC

Figure 1.25: Photographs of front-end and ADC prototype ASICs, glued and bonded on PCB.

significantly higher value, improving the noise performance. The first channels group (with passive resistance) utilizes 0.5 pF preamplifier feedback capacitance in calibration mode, while the second one – 0.23 pF. This results in different charge gain between the two groups with the ratio between them of 0.5/0.23≈2.17. The area occupied by a single channel is 630 μm × 100 μm. The average power consumption is around 8.9 mW per channel and can be effectively lowered 200 times due to the power pulsing foreseen for the ILC beam structure.

For the ADC prototype, the pipeline architecture was chosen. The development of 8-channel prototype [63] was preceded by several steps – the Multiplying DAC (MDAC) core was initially designed [64] and a single channel ADC was developed after that [50, 65]. The complete multichannel digitizer, comprising 8 ADC cores followed by a data serializer with a Low-Voltage Differential Signaling (LVDS) drivers, steered by several built-in Digital-to-Analog Converters (DACs) and a digital control unit, was developed. The chosen 10-bit pipeline ADC utilizes 10 identical stages, each one comprising a Sample and Hold (S&H) circuit, 1.5 bit (3 possible values) flash ADC, 1-bit DAC and a very precise amplifier. The input voltage is sampled by the S&H circuit and converted by the 1.5 bit ADC. The conversion result is fed to the DAC. Its output voltage is subtracted from the sampled input one and the remaining residue is doubled by the output amplifier and sent to the next stage. The next sample from the ADC input can be taken as soon as single stage conversion is done, improving the maximum sample rate. The active size of the multichannel ADC prototype is 3.17 mm × 2.95 mm with 8 ADC cores placed in parallel with 200 μm pitch. The average ADC core power consumption is around 800 uW per channel per MSps, resulting in around 16 mW per channel at nominal sample rate of 20 MSps.

Complete readout architecture

The block diagram of the complete LumiCal single layer readout module architecture is presented in Figure 1.26. In order to increase the system testability as well as to allow operations with different sensors (e.g. BeamCal), the sensor is connected to the readout board through a dedicated connector. The current signal from radiation sensor is amplified by four 8-channel front-end ASICs and digitized by four 8-channel pipeline ADCs. The initially serialized data are fed to the Xilinx Spartan 3

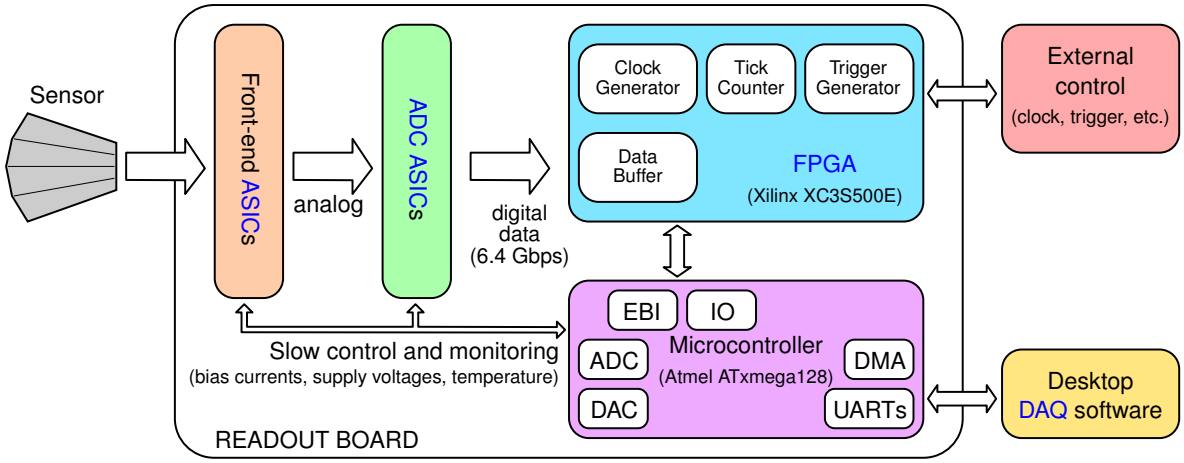


Figure 1.26: Block diagram of the complete readout architecture [66].

(XC3S500E) FPGA. Since during the testbeam a continuous beam, resulting in asynchronously generated events, is foreseen, a continuous sampling is applied (see Section 1.4.1). From the detailed deconvolution study, the sampling period similar to the shaper peaking time was chosen [66]. This results in 20 MSps ADC and about 6.4 Gbps raw data stream between the ADC ASICs and FPGA. Since the communication protocol (UART) between the readout board and the external PC receiving and storing the detector data limits the transmission bandwidth to around 1 Mbps, the first trigger level has to be applied by the on-board FPGA. Two triggering schemes are possible in the current system – the trigger can be provided from an external source (e.g. scintillators detecting beam particles, see Section 2.1.2) or generated internally by the FPGA itself. The second option, so-called self-triggered or event driven, is based on digital comparators tracking the signal level in each channel separately and detecting the events that exceed the preset threshold. Regardless of the source, an adjustable number of consecutive samples (in order to enable the pulse amplitude reconstruction algorithm) is concatenated into the data package after the trigger signal. Since the transmission bandwidth is limited, a veto mechanism is applied in order to ensure a sufficient time for data packaging between the accepted triggers. The example waveforms of the presented system are shown in Figure 1.27. On the first trigger occurrence, the 8 consecutive ADC samples from the FPGA data buffer are concatenated into the data packet, transmitted later as the "A" event. During the packet building, a veto signal is set resulting in rejection of the second trigger. The third trigger is accepted by the system, resulting in the "B" event, since all the required operations related to the "A" event are accomplished. The veto mechanism limits therefore the maximum event rate which the system is capable to register. The detailed studies showed that for packet containing only 3 ADC samples per event (minimum value

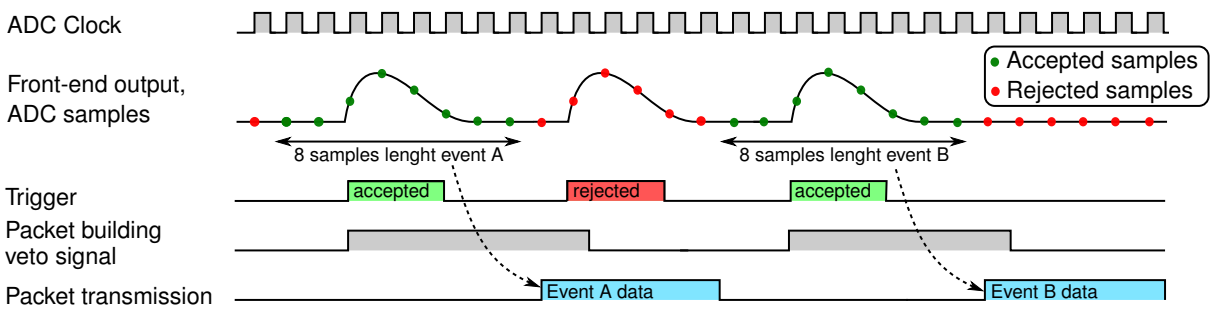


Figure 1.27: Single layer readout system waveforms [66].

required by the deconvolution process), the maximum event rate slightly exceeds 1000 events per second [66]. Since with the increased number of samples per event the size of data packet is also increasing, the average event rate decreases proportionally.

Apart from the DAQ, the readout board provides a voltage and current biasing required by the front-end and ADC ASICs, a High Voltage (HV) filter for sensor biasing and a monitoring of the key parameters (e.g. current, temperature). The whole DAQ operation as well as other parameters (e.g. biasing) are controlled by the Atmel ATXmega128 microcontroller (see Figure 1.26) connected to the PC through a dedicated UART connection. This allows to control the whole system using a custom PC software, such like EUDAQ platform – a portable desktop DAQ system designed for use with the EUDET pixel detector [67].

Chapter 2

Testbeam of LumiCal multi-plane prototype

In the recent years the single layer LumiCal readout board was successfully used in a number of testbeams [66, 48]. The next step in the detector prototype development was to prepare and conduct a testbeam of a multi-plane module. Apart from the readout board modifications, to allow the multiple-plane operation, a very sophisticated mechanical structure had to be developed to meet the demanding geometrical requirements. As it was shown in Section 1.3.3, the precision of the shower polar angle reconstruction imposes a tens of micrometers precision in relative absorber layers positioning. Since only four sensors plus readout planes are currently available, the mechanical structure had to enable modifications in the detector layout during testbeam, in order to imitate configurations with up to ten active layers (see details in following section). The multi-plane testbeam was performed in October 2014 at T9 east area of Proton Synchrotron (PS) at CERN. The overall view of CERN accelerator complex with east area marked is presented in Figure 2.1.

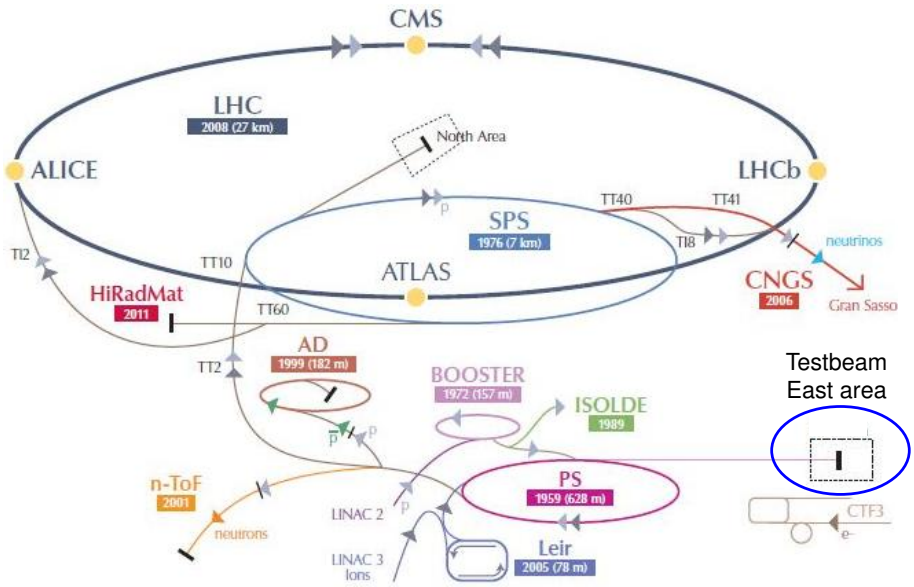


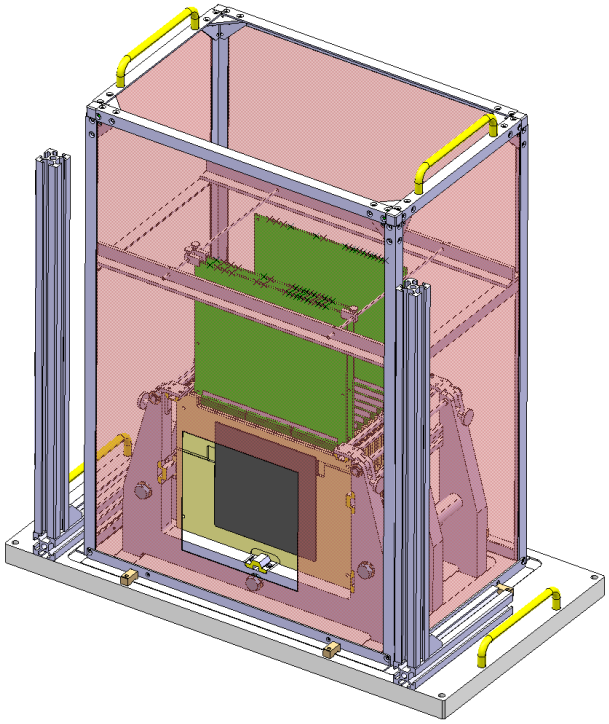
Figure 2.1: Overall view of CERN accelerator complex. The testbeam east area, marked with blue ellipse, is located in the bottom right corner.

2.1 Overview of testbeam instrumentation

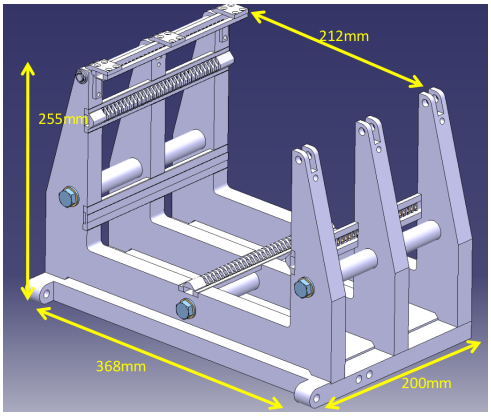
2.1.1 Mechanical framework

Mechanical supporting structure

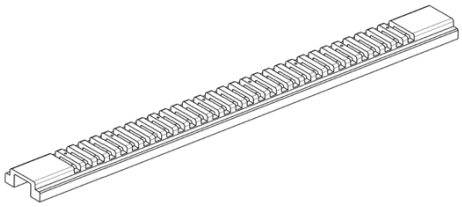
In order to meet the demanding geometrical requirements of the LumiCal detector and to enable a very flexible configuration of active sensor layers together with tungsten absorbers, a very sophisticated mechanical structure was designed and developed at CERN [68, 69]. The overall view of the structure is presented in Figure 2.2a. The most important component, the layers positioning structure, is presented in Figure 2.2b. It includes three aluminum combs with 30 slots each, presented in Figure 2.2c, which allow to install the tungsten absorber or active sensor layer with the required precision. The 3.5 mm thick tungsten absorber plates are mounted in supporting frames, as shown in Figure 2.3a. The light gray insets located on left, right (outside) and bottom (inside) sides of the supporting frame (yellow) contain a small bearing balls providing a precisely positioned support points for the comb slots.



a) Overview of the complete mechanical structure with the tungsten absorbers and readout boards installed



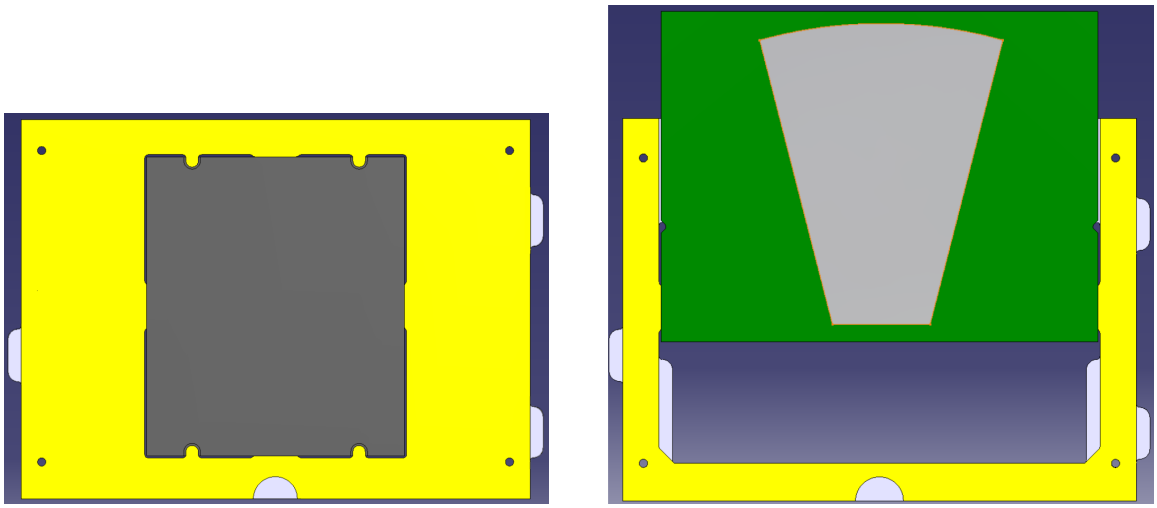
b) Dimensions of the layers positioning structure



c) 30 slots comb positioning the detector layers

Figure 2.2: Overview of the LumiCal prototype mechanical structure [68, 69].

As it was shown in Section 1.3.3, the 3.5 mm thick tungsten absorber layers should be uniformly distributed with 1 mm gap, between consecutive layers, provided by the combs. However, this require a quite sophisticated sensor supporting structure, with overall thickness lower than 1 mm, comprising a mechanical support, a backplane HV polarization (i.e. a kapton foil), a 300 μm thick silicon sensor, and a kapton fanout coupling the sensor pads to the readout electronics. Since currently the sensors are mounted onto a rather thick (around 2 mm) PCB serving as the mechanical support together



a) Tungsten absorber (gray) in a supporting frame (yellow)

b) Sensor (gray) PCB (green) partially retracted from a supporting frame (yellow)

Figure 2.3: Detector layers supporting frames [68, 69].

with HV polarization, the target geometry with silicon sensor located in a 1 mm gap, presented in Figure 2.4, is not yet possible. For this reason, a workaround with active sensor layers located in place of tungsten absorber, as presented in Figure 2.5 was chosen. In order to assemble the sensor PCB in the comb slot provided for the tungsten absorber, a supporting frame with identical outer dimensions was prepared as shown in Figure 2.3b. This enables a flexible detector configuration and allows to easily change the detector prototype geometry. This functionality was fully exploited during the

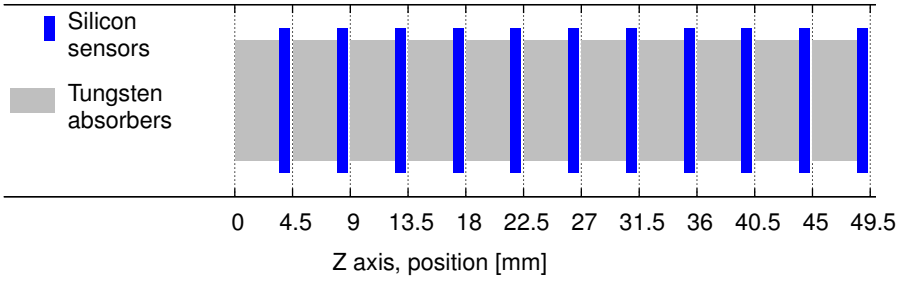


Figure 2.4: Target geometry of the LumiCal detector prototype. Y axis (perpendicular to Z) not in scale.

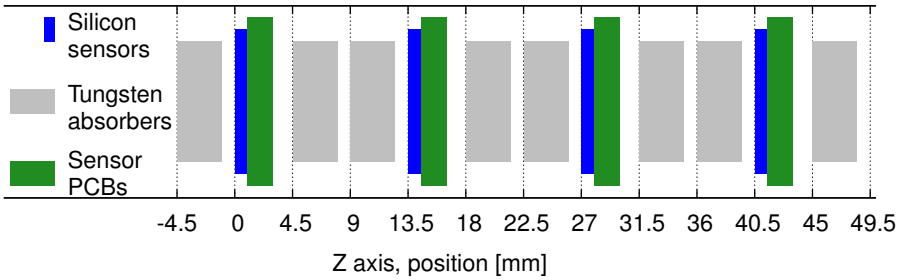
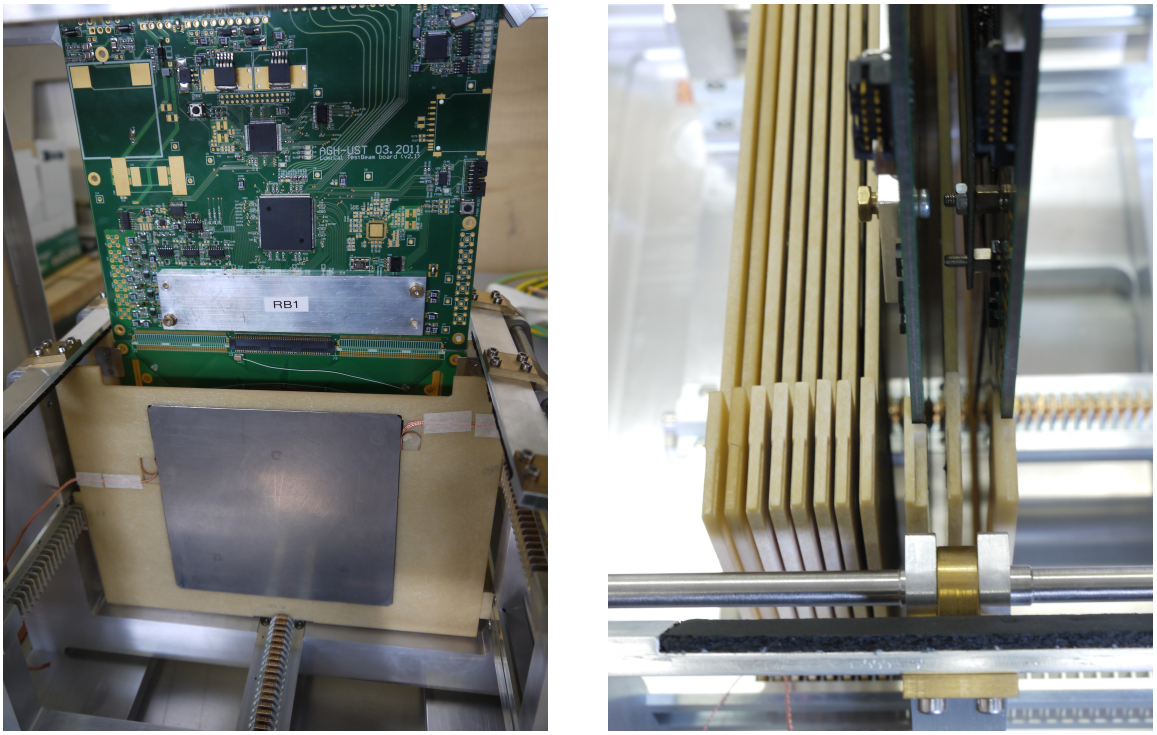


Figure 2.5: Current geometry of the LumiCal detector prototype with active sensor layers located in place of tungsten absorbers. Y axis (perpendicular to Z) not in scale.

last testbeam in order to improve measurements of the shower development, as it is discussed in the following section.

The positioning precision of supporting structure , as well as the tungsten absorber thickness uniformity, were extensively tested [69]. The maximum differences between the theoretical and measured absorber plane positions do not exceed the required ±50 μm precision. The integration tests of mechanical structure with active sensors and readout electronics were performed before the testbeam and the full detector prototype functionality was confirmed.



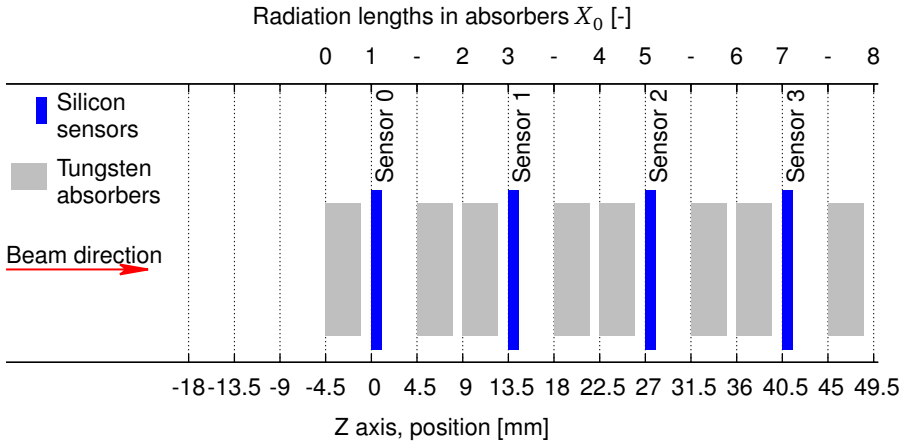
a) Photograph of readout board with silicon sensor mounted in supporting structure, preceded by the tungsten absorber layer

b) Detailed view of two silicon sensors, separated by one tungsten absorber and preceded by 8 absorber layers. An additional one empty slot on both side of each silicon sensor was left in order to simplify the trail assembly

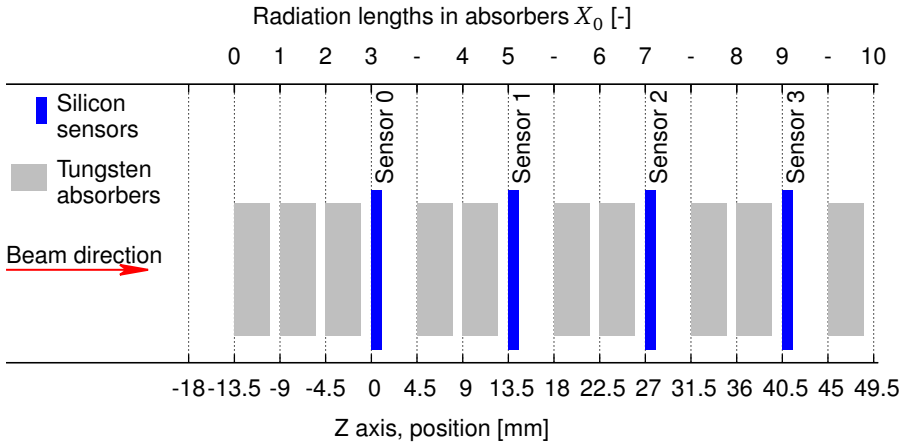
Figure 2.6: Photographs of LumiCal mechanical supporting structure.

Detector module geometry

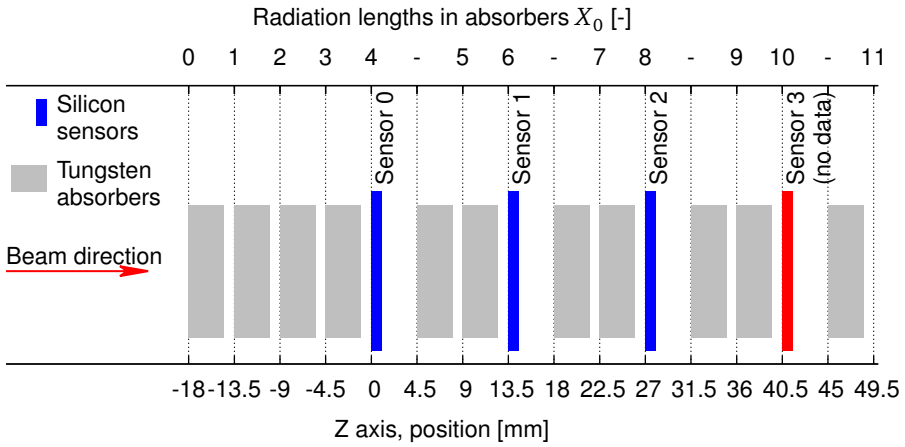
The distribution of energy deposited in each LumiCal layer by the electromagnetic shower reaches the maximum value around the 10th layer for the 250 GeV primary electrons, as it was shown in Section 1.3.3. For the electrons from PS accelerator beam with energy of around 5 GeV, the expected maximum of shower development is located around the 6th layer. In order to reconstruct the shower maximum, the data from at least first 10 layers should be collected. Since only four readout boards are available, this condition could be meet only with at least three absorber layers assembled between each active sensor layer. However, this leads to a rather low spatial resolution of shower development what could result in large uncertainties. Since the mechanical support structure enables a relatively simple detector geometry changes, a different approach was applied.



a) First configuration



b) Second configuration



c) Third configuration

Figure 2.7: Three LumiCal detector prototype configurations used in testbeam. Y axis (perpendicular to Z) not in scale.

A three different detector configurations were used during the testbeam, with the active sensor layers always separated by two absorber layers. By adding additional absorber layers upstream the detector, the sensor layers were effectively moved downstream. The three configurations used in the testbeam are presented in Figure 2.7. The single absorber layer after the last silicon sensor was added in order to simulate the particles backscattering as it takes place in the target detector. The effective positions of active sensor layers in the LumiCal prototype, expressed in the number of absorber layers (i.e. radiation lengths in absorber X_0), are presented in Table 2.1. The shower can be therefore sampled up to 10th layer with the target spatial sampling resolution of one radiation length, by combining the data obtained in all three configurations. Since the positions of sensors S1–S3 in the first configuration are replicated by the S0–S2 in the second one, the measurement results for the corresponding sensors from both configurations should be almost identical. If so, the data can be combined in order to imitate the detector prototype comprising nine active sensor layers.

	Radiation lengths in absorber X_0									
Configuration	1	2	3	4	5	6	7	8	9	10
1	S0		S1		S2		S3			
2			S0		S1		S2		S3	
3				S0		S1		S2		S3

Table 2.1: Relative positions of active sensor layers in three configurations expressed in number of absorber layers (i.e. radiation lengths in absorber X_0). S0–S3 stands for Sensor 0 – Sensor 3.

Unfortunately, due to malfunctioning of the FPGA on readout board , all the data from S3 sensor in the third configuration are corrupted. The malfunctioning was probably caused by a Single-Event Upset (SEU) in the restricted part of the FPGA configuration memory, introduced by the scattered charge particle. For this reason, the available data are limited to the 9th absorber layer gathered by the S3 sensor in the second configuration.

2.1.2 Testbeam instrumentation

PS east area testbeam facility

A high energy electrons source is required to enable the detector prototype validation in the experimental conditions similar to the target ones, foreseen at the future linear collider. Therefore, a natural candidate for the LumiCal testbeam is DESY II synchrotron, providing an electron beam with energies reaching several GeV. As it was already mentioned, the previous single-layer testbeams were done using this facility. However, due to the high DESY testbeam facility occupancy, it was not possible to perform a multi-layer testbeam in 2014 at DESY. Therefore, the PS accelerator T9 testbeam east area, hosted at Conseil Européen pour la Recherche Nucléaire (CERN), was chosen.

No.	Material and length	Diameter	Comment
1	200 mm Be + 3 mm W	10 mm	Electron target
2	100 mm Al + 3 mm W	10 mm	Electron target
3	200 mm Al	10 mm	Hadron target
4	20 mm Al	10 mm	Thin target
5	0 mm	–	Primary beam (empty target)

Table 2.2: PS east area beam converting targets.

The PS accelerator, forming a part of the LHC beam delivery system, provides a primary proton beam with momentum of 24 GeV/c. Since the beam is shared between different testbeam instrumentations (using both the primary and secondary beams) and the LHC beam delivery system, the primary beam for the T9 area is provided in 400 ms long spills with typical time separation of 33.6 s between them. The primary beam is converted using several targets, listed in Table 2.2. For the discussed testbeam, the "Electron targets" were used providing a secondary beam with muons, pions, hadrons and electrons with momentums in range of 1–15 GeV/c. The beam momentum can be fixed by magnetic field of the beam delivery electromagnets while the horizontal spatial spread is reduced by a set of collimators. The simplified overall view (without magnets) of the PS east area testbeam facility is presented in Figure 2.8.

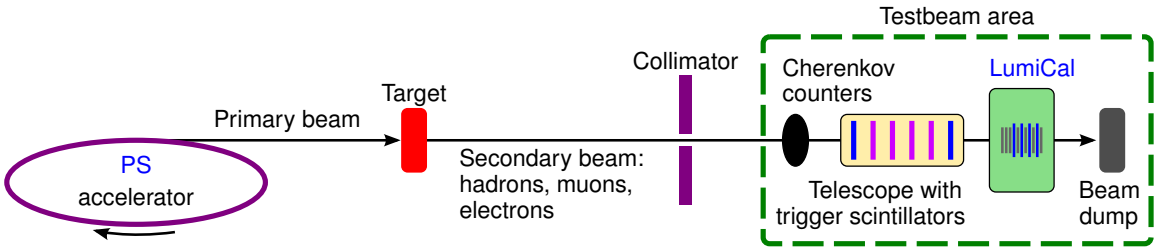


Figure 2.8: Overall, simplified view (not in scale) of the testbeam instrumentation.

Testbeam area instrumentation

The photographs showing the details of the testbeam area instrumentation are presented in Figures 2.9 and 2.10, respectively. The schematic diagram of the instrumentation geometry is presented in Figure 2.11. Since the secondary beam consists of a mix of various particles, the Cherenkov counters were used to discriminate the electrons or/and muons from the incoming beam. The gas Cherenkov counters enable the particle recognition as well as the energy discrimination by changing the biasing High Voltage (HV) and pressure of the gas medium (CO_2). For the given electrons energy of 5 GeV, the gas pressure was set to 53 kPa with HV set to 1900 and 1950 V for the first and second Cherenkov counter, respectively.

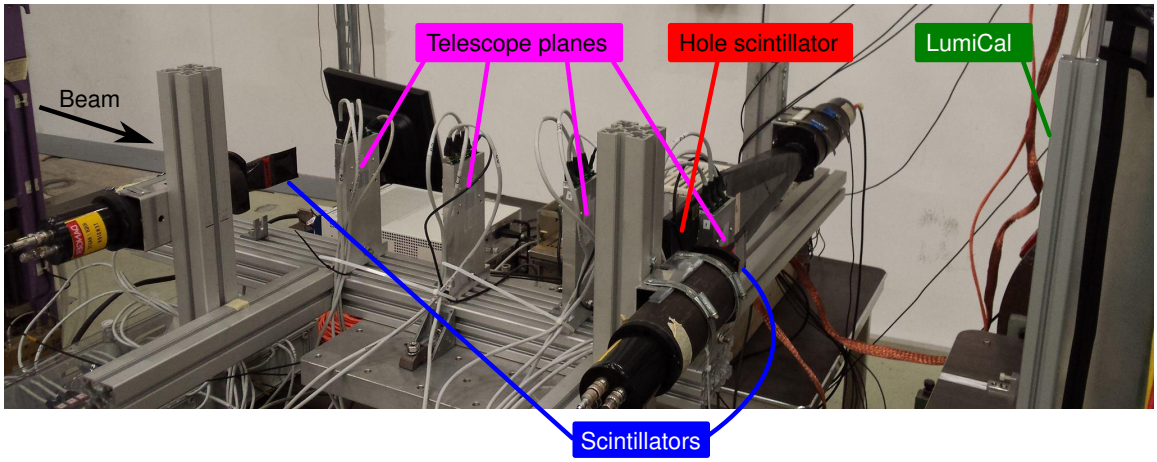


Figure 2.9: Detailed photograph of the testbeam area instrumentation.

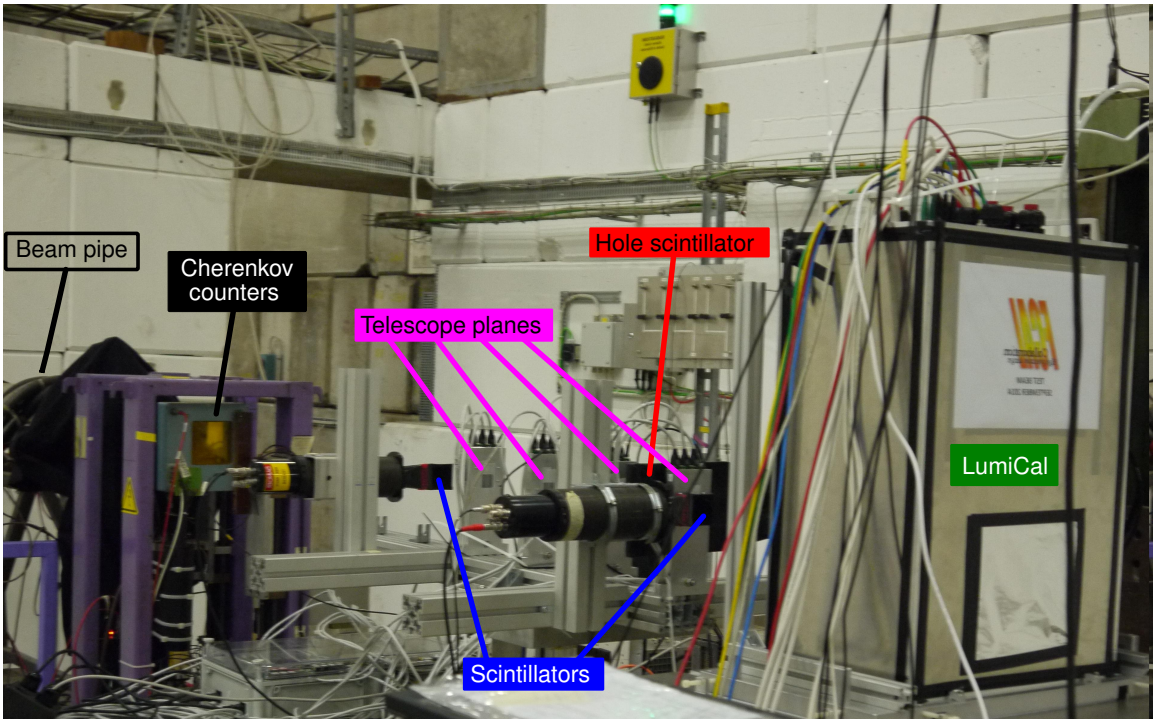


Figure 2.10: Overall photograph of the testbeam area instrumentation.

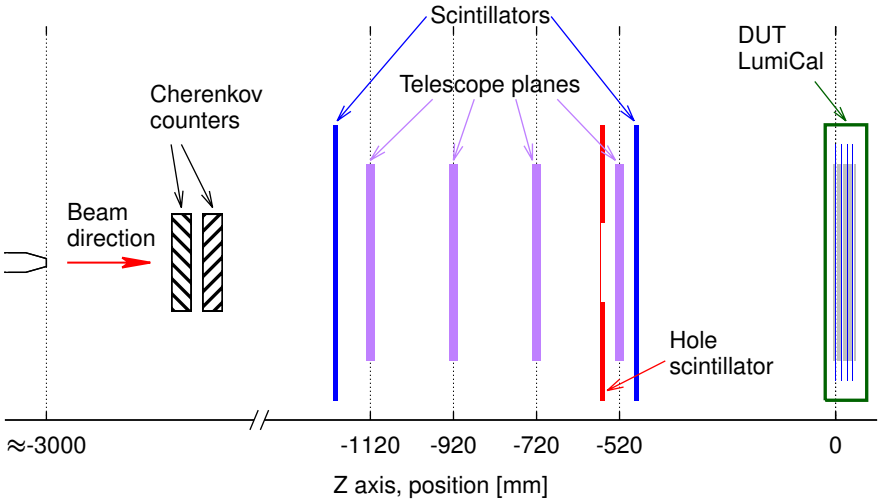


Figure 2.11: Testbeam area instrumentation geometry. Y axis (perpendicular to Z) not in scale.

In order to enable the particle track reconstruction, a multilayer tracking detector, so-called telescope, was developed by the Aarhus University. The telescope utilizes the Mimosa26 chips, a Monolithic Active Pixel Sensors (MAPS) with fast binary readout [70]. The Mimosa26 chip comprises 1152 × 576 pixels with 18.4 μm pitch, resulting in ∼21.2 × 10.6 mm^2 active area. The Mimosa26 utilizes a binary readout indicating the pixel signals exceeding the preset discrimination level. The pixel matrix is read continuously (without triggering) providing a complete frame every 115.2 μs. The data are gathered, triggered and stored by a custom DAQ system, based on the PCI eXtensions for Instrumentation (PXI) crate, developed by the Aarhus University in collaboration with Strasbourg

University. A four telescope planes, each one comprising one Mimosa26 chip, were set upstream the LumiCal as it is shown in Figure 2.11.

To provide a proper trigger, indicating only the particles traversing the active part of telescope sensors and the readable region of LumiCal, three scintillators were used. The two solid 5 × 5 mm^2 scintillators were placed upstream and downstream the telescope (marked in blue in Figure 2.11) and additional one (marked in red), with 9 mm diameter circular hole, was placed just before the last telescope plane. A compact photomultipliers were attached to the scintillators providing electrical pulses corresponding to the particles traversing the scintillators. The coincidence of signals produced by the 5 × 5 mm^2 scintillators indicates incoming particle leaving the telescope within 25 mm^2 area perpendicular to the beam axis. In order to limit this area, the signal from the hole scintillator was set to anti-coincidence, indicating particles which were not detected by the hole scintillator, i.e. the ones that have passed the circular hole. This signal was combined with the Cherenkov counters response, as it is shown in Figure 2.12, to create a system trigger denoting the electrons passing through the central part of the detector system. The schematic front view of the testbeam instrumentation along the beam axis is presented in Figure 2.13.

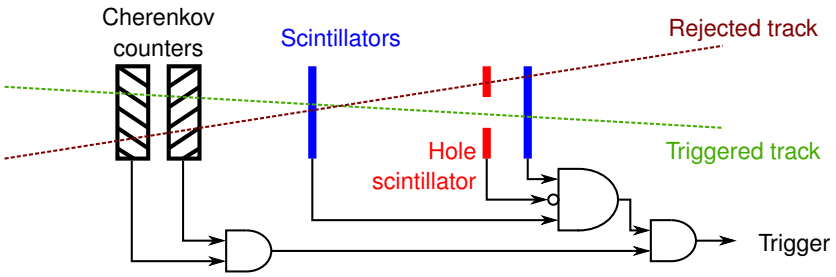


Figure 2.12: Trigger system.

It has to be noted, that the scintillation process efficiency is limited to around 90 %. The two effects, related to this issue, can be considered. If the particle traversing the triggering system is not detected by one of the solid scintillators, the trigger signal is not generated, and the event is lost. The second effect concerns the particles passing outside the circular hole of the anti-coincidence scintillator. An exemplary track of such particle is shown in Figure 2.12 as dark-red line, labeled as rejected track. In such case the trigger should not be generated, however, if the particle is not detected by the hole scintillator, the anti-coincidence condition will be met, causing the triggering for particle passing far away from the center of the system. As it will be shown in the following section, such cases were registered indicating a not fully-efficient scintillation triggering mechanism.

The main limitation of the testbeam instrumentation is introduced by the T9 east area beam structure. As it was already shown, the beam is split into a 400 ms long spills, containing typically 10^3–10^4 particles. Taking into account the spill repetition frequency, slightly below 2 per minute (≈0.03 Hz), and a low (of around 5 %) electron contents of the secondary beam, a 1.5–15 electrons per second are expected on average. However, the electrons arrive in a very short spills, what is very inconvenient for the considered system. As it was explained in Section 1.4.2, the LumiCal DAQ utilizes a veto mechanism rejecting triggers during the event data packaging. As a result, some of the electron triggers generated during 400-ms long spill will be rejected by the LumiCal veto, reducing the average event rate. Moreover, the highly non-uniform beam time structure may impact on the telescope track reconstruction. Since the Mimosa26 chip provides a continuous readout, a high particle intensity during short spill can produce multiple track events, complicating the data analysis.

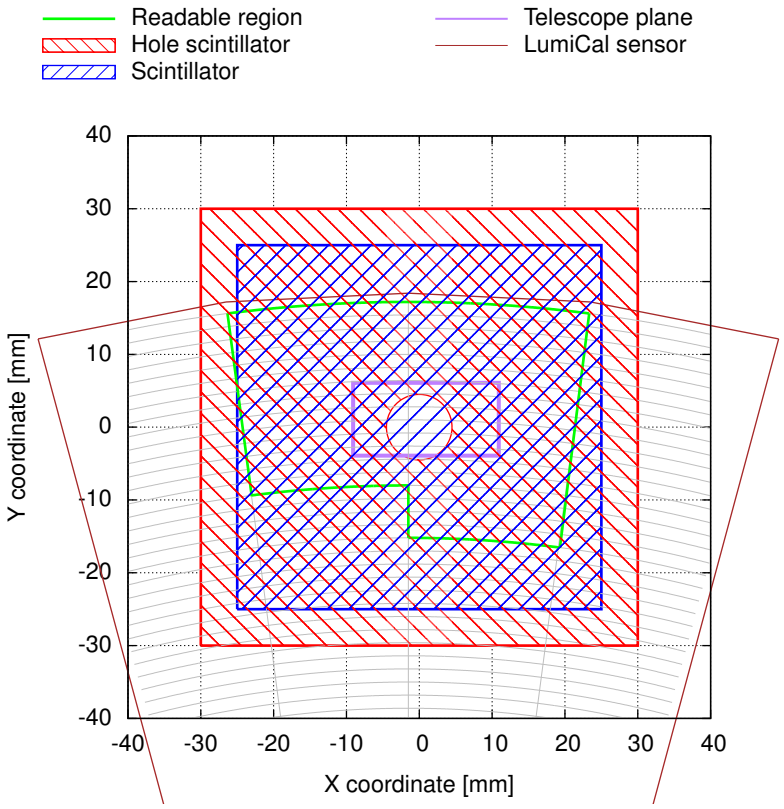


Figure 2.13: Front view of testbeam instrumentation system geometry. The mutual positions of instrumentation components approximated based on analysis results.

2.2 Analysis components

Since the testbeam instrumentation utilizes two detector systems, the telescope, and the Device Under Test (DUT) – the LumiCal, an independent initial data processing is required for both of them. The particle tracks have to be reconstructed from raw binary data, provided by the telescope Mimosa26 chips. To significantly improve the precision of this reconstruction, the telescope alignment procedure has to be used. As it was already shown, the asynchronous sampling in the LumiCal requires amplitude reconstruction in order to compute the charge deposited in each channel. Since the telescope alignment and tracking software were already provided, only the most important issues are presented here. The preprocessing of LumiCal data as well as the amplitude reconstruction method are discussed in more details, since the development of the LumiCal detector is the main subject of this dissertation.

2.2.1 Telescope alignment and tracking

The Mimosa26 utilizes a binary readout indicating a signal in particular pixel exceeding the preset threshold level. One has to note that in such case a false hits can be generated due to the pixel noise. A higher threshold increases the system noise immunity, however, it reduces the sensitivity to lower depositions, impairing the MIPs tracking ability. To improve it, a lower thresholds are needed, resulting in higher false hit rate. Since for the given trigger configuration and beam structure a single particle track per event in average was foreseen, the corresponding average hit count per event per

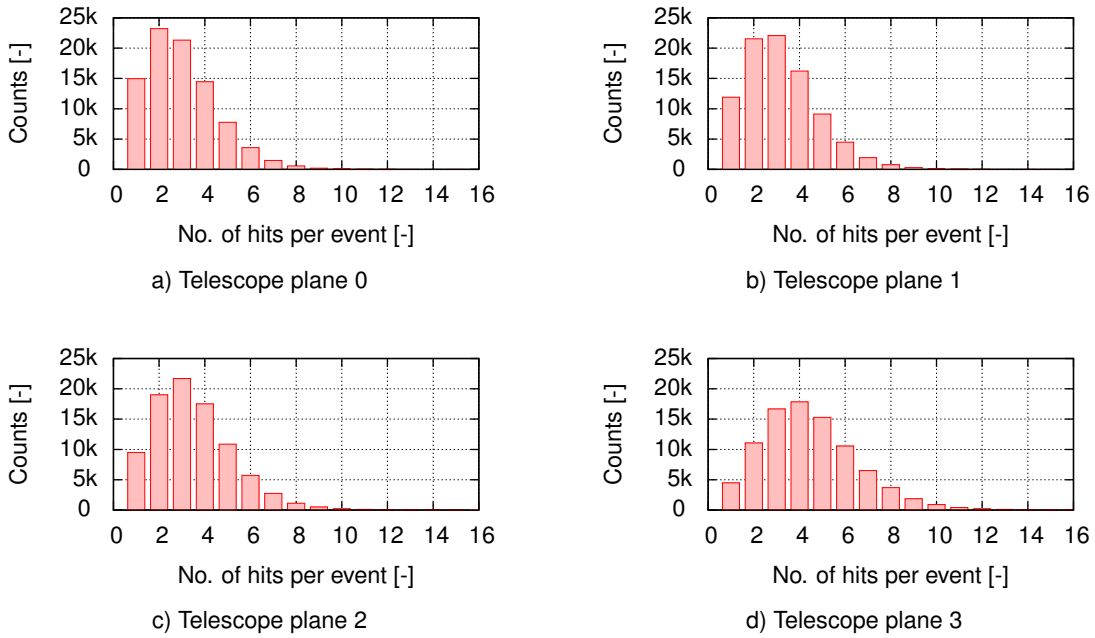


Figure 2.14: Histograms of the number of hits per event for raw telescope data. X axis range limited for clarity.

Telescope plane	No. of hits per event: average	maximum
0	2.99 ± 1.57	15
1	3.20 ± 1.63	39
2	3.47 ± 1.76	62
3	4.45 ± 2.13	65

Table 2.3: Average and maximum number of hits per event for raw telescope data.

plane should be also around one if the noise hits were neglected. To estimate the noise false hit rate, the histograms presenting the number of hits per event for each telescope plane were created and are presented in Figure 2.14. The average number of hits per event and its maximum values are presented in Table 2.3. It is clearly seen, that a false noise hits contribution is quite high and dominates over a real hits generated by the beam particles, especially for the fourth telescope plane. To depict the spatial distribution of the hits, the hit-maps, created for the raw telescope data, are presented in Figure 2.15. Below each hit-map a histogram of hits number in X axis, regardless of their Y axis position, is presented. A clear pattern, corresponding to the Mimosa26 internal architecture, can be seen on the Figure 2.15, especially for the fourth plane (Figure 2.15d). The four regions with different false hit rate, changing according to their X position, can be found, while the transverse beam profile is almost imperceptible. A noticeable beam structure can be only seen on the left side of the third telescope plane histogram (Figure 2.15c, bottom). The high false noise hit rate requires therefore a sophisticated tracking algorithm to detect the real particle track among the false hits.

Alignment considerations

The second component of the telescope data preprocessing, beside tracking, is the alignment procedure. Since the positions of the telescope planes were only roughly set by the telescope mechanical

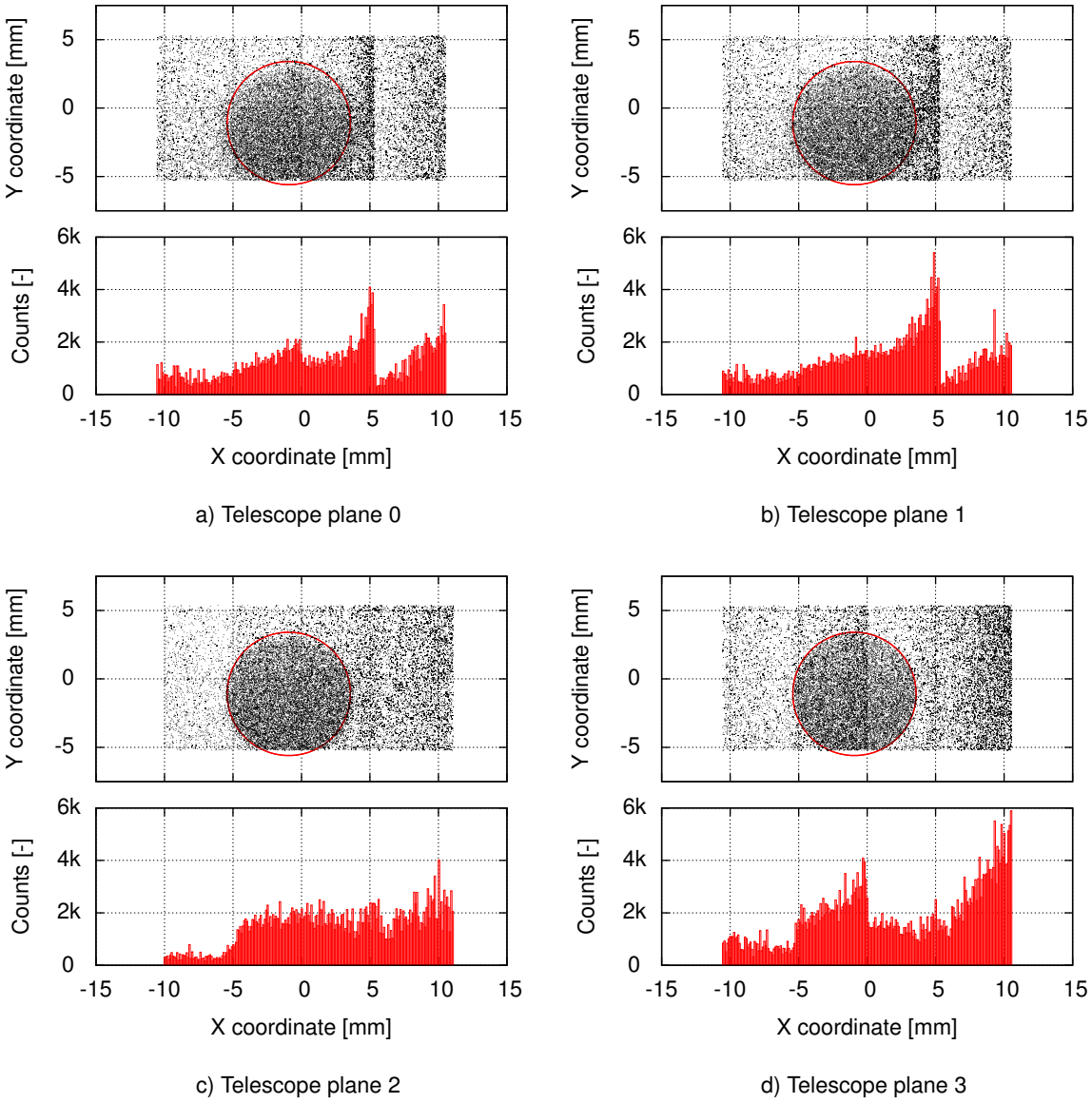
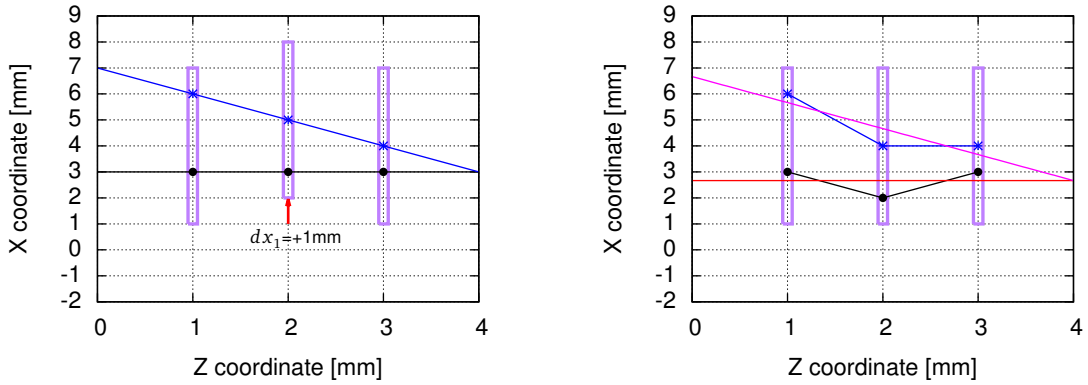


Figure 2.15: Maps of the raw telescope hits (top) together with X axis histograms (bottom). The red circle represents the hole in the anti-coincidence scintillator.

support structure, one can expect a significant (in a μm scale) misplacement between them. A very simplified, two-dimensional schemes illustrating the alignment problem are shown in Figure 2.16. In this example (Figure 2.16a), the second telescope plane is misplaced in X axis by $dx_1 = 1$ mm. Two exemplary particle hits positions were registered. The simplest reconstruction algorithm, assuming an ideal telescope plane alignment, presented in Figure 2.16b, reproduces the particle tracks by a straight line fitting. A good convergence between the fitted (Figure 2.16b) and the real (Figure 2.16a) tracks in the given example comes from a very simple misplacement (only one plane misplaced in only one axis) introduced for the plots clarity. In a real case, for a three-dimensional problem, the differences between the original and reconstructed tracks can be much more significant. For this reason, the alignment procedure is required to reproduce the testbeam telescope planes mutual positions.



a) Testbeam configuration, second plane misplaced in X axis by $dx_1 = 1$ mm. Two particle track registered

b) Simple track reconstruction assuming an ideal telescope plane alignment during data taking

Figure 2.16: Simplified, two-dimensional schemes illustrating the alignment problem.

A solution for the alignment issue can be searched for in Figure 2.16b. The hit positions in each plane differ from the track reconstructed by linear fit. If the fit corresponding to the particle track n is described as:

$$x_n(z) = a_n \cdot z + b_n \,, \tag{2.1}$$

the, so-called, residues δx_n^p can be calculated for each hit positions (x_n^p, z_n^p) in plane p as follows:

$$\delta x_n^p = x_n^p - x_n(z_n^p) = x_n^p - a_n z_n^p - b_n \,, \tag{2.2}$$

and the sum of residues Δx over all planes P (equal 3 in given example) and all tracks N (equal 2 in the example) can be calculated as:

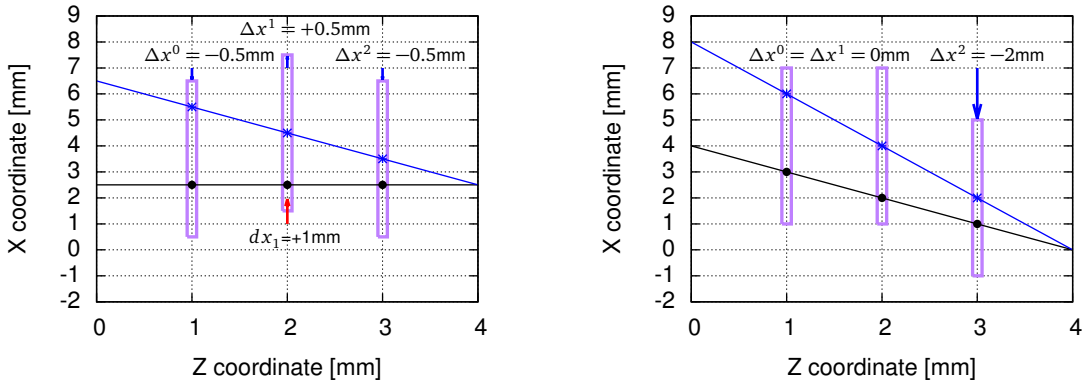
$$\Delta x = \sum_{n=0}^{N} \sum_{p=0}^{P} \left| \delta x_n^p \right| , \tag{2.3}$$

and treated as a metric demonstrating the telescope plane misplacement. One has to note, that for an ideal alignment, all the hit positions will be perfectly consistent with the fitted lines, resulting in $\Delta x = 0$.

To enable the alignment, each telescope plane p can be intentionally shifted (for clarity, only one-dimensional alignment in X axis will be considered) by Δx^p, resulting in new hits positions $(x_n^p, z_n^p) \rightarrow (x_n^p + \Delta x^p, z_n^p)$. As a next step, new linear fits can be performed, providing new fits coefficients $\widetilde{a_n}$, $\widetilde{b_n}$ for each track n. Then, the alignment metric can be recalculated as:

$$\begin{aligned} \widetilde{\Delta x}\left(\Delta x^0, \Delta x^1, ..., \Delta x^P\right) &= \sum_{n=0}^{N} \sum_{p=0}^{P} \left| \widetilde{\delta x_n^p} \right| = \sum_{n=0}^{N} \sum_{p=0}^{P} \left| \left(x_n^p + \Delta x^p\right) - \widetilde{x_n}(z_n^p) \right| = \\ &= \sum_{n=0}^{N} \sum_{p=0}^{P} \left| \left(x_n^p + \Delta x^p\right) - \widetilde{a_n} z_n^p - \widetilde{b_n} \right| . \end{aligned} \tag{2.4}$$

Since the ideal alignment is obtained for $\widetilde{\Delta x} = 0$, the above steps can be repeated using one of the numerous numerical minimizing algorithms in order to find the optimal Δx^p shift, corresponding to the minimum metric $\widetilde{\Delta x}$.



a) All planes shifted resulting in telescope position offset

b) Only third plane shifted resulting in rotation of the telescope coordinate system

Figure 2.17: Boundary examples of the alignment procedure results with minimized metric and amended telescope geometry.

One can expect that the above procedure restores the initial misalignment (shown in Figure 2.16a), corresponding to the set of optimized parameters $\left(\Delta x^0{=}0; \Delta x^1{=}dx_1{=}1; \Delta x^2{=}0\right)$[mm]. However, it has to be noted that, without any other constraints, an infinite number of possible solutions with minimum metric can be found. To illustrate this, two boundary cases, shown in Figure 2.17, are considered. Since the alignment procedure is sensitive only to mutual plane positions, an offset of the whole telescope can be introduced as it is illustrated in Figure 2.17a. The Δx^0 is equal to the Δx^2, the difference $\left(\Delta x^0 - \Delta x^1\right) = \left(\Delta x^2 - \Delta x^1\right) = 1$ mm (exactly equal to the initial misalignment $dx_1 = 1$ mm), while the whole telescope coordinate system is shifted by -0.5 mm. The less trivial case is presented in Figure 2.17b. Although $\Delta x^0 \neq \Delta x^2$ and $\left(\Delta x^0 - \Delta x^1\right) \neq \left(\Delta x^2 - \Delta x^1\right) \neq dx_1$, the minimum metric condition is met, resulting in effective telescope coordinate system rotation. In general, the final result of the presented alignment procedure is a linear combination of rotation and offset. Therefore, an additional condition is required in order to find the coordinate system transformation introduced by the alignment procedure, but only if the absolute telescope position needs to be preserved. It also should be noted that, contrary to the simplified example provided above, the real telescope alignment is a three-dimensional problem, since all the planes can be misplaced in all three axis.

Tracking and alignment

As can be seen from the above paragraphs, the tracking and alignment procedures cannot be separated. In the presented simplified alignment example, only one hit per plane per event was tacitly assumed, in order to disambiguate the track recognition and fitting. In real terms, in addition to the hits generated by the beam particle, a false hits appear, making the track reconstruction more complicated.

Assuming the ideal alignment of the telescope plane, the false hits problem can be easily solved. Since the particle tracks are a straight lines (and scattering can be neglected), the real hit positions in all telescope planes should be placed along these lines within a pixel-size precision. Contrary to this, a false hits should be generated in an uncorrelated manner (as they originate from noise), therefore a number of events in which the false hits in all planes can be connected with ideal straight line should be negligible. In such case, a tracking algorithm can be quite simple, as presented below.

Each point in the first plane may be connected to any point on the second plane to form a straight line. If the hits within a small, arbitrary chosen, radius around this line can be found in the two remaining planes, these four hits are associated together as a particle track. Without misalignment, the search radius can be small (comparable to single pixel size), what should be sufficient for false hit rejection.

However, to enable the alignment procedure for the real case, the search radius has to be significantly increased, in order to cover the planes misplacement (in the simplified example provided above (Figure 2.16b) the initial search precision has to be at least greater than 1 mm). In such case, also the false hits can be mistakenly associated as particle track. Since these hits are, in fact, uncorrelated, the fractional metric $\widetilde{\delta x_n}$ assigned to this false track should increase with decreasing misalignment, disturbing the metric minimization procedure. Therefore, the tracking and alignment procedures have to be performed alternately, with the track search condition tighten after each consecutive alignment step. Since each iteration decreases the initial misalignment, more false tracks can be rejected, improving the overall procedure accuracy. The presented steps are repeated until a requested alignment precision is met.

Custom tracking and alignment procedure

A complete tracking and alignment software was provided by the Aarhus University in collaboration with Strasbourg University, together with amendments introduced by the Tel Aviv University. Though the software, in general, follows the algorithm presented in the previous sections, it has to be treated as a "black-box" procedure providing a ready-to-use, aligned and reconstructed beam particle tracks. In order to verify it, a custom tracking and alignment procedure was developed too.

The already presented tracking algorithm was used for the track recognition. Also the alignment utilizes, in general, the presented algorithm, however a more sophisticated procedure was developed, since, at it was already mentioned, the more complex three-dimensional problem has to be considered in a real case. Since all the particle tracks are distributed along the Z axis (in particular, track cannot be perpendicular to it), they can be described as a function of z coordinate, $(x_n, y_n) = f_n(z)$. In that case, a complex three-dimensional problem can be simplified, since the X and Y axis are mutually perpendicular, what allows to decompose the $(x_n, y_n) = f_n(z)$ function into two independent components $\{x_n = f_{x,n}(z); y_n = f_{y,n}(z)\}$. Hence, a multiple one-dimensional fit (equation 2.1) can be calculated as:

$$\begin{cases} x_n(z) = a_{x,n} \cdot z + b_{x,n} \\ y_n(z) = a_{y,n} \cdot z + b_{y,n} \end{cases}, \tag{2.5}$$

providing a two fractional residues for each hit position (x_n^p, y_n^p, z_n^p) in plane p, derived from equation 2.2, as:

$$\begin{cases} \delta x_n^p = x_n^p - x_n(z_n^p) = x_n^p - a_{x,n} \cdot z_n^p - b_{x,n} \\ \delta y_n^p = y_n^p - y_n(z_n^p) = y_n^p - a_{y,n} \cdot z_n^p - b_{y,n} \end{cases}. \tag{2.6}$$

By changing the designations:

$$\begin{array}{lll} x_n(z) \to \varepsilon_{x,n} & y_n(z) \to \varepsilon_{y,n} & \\ x_n^p \to \rho_{x,n}^p & y_n^p \to \rho_{y,n}^p & z_n^p \to \rho_{z,n}^p \\ \Delta x^p \to \Delta\chi_x^p & \Delta y^p \to \Delta\chi_y^p & \Delta z^p \to \Delta\chi_z^p \,, \end{array}$$

equations 2.6 can be written as:

$$\delta\rho^p_{i,n} = \rho^p_{i,n} - \varepsilon_{i,n}(\rho^p_{z,n}) = \rho^p_{i,n} - a_{i,n}\cdot\rho^p_{z,n} - b_{i,n}, \qquad i \in (x,y), \tag{2.7}$$

leading to a three-dimensional metric defined as:

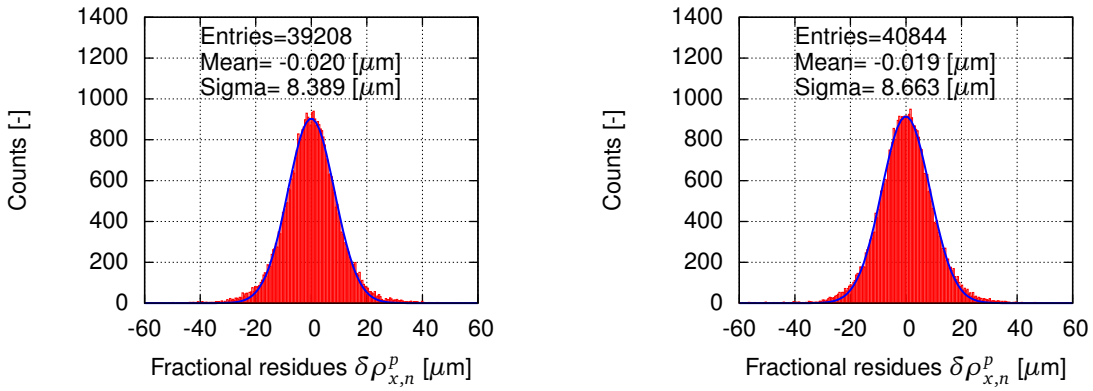
$$\Delta\rho = \sum_{i}^{x,y}\sum_{n=0}^{N}\sum_{p=0}^{P}\left|\delta\rho^p_{i,n}\right| . \tag{2.8}$$

Similarly to a one-dimensional case, a three-dimensional shift vectors $(\Delta\chi^p_x, \Delta\chi^p_y, \Delta\chi^p_z)$ can be introduced for each plane p. As it was previously shown, a coordinate system offset can be introduced by the alignment procedure. To preserve the offset in Z axis, in order to keep the telescope relative distance to the LumiCal unchanged, the $\Delta\chi^0_z$ parameter was fixed. Then, the alignment procedure metric becomes a function of 11 free parameters and can be derived from 2.4 as:

$$\begin{aligned}\widetilde{\Delta\rho}(\Delta\chi^0_x, \Delta\chi^0_y; \Delta\chi^1_x, \Delta\chi^1_y, \Delta\chi^1_z; \ldots; \Delta\chi^3_x, \Delta\chi^3_y, \Delta\chi^3_z) &= \sum_{i}^{x,y}\sum_{n=0}^{N}\sum_{p=0}^{3}\left|\widetilde{\delta\rho^p_{i,n}}\right| = \\ = \sum_{i}^{x,y}\sum_{n=0}^{N}\sum_{p=0}^{3}&\left|(\rho^p_{i,n} + \Delta\chi^p_i) - \widetilde{a_{i,n}}\cdot(\rho^p_{z,n} + \Delta\chi^p_z) - \widetilde{b_{i,n}}\right|.\end{aligned} \tag{2.9}$$

The telescope alignment can be therefore found by minimization of this metric. Since it is not possible to determinate derivatives of the proposed metric, an optimization method using only the function values is required. In this case, a Powell's method (a conjugate direction method) [71] was used. The final telescope alignment was obtained by alternating tracking and alignment procedures.

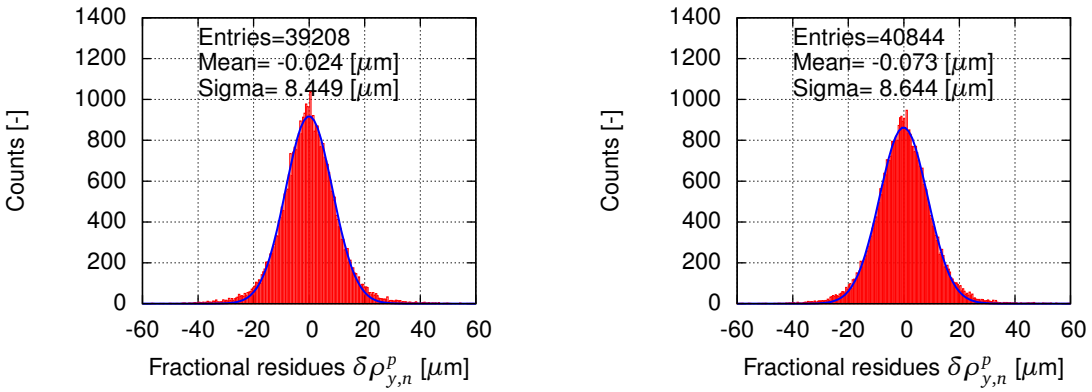
To measure the alignment quality, the distributions of a fractional residues $\delta\rho^p_{i,n}$, for all planes p and tracks n together, can be calculated for X and Y axis independently. The histograms for X axis ($\delta\rho^p_{x,n}$) and Y axis ($\delta\rho^p_{y,n}$) are presented in Figures 2.18 and 2.19, respectively. The fractional residues calculated for tracks obtained from the original "black-box" procedure are presented on the left, while the ones calculated with custom procedure on the right. Since the results obtained using both methods are very similar, the tracks reconstructed by the original "black-box" software were used in the further analysis.



a) Original, "black-box" alignment procedure

b) Custom alignment procedure

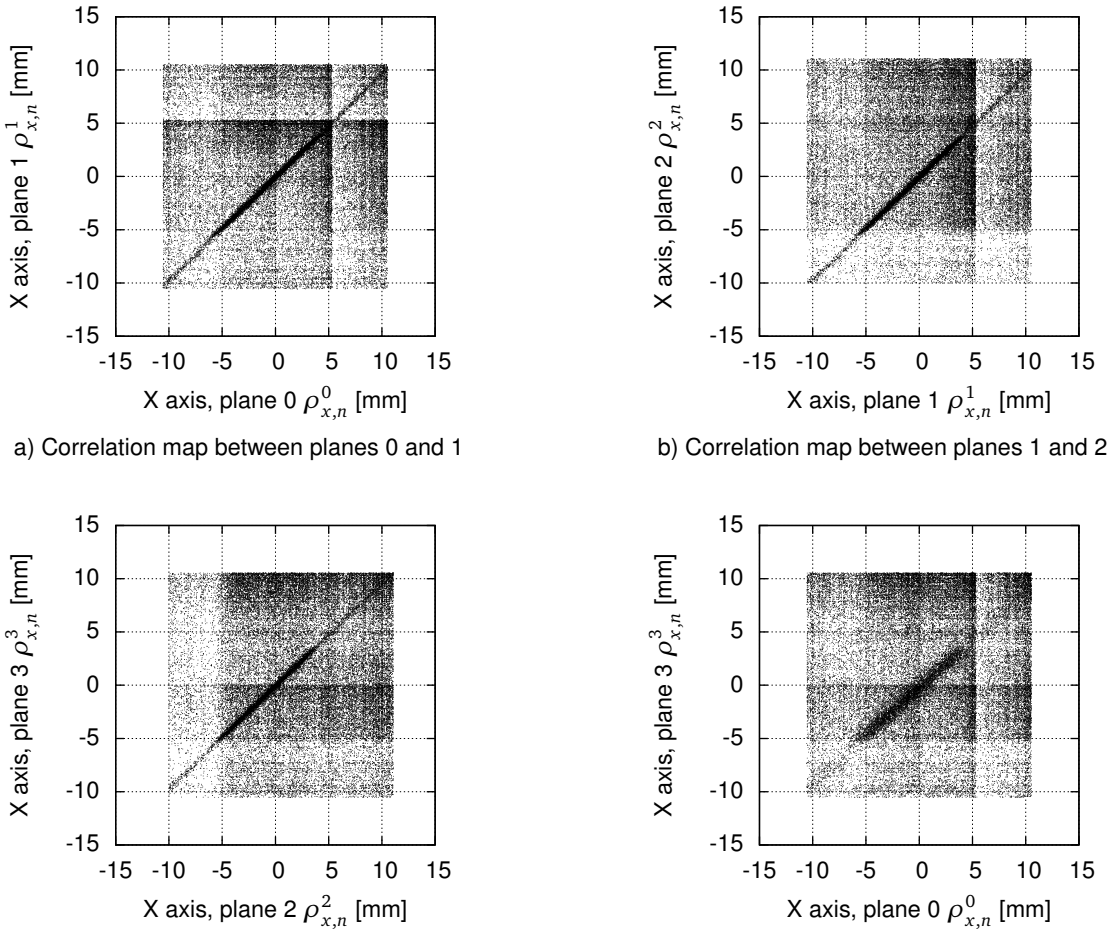
Figure 2.18: Histograms of a fractional residues $\delta\rho^p_{x,n}$ (X axis) distribution.



a) Original, "black-box" alignment procedure

b) Custom alignment procedure

Figure 2.19: Histograms of a fractional residues $\delta\rho^p_{y,n}$ (Y axis) distribution.



a) Correlation map between planes 0 and 1

b) Correlation map between planes 1 and 2

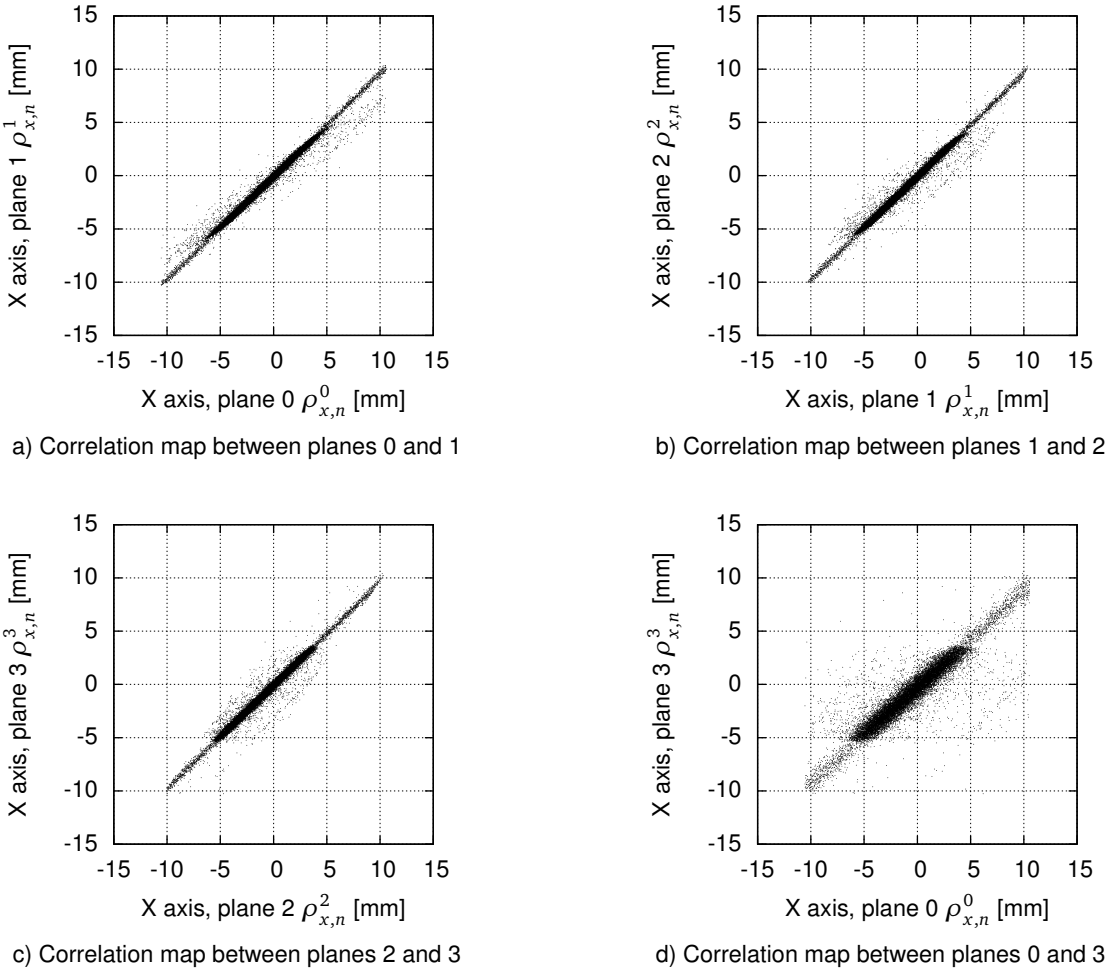
c) Correlation map between planes 2 and 3

d) Correlation map between planes 0 and 3

Figure 2.20: Correlation maps between X axis hit coordinates ($\rho^p_{x,n}$) in different telescope planes for the raw data.

Tracking performance

In order to estimate the performance of tracking algorithm, correlation maps between $\rho^p_{i,n}$ hit coordinates in different telescope planes can be calculated. The correlation maps of $\rho^p_{x,n}$ coordinate (X axis) for neighboring telescope planes (0 and 1, 1 and 2, 2 and 3) and correlation map between first and last plane (0 and 3) after alignment for the raw data are presented in Figure 2.20. Aside the expected linear correlation, corresponding to the real particles tracks, large regions can be found with high rate of false noisy hits. The location of these regions remains in a very good agreement with the histograms presented in Figure 2.15. On the contrary to the correlation maps for the raw data, the maps created for the reconstructed tracks, presented in Figure 2.21, show very good correlation indicating a very efficient false hits rejecting capability of the tracking procedure.



a) Correlation map between planes 0 and 1

b) Correlation map between planes 1 and 2

c) Correlation map between planes 2 and 3

d) Correlation map between planes 0 and 3

Figure 2.21: Correlation maps between X axis hit coordinates ($\rho^p_{x,n}$) in different telescope planes for the reconstructed tracks.

As the final check, the hit-maps for the reconstructed tracks are shown in Figure 2.22. Contrary to the raw data hit-maps, shown in Figure 2.15, the beam profile can be clearly seen for the reconstructed tracks. In particular, the distribution for the last telescope plane (Figure 2.22d) remains in a very good agreement with the hole in the anti-coincidence scintillator (since it was mounted directly upstream that plane - see Figure 2.11). Also the scintillation process efficiency problem, dis-

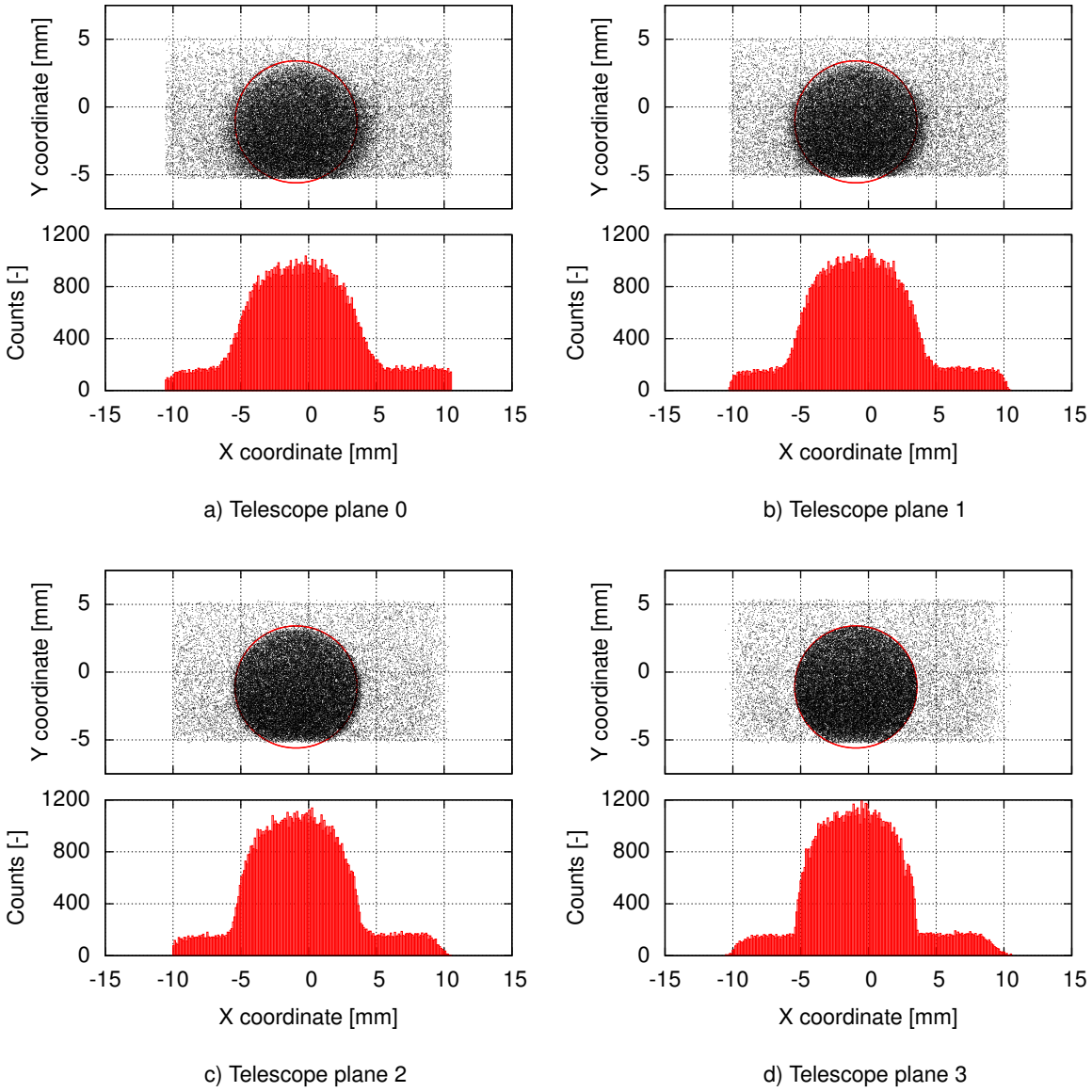
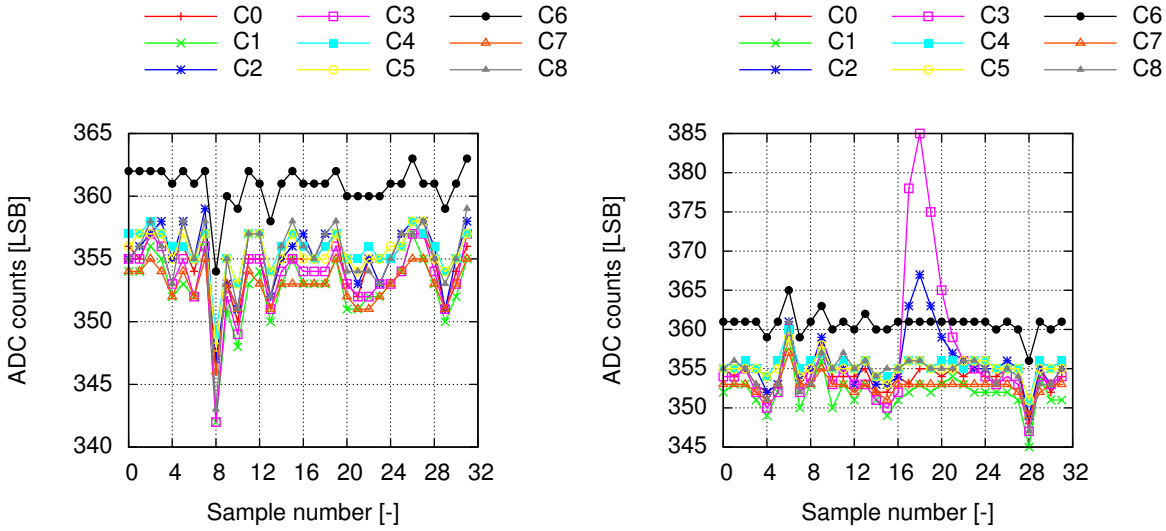


Figure 2.22: Maps of the tracks telescope hits (after data processing, top) together with X axis histograms (bottom). The red circle represents the hole in the anti-coincidence scintillator.

cussed already in the previous section, can be clearly seen in Figure 2.22d. The average number of tracks passing the hole was estimated above 95 %, in good agreement with the expected scintillation efficiency. The reconstructed telescope tracks were afterwards used for the position reconstruction analysis, presented in section 2.3.3.

2.2.2 Time and amplitude reconstruction

Since the beams provided by the PS and DESY II accelerators are continuous (i.e. there is no clock associated with the incoming particles), the LumiCal readout module utilizes an asynchronous sampling mode, as it was described in sections 1.4.1 and 1.4.2. However, one has to note that the example of continuous, asynchronous sampling of the front-end response, shown in Figure 1.22,



a) Example of event without signal

b) Example of event with signal (channels C2 and C3)

Figure 2.23: Example of a raw LumiCal data. Only nine channels (C0–C8) are presented for clarity.

is very simplified and does not include various aspects affecting the readout response. Contrary to this idealized image, an example of real raw data collected during the testbeam is presented in Figure 2.23. For clarity, only nine channels C0–C8 are shown. Since the expected event rate was rather low, 32 ADC samples per event were collected in order to boost the data processing. The two major problems can be clearly seen in Figure 2.23 - the front-end output constant value, so-called pedestal or baseline, varies between channels, mainly due to the spread of the front-end parameters, typical for sub-micron technologies. Especially the channel C6 pedestal differs significantly from the others in the given example. However, this problem can be easily resolved by the pedestal removal procedure, described in details below.

The second, even more important problem, is connected to common mode disturbances. Apart from the pedestal spread, the baseline of each channel should, in ideal case, vary in time only due to the noise generated in the readout chain. Since the noise generated in different channels is uncorrelated, also the baseline variations in different channels should be uncorrelated. However, even without detailed analysis, a strong correlations between channel baselines can be clearly seen in the presented example, e.g. on the 8th sample in Figure 2.23a, or between samples 3rd and 16th in Figure 2.23b. A common mode variations are mostly caused by disturbances and fluctuations of some parameters, like power supply voltage, affecting the baselines in separate channels in the same way. To illustrate the scale of this problem in the given LumiCal readout system, one can compare the amplitude of common mode disturbance at sample 6 in Figure 2.23b, of around 10 LSB, to the signal amplitude at channel C2, slightly lower than 20 LSB. Since the disturbance reaches above 50 % of the signal amplitude, an efficient CMS procedure is required.

Pedestal removal and Common Mode Subtraction (CMS)

Since the front-end baseline value depends on various parameters, e.g. the ASIC temperature, it can vary in a larger time interval depending on changes of these parameters. The chosen record of 32 ADC samples per event allows calculation of the pedestal value in each event independently. As can

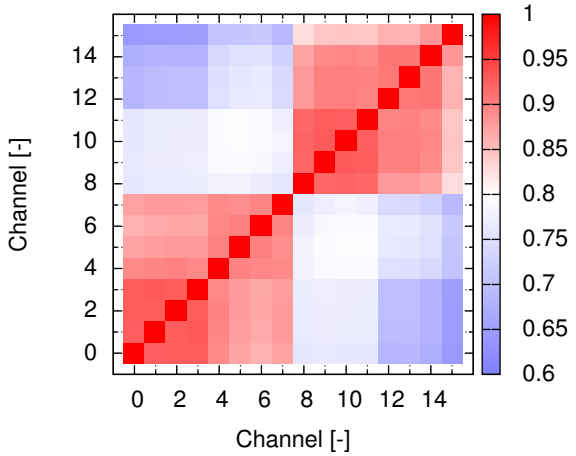
be seen from Figure 2.23b, the trigger position in the event was set to around 17th sample, and so the pedestal P_n^k of channel k in event n can be calculated as an average of the first fourteen samples as follows:

$$P_n^k = \frac{1}{14}\sum_{i=0}^{13} S_{i,n}^k \,, \tag{2.10}$$

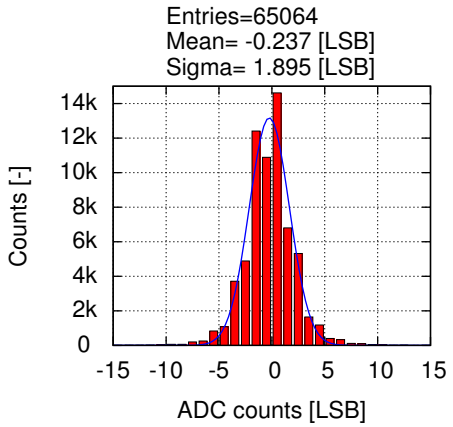
where $S_{i,n}^k$ is sample i from event n in channel k. The average pedestal value is then subtracted from all the samples $(S_{0,n}^k, S_{1,n}^k, ..., S_{31,n}^k)$:

$$\overline{S_{i,n}^k} = S_{i,n}^k - P_n^k \qquad \forall_{i\in(0,1,..31)} \,, \tag{2.11}$$

resulting in the events comprising data with baselines equalized to zero.



a) Correlation coefficients for baseline samples for 16 channels



b) Exemplary baseline histogram of arbitrary chosen channel 9

Figure 2.24: Correlation coefficients for baseline samples for 16 channel and an exemplary baseline histogram for one channel for raw data after pedestal removal.

In order to estimate the correlation between different channel baselines, a Pearson product-moment correlation coefficient [72, 73] was calculated. An exemplary map of these coefficients calculated for 16 channels (two ASICs) is presented in Figure 2.24a. A very clearly distinguishable areas, related to two separate 8-channel ASICs, can be easily found. Within each ASIC the coefficients remain above 0.8 indicating a very strong correlations between baseline samples. The correlations between channels from separate ASICs are weaker, but still quite high since the coefficients remain above 0.6. Within each ASIC a two separate regions, related to two groups of four channels with different gain, can also be found. The channels with the same gain are clearly more correlated to each other than to the ones with different gain. A histogram presenting the baseline variations after pedestal subtraction is presented in Figure 2.24b. The sigma of Gaussian fit, slightly below two Least Significant Bits (LSBs), was obtained in this case. A proper CMS procedure should decrease this value even more.

Contrary to the pedestal removal procedure, where the mean pedestal is calculated as an average over time (sample number i) for fixed channel k, the mean common mode CM_n^i in event n is an

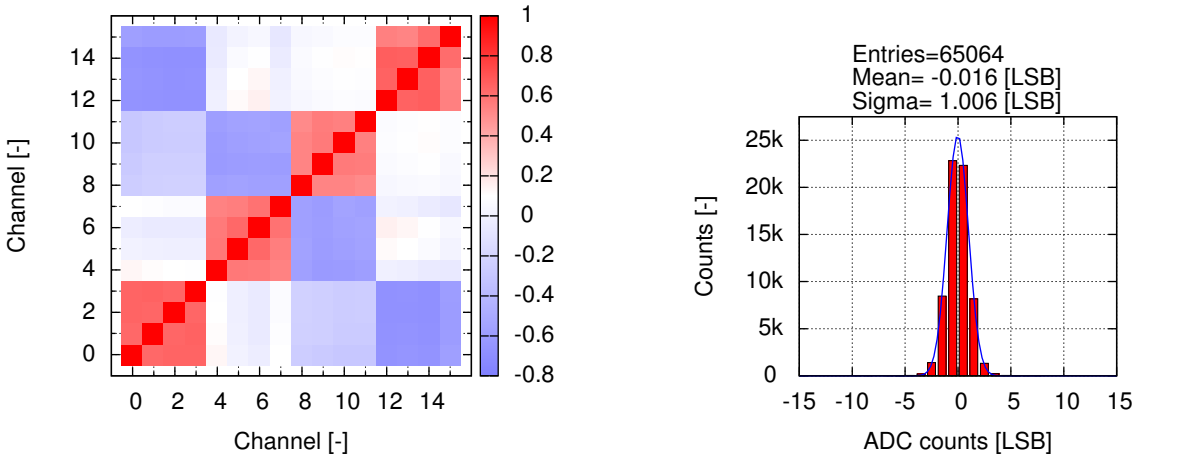
average over channels for fixed sample number i, as follows:

$$CM_n^i = \frac{1}{(k_e - k_s)} \sum_{k=k_s}^{k_e} S_{i,n}^k \ . \tag{2.12}$$

Analogously to the pedestal removal procedure, the mean common mode is subtracted from sample i in each channel k in range (k_s, k_e):

$$\widetilde{S_{i,n}^k} = \overline{S_{i,n}^k} - CM_n^i \qquad \forall_{k\in(k_s,\ k_s+1,\ldots,\ k_e)} \ . \tag{2.13}$$

Since the common mode subtraction procedure increases the statistical (uncorrelated) noise to $\widetilde{\sigma}$ according to $\widetilde{\sigma}^2 = \sigma^2 + \sigma^2/K$, where σ is noise Root Mean Square (RMS) and $K = (k_e - k_s)$ is number of channels taken to estimate the mean common mode, one should expect that higher K value should improve the procedure performance. It is true, assuming that all channels behave in similar way, which is not true for the analyzed data, for which different patterns exist for different groups of channels, as seen in Figure 2.24a.



a) Correlation coefficients for baseline samples for 16 channels

b) Exemplary baseline histogram of arbitrary chosen channel 9

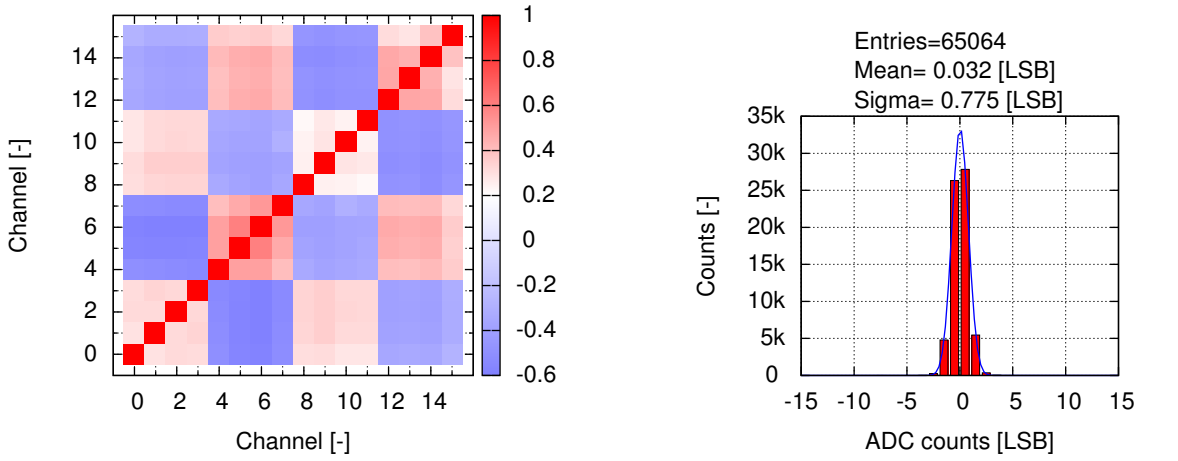
Figure 2.25: Correlation coefficients for baseline samples for 16 channel and an exemplary baseline histogram for one channel for mean common mode calculated for all 32 channels altogether.

In order to verify the influence of the range (k_s, k_e) of channels taken for the mean common mode CM_n^i calculation, three cases are considered. In the first one, a single value of mean common mode is calculated for all 32 channels, i.e. $(k_s, k_e) = (0, 31)$, resulting in highest possible $K = 32$. The result of this type common mode subtraction is shown in Figure 2.25. The sigma of the baseline histogram, presented in Figure 2.25b, is almost two times smaller then the one obtained for the data just after pedestal removal procedure. However, a correlation coefficients map, shown in Figure 2.25a, indicates that this procedure is not fully efficient, since a very strong positive correlation (with coefficient above 0.6) can still be found within groups of four equal-gain channels, while a strong negative correlations (coefficient below -0.5) are introduced between different ASICs, especially for channels with different gains. This can be understood since these groups were initially weakly correlated (see Figure 2.24a), therefore the subtraction of the same mean common mode value introduces a negative correlation.

To avoid introducing of negative correlations between separate ASICs, a second case of CMS procedure can be considered. In this case, the mean common mode is calculated independently for each ASIC, i.e. four mean common mode values CM_n^i are calculated in channels ranges:

$$(k_s, k_e) \in [(0,7);\ (8,15);\ (16,23);\ (24,31)]\ . \tag{2.14}$$

The results of this CMS procedure are presented in Figure 2.26. The sigma of the baseline histogram (Figure 2.26b) is reduced compared to the first case, and it is 2.5 times smaller than the initial one. The correlations between channels with the same gain, even in separate ASICs, were significantly reduced, with the coefficients below 0.3, although a strong negative correlations were introduced within each ASIC between channels with different gain.



a) Correlation coefficients for baseline samples for 16 channels

b) Exemplary baseline histogram of arbitrary chosen channel 9

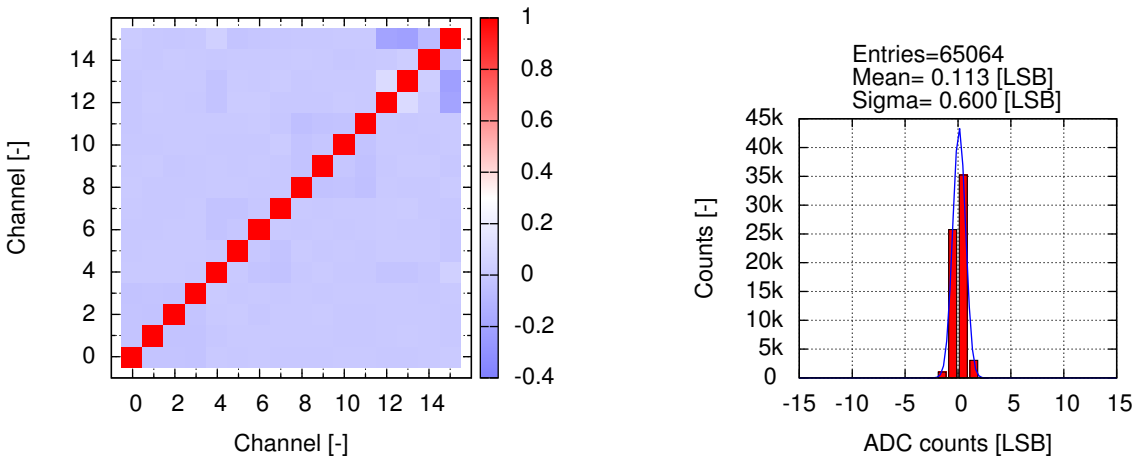
Figure 2.26: Correlation coefficients for baseline samples for 16 channel and an exemplary baseline histogram for one channel for mean common mode calculated for each ASIC independently (4 groups of 8 channels each).

From the above results, as well as from the initial correlation map (Figure 2.24a), the third CMS case can be inferred, with the mean common mode calculated for each group of equal-gain channels independently, i.e. eight CM_n^i values calculated in channels ranges:

$$(k_s, k_e) \in [(0,3);\ (4,7);\ (8,11);\ (12,15);\ (16,19);\ (20,23);\ (24,27);\ (28,31)]\ . \tag{2.15}$$

In this case $K = 4$, so the CMS procedure is expected to increase the uncorrelated noise level to $\tilde{\sigma}^2 = 1.25\sigma^2$. Since the uncorrelated noise level is significantly lower than the common mode disturbances, therefore a better CMS performance may be more important than the uncorrelated noise level increase. The results obtained for this case are presented in Figure 2.27. The resulting coefficients map (Figure 2.27a) shows a uniform pattern of a weak negative correlations. The sigma of baseline histogram (Figure 2.27b), equals 0.6 LSB, is more than 3 times lower then the initial one, and it is the smallest of all hitherto obtained. The results indicate that, despite of very low statistics (only 4 channels) and the uncorrelated noise level increase, this method provides the best common mode rejection capability, therefore it is used as a default CMS procedure for the LumiCal data processing.

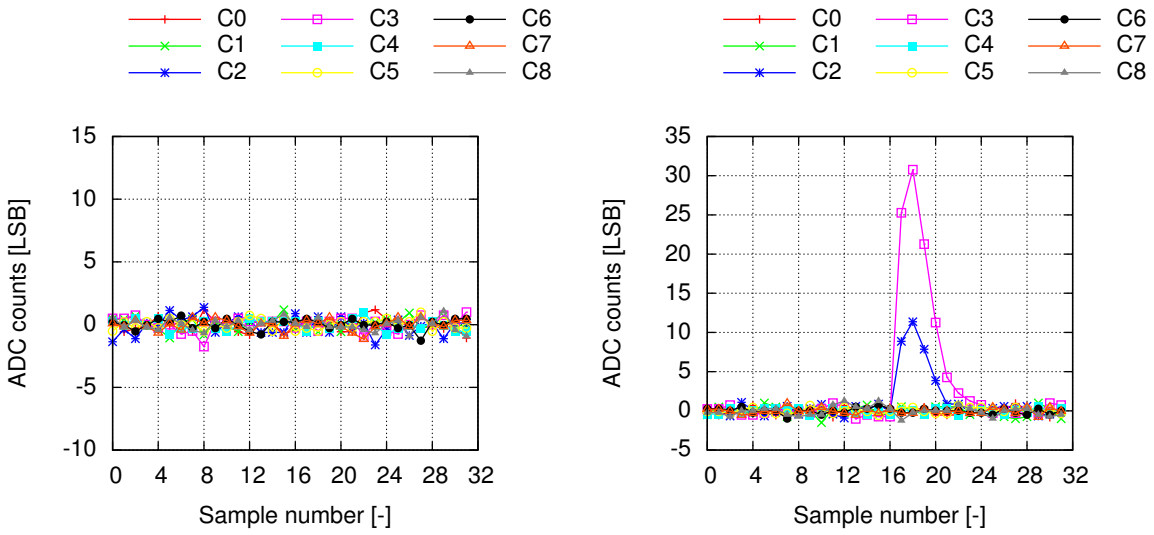
In order to illustrate the pedestal removal and CMS procedure results, an exemplary raw data, presented in Figure 2.23, is shown in Figure 2.28 after initial processing.



a) Correlation coefficients for baseline samples for 16 channels

b) Exemplary baseline histogram of arbitrary chosen channel 9

Figure 2.27: Correlation coefficients for baseline samples for 16 channel and an exemplary baseline histogram for one channel for mean common mode calculated for each equal-gain channels group in each ASIC independently (8 groups of 4 channels each).



a) Example of event without signal

b) Example of event with signal (channels C2 and C3)

Figure 2.28: Examples of a LumiCal data after pedestal removal and CMS procedures. Only nine channels (C0–C8) are presented for clarity.

Deconvolution method

The initial data processing, described in previous section, prepares the LumiCal data for the main part of signal reconstruction. As it was already described in Section 1.4.1, the charge deposited in active sensor volume is directly proportional to the front-end pulse amplitude. Since the LumiCal readout utilizes an asynchronous ADC sampling scheme, the pulse amplitude is not directly available from the initially processed data and, therefore, has to be reconstructed. The simplest reconstruction

algorithm is based on a theoretical pulse shape fitting, e.g. using the least squares method. The time response of the complete front-end chain, for a general $CR-(RC)^n$ shaping, is given by formula 1.23. The particular LumiCal front-end utilizes a simple $CR-RC$ shaping, for which the formula 1.23 simplifies to the form:

$$|\mathrm{V}_{\mathrm{front-end}}(t)| = \frac{\mathrm{q_{in}}}{\mathrm{C_{feed}}}\left(\frac{t}{\tau_{\mathrm{sh}}}\right)e^{-\frac{t}{\tau_{\mathrm{sh}}}} , \tag{2.16}$$

with the maximum value given as:

$$\mathrm{V}^{\mathrm{max}}_{\mathrm{front-end}} = \mathrm{V}_{\mathrm{front-end}}(T_{peak}) = \frac{\mathrm{q_{in}}}{\mathrm{C_{feed}}}\cdot\frac{1}{e} . \tag{2.17}$$

In such case, a function $p(t)$, given by the formula:

$$p(t) = \begin{cases} b & \text{for } t < t_0 \\ \alpha\left(\frac{t-t_0}{\tau_{\mathrm{sh}}}\right)e^{-\frac{t-t_0}{\tau_{\mathrm{sh}}}} + b & \text{for } t \geq t_0 , \end{cases} \tag{2.18}$$

can be fitted to the each pulse via α, b, t_0 parameters in order to reconstruct the pedestal b, pulse start time t_0 and pulse amplitude $A = (\alpha/e)$. However, the pulse fitting is a rather slow procedure which requires an initial guess of the fit parameters set, and due to the required complex calculations can be done only during the offline computer analysis. In addition, its complexity would be even higher if pile-up effects were included.

In order to enable a fast amplitude reconstruction, a deconvolution method, proposed for pulse processing in HEP experiments at the beginning of 90's [74], was proposed for the LumiCal readout. The great advantage of this method is the possibility to implement it inside the system DSP block, reducing significantly the total amount of data transmitted from the detector. Since the output pulse of the front-end electronics is a convolution of its pulse response with the sensor current signal (and so, deposited charge), an inverse procedure, so-called deconvolution, can be performed in order to reconstruct the input signal. Initially the deconvolution method was implemented in early 90's in Analog Pipeline Voltage (APV) ASIC for the CMS experiment at LHC, where it was performed by an analogue pulse shape processor [75]. Nowadays, with the ADC integrated in each readout channel, the deconvolution can be performed in digital manner using digital filters.

The digital filters are very common blocks of modern DSP systems. Similarly to their analogue counterparts, they attenuate or amplify certain bands of frequencies, although they operate on discrete-time, discrete-value samples instead of continuous ones, used in analogue filters. The most common architectures of digital filters are Finite Impulse Response (FIR) filter, Infinite Impulse Response (IIR) filter and an Adaptive Digital Filter [76]. The first one has the simplest architecture, performing a simple weighted average (convolution) of the series of N data samples. The IIR has a recursive linear architecture, with each output sample depending on both the series of N data samples and the previous output samples. In other words, the IIR architecture comprises a feedback circuit and, therefore, this architecture is most similar to the analogue filters. The Adaptive Digital Filter has a most sophisticated architecture which can learn and adapts itself to a desired signal.

The output sample s_k of the simplest FIR architecture filter can be expressed, in general, as:

$$s_k = \sum_{i=0}^{N-1} w_i v_{k-i} , \tag{2.19}$$

where w_i represents weight associated to input sample v_{k-i}. The filter order depends on the length N of the series of data samples, therefore a higher order filter requires a more processing power

for its implementation. Since the deconvolution filter has to represent the inverse front-end pulse response function, a higher $CR-(RC)^n$ shaping utilized in the shaper induces a higher order of FIR filter. Therefore, a simple $CR-RC$ shaping was implemented in the LumiCal front-end electronics in order to reduce the complexity of the deconvolution filter. Since the transfer function $H(s)$ of the $CR-RC$ shaper can be derived from 1.20 by putting $n=1$, the front-end response $V_{sh}(s)$ in a Laplace domain can be expressed as:

$$V_{sh}(s) = \frac{1}{s}\cdot H(s) = \frac{\tau_{\mathrm{sh}}}{(1+s\tau_{\mathrm{sh}})^2} = \frac{1}{\tau_{\mathrm{sh}}}\cdot\frac{1}{\left(s+\frac{1}{\tau_{\mathrm{sh}}}\right)^2}\ . \tag{2.20}$$

Aside the constant $(1/\tau_{\mathrm{sh}})$ factor, the deconvolution filter transfer function $D(s)$ is therefore given by:

$$D(s) = \frac{1}{V_{sh}(s)} \cong \left(s+\frac{1}{\tau_{\mathrm{sh}}}\right)^2 = (s-s_0)^2\ . \tag{2.21}$$

Such kind of transfer function, comprising only a double zero and no poles, cannot be easily implemented in analogue circuitry, although, it may be easily achieved in discrete-time domain. To transform the $D(s)$ from a continuous domain s into a discrete domain z, a Z transform, utilizing a pole-zero mapping technique, can be used. In such case, each S-plane pole (or zero) s_0 is replaced by z_0 in Z-plane according to:

$$z_0 = e^{s_0 T_{smp}}\ , \tag{2.22}$$

where T_{smp} is sampling period. The formula 2.21, comprising double zero $s_0 = -1/\tau_{\mathrm{sh}}$, can be transformed in $D(z)$ as follows:

$$D(z) = (z-z_0)^2 = \left(z-e^{-\frac{T_{smp}}{\tau_{\mathrm{sh}}}}\right)^2 = z^2 - 2e^{-\frac{T_{smp}}{\tau_{\mathrm{sh}}}}z + e^{-\frac{2T_{smp}}{\tau_{\mathrm{sh}}}}\ . \tag{2.23}$$

Since z^2 represents the sample which will be received after two sampling periods in the future, equation 2.23 can be multiplied by z^{-2}, what corresponds to delaying all the samples by two periods, resulting in the final equation:

$$D(z) = 1 - 2e^{-\frac{T_{smp}}{\tau_{\mathrm{sh}}}}z^{-1} + e^{-\frac{2T_{smp}}{\tau_{\mathrm{sh}}}}z^{-2}\ , \tag{2.24}$$

where z^{-1} is a unit delay corresponding to the sample taken one sampling period before the current one. The output sample value d_i, obtained at time $i\cdot T_{smp}$, can be expressed from 2.24 as:

$$d_i = v_i - 2e^{-\frac{T_{smp}}{\tau_{\mathrm{sh}}}}v_{i-1} + e^{-\frac{2T_{smp}}{\tau_{\mathrm{sh}}}}v_{i-2}\ , \tag{2.25}$$

where v_i is the shaper output sample taken at time $i\cdot T_{smp}$, i.e.:

$$v_i = V_{sh}(i\cdot T_{smp})\ . \tag{2.26}$$

From the comparison of formulas 2.19 and 2.25 it can be seen that the deconvolution filter is a second order FIR filter with the weights given as:

$$w_0 = 1\ , \qquad w_1 = -2e^{-\frac{T_{smp}}{\tau_{\mathrm{sh}}}}\ , \qquad w_2 = e^{-\frac{2T_{smp}}{\tau_{\mathrm{sh}}}}\ . \tag{2.27}$$

For the chosen $CR-RC$ shaping the deconvolution filter requires only two multiplications and two additions. The weights depend only on the ratio between sampling period T_{smp} and shaper time constant τ_{sh}, which for a given readout is constant. Therefore, the deconvolution can be performed

online as a part of the DAQ system, either by the on-board FPGA or even by the System-on-Chip (SoC) readout ASIC.

Based on formula 2.25, the deconvolution filter response to the front-end pulse given by equation 2.18 can be calculated. In order to simplify the equations, the pulse pedestal b can be set to zero. Since the pedestal removal procedure is performed as an initial data processing, this assumption is well-motivated and does not result in loss of generality. One has to note, that, in general, the pulse starting time t_0 has to be located within $[0, T_{smp})$ range. Since the whole sampling-filtering process is periodical, the pulse starting time lower than zero, or $\geq T_{smp}$, corresponds to the case of the pulse beginning one sample earlier or later than the considered one, respectively. In other words, the pulse starting time equal to $t_0 + k \cdot T_{smp}$ can be treated as a pulse beginning at t_0 in reference to the sample k. Based on these assumptions, the consecutive shaper output samples can be expressed as:

$$\begin{aligned}
v_{-1} &= 0 \\
v_0 &= 0 \\
v_1 &= Ae\frac{T_{smp}-t_0}{\tau_{\mathrm{sh}}}e^{-\frac{T_{smp}-t_0}{\tau_{\mathrm{sh}}}} \\
v_2 &= Ae\frac{2T_{smp}-t_0}{\tau_{\mathrm{sh}}}e^{-\frac{2T_{smp}-t_0}{\tau_{\mathrm{sh}}}} \\
&\ldots \\
v_k &= Ae\frac{kT_{smp}-t_0}{\tau_{\mathrm{sh}}}e^{-\frac{kT_{smp}-t_0}{\tau_{\mathrm{sh}}}} \\
&\ldots ,
\end{aligned} \tag{2.28}$$

resulting in the consecutive deconvolution filter samples given by:

$$\begin{aligned}
d_{-1} &= w_{-1}v_{-1} + w_{-2}v_{-2} + w_{-3}v_{-3} = 0 \\
d_0 &= w_0v_0 + w_{-1}v_{-1} + w_{-2}v_{-2} = 0 \\
d_1 &= w_1v_1 + w_0v_0 + w_{-1}v_{-1} = Ae\frac{T_{smp}-t_0}{\tau_{\mathrm{sh}}}e^{-\frac{T_{smp}-t_0}{\tau_{\mathrm{sh}}}} \\
d_2 &= w_2v_2 + w_1v_1 + w_0v_0 = Ae\frac{2T_{smp}-t_0}{\tau_{\mathrm{sh}}}e^{-\frac{2T_{smp}-t_0}{\tau_{\mathrm{sh}}}} - \\
&- \left[2e^{-\frac{T_{smp}}{\tau_{\mathrm{sh}}}}\right]\cdot\left[Ae\frac{T_{smp}-t_0}{\tau_{\mathrm{sh}}}e^{-\frac{T_{smp}-t_0}{\tau_{\mathrm{sh}}}}\right] = Ae\frac{t_0}{\tau_{\mathrm{sh}}}e^{-\frac{2T_{smp}-t_0}{\tau_{\mathrm{sh}}}} \\
d_k\Big|_{k>2} &= w_kv_k + w_{k-1}v_{k-1} + w_{k-2}v_{k-2} = Ae\frac{kT_{smp}-t_0}{\tau_{\mathrm{sh}}}e^{-\frac{kT_{smp}-t_0}{\tau_{\mathrm{sh}}}} - \\
&- \left[2e^{-\frac{T_{smp}}{\tau_{\mathrm{sh}}}}\right]\cdot\left[Ae\frac{(k-1)T_{smp}-t_0}{\tau_{\mathrm{sh}}}e^{-\frac{(k-1)T_{smp}-t_0}{\tau_{\mathrm{sh}}}}\right] + \\
&+ \left[e^{-\frac{2T_{smp}}{\tau_{\mathrm{sh}}}}\right]\cdot\left[Ae\frac{(k-2)T_{smp}-t_0}{\tau_{\mathrm{sh}}}e^{-\frac{(k-2)T_{smp}-t_0}{\tau_{\mathrm{sh}}}}\right] = \\
&= Ae\frac{1}{\tau_{\mathrm{sh}}}e^{-\frac{kT_{smp}-t_0}{\tau_{\mathrm{sh}}}}\left[kT_{smp}-t_0-2(k-1)T_{smp}+2t_0+(k-2)T_{smp}-t_0\right] \equiv 0 .
\end{aligned} \tag{2.29}$$

As can be seen from equations 2.29, the deconvolution filter produces only two non-zero samples d_k for asynchronous sampling of the $CR-RC$ pulse. If all three input samples v_i are located on zeroed baseline, or on the pulse, the filter output sample d_k is always equal to zero. The non-zero

samples d_k are produced only in case where at least one input sample v_i is located on baseline and the remaining one or two are located on the pulse. In the exceptional case of a synchronous sampling only one non-zero output sample d_k is produced. This can be derived from equations 2.29 by setting the $t_0 = 0$ what corresponds to the input pulse synchronized to the sampling clock. In this case, the output samples d_k are given as:

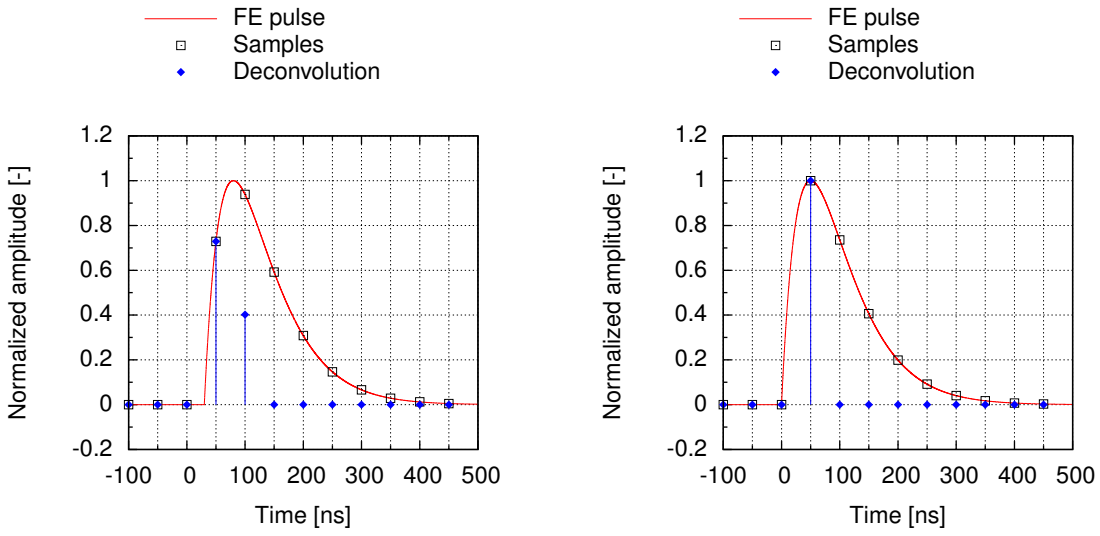
$$\begin{aligned} d_k\Big|_{k<1} &= 0 \\ d_1 &= Ae\frac{T_{smp}-0}{\tau_{\mathrm{sh}}}e^{-\frac{T_{smp}-0}{\tau_{\mathrm{sh}}}} = Ae\frac{T_{smp}}{\tau_{\mathrm{sh}}}e^{-\frac{T_{smp}}{\tau_{\mathrm{sh}}}} \\ d_k\Big|_{k>1} &= 0\,. \end{aligned} \tag{2.30}$$

Some additional simplification can be done in the synchronous case by setting the sampling period exactly equal to the shaper time constant, i.e. $T_{smp} = \tau_{\mathrm{sh}}$. In such case, the one non-zero sample d_1 directly represents the pulse amplitude since:

$$d_1 = Ae\frac{\tau_{\mathrm{sh}}}{\tau_{\mathrm{sh}}}e^{-\frac{\tau_{\mathrm{sh}}}{\tau_{\mathrm{sh}}}} = Ae\cdot e^{-1} = A\,. \tag{2.31}$$

In a more general case of $T_{smp} \neq \tau_{\mathrm{sh}}$ the pulse amplitude can be calculated from equation 2.30 as:

$$A = d_1 \cdot \frac{\tau_{\mathrm{sh}}}{T_{smp}}e^{\frac{T_{smp}-\tau_{\mathrm{sh}}}{\tau_{\mathrm{sh}}}}\,. \tag{2.32}$$



a) Example of asynchronous sampling with two non-zero filter output samples at $t_0 = 30$ ns

b) Example of synchronous sampling with only one non-zero filter output sample at $t_0 = 0$ ns

Figure 2.29: Examples of deconvolution filter output at $T_{smp} = \tau_{\mathrm{sh}} = 50$ ns.

The example responses of the deconvolution filter (blue diamonds) to the sampled (black squares) front-end pulse response (red line) are shown in Figure 2.29 for $T_{smp} = \tau_{\mathrm{sh}} = 50$ ns. In the asynchronous case, with $t_0 = 30$ ns (Figure 2.29a), the two non-zero samples are produced. In the case of synchronous sampling (Figure 2.29b) only one non-zero sample, directly representing the pulse maximum, is produced as described by equations 2.30 and 2.31.

In the asynchronous sampling case, described by equations 2.29, the ratio of the two samples is given by:

$$\frac{d_2}{d_1} = \frac{t_0}{T_{smp} - t_0} e^{-\frac{T_{smp}}{\tau_{\mathrm{sh}}}} , \tag{2.33}$$

enabling the reconstruction of the pulse starting time t_0 for the given T_{smp} and τ_{sh}. From equation 2.33, the reconstructed pulse starting time t_0 can be expressed as:

$$t_0 = \frac{\frac{d_2}{d_1} T_{smp}}{\frac{d_2}{d_1} + e^{-\frac{T_{smp}}{\tau_{\mathrm{sh}}}}} . \tag{2.34}$$

In order to obtain the equation enabling the reconstruction of the pulse amplitude, the sum of two non-zero samples d_1, d_2 can be calculated as follows:

$$d_1 + d_2 = \frac{A}{\tau_{\mathrm{sh}}} e^{-\frac{T_{smp} - t_0 - \tau_{\mathrm{sh}}}{\tau_{\mathrm{sh}}}} \left[T_{smp} - t_0 \left(1 - e^{-\frac{T_{smp}}{\tau_{\mathrm{sh}}}} \right) \right] . \tag{2.35}$$

The pulse amplitude A can be obtained from equation 2.35 as:

$$\begin{aligned} A &= (d_1 + d_2) \frac{\tau_{\mathrm{sh}} e^{\frac{T_{smp} - t_0 - \tau_{\mathrm{sh}}}{\tau_{\mathrm{sh}}}}}{T_{smp} - t_0 \left(1 - e^{-\frac{T_{smp}}{\tau_{\mathrm{sh}}}} \right)} = \\ &= (d_1 + d_2) \left[\frac{\tau_{\mathrm{sh}}}{T_{smp}} e^{\frac{T_{smp} - \tau_{\mathrm{sh}}}{\tau_{\mathrm{sh}}}} \right] \frac{e^{\frac{-t_0}{\tau_{\mathrm{sh}}}}}{1 - \frac{t_0}{T_{smp}} \left(1 - e^{-\frac{T_{smp}}{\tau_{\mathrm{sh}}}} \right)} . \end{aligned} \tag{2.36}$$

As can be seen from the above equation, the pulse amplitude is given by the sum of two samples multiplied by the time dependent correction factor. Apart from sampling period T_{smp} and shaper time constant τ_{sh}, this factor depends on the reconstructed pulse starting time t_0. One should note that in the synchronous sampling case the second output sample $d_2 \equiv 0$ and equation 2.34 provides a properly reconstructed $t_0 = 0$, and, equation 2.36 reduces to 2.32. This shows, that the synchronous sampling does not have to be considered as a separate, special case, since the equations 2.34 and 2.36, derived for the general asynchronous sampling provide a proper results for any t_0 in range $[0, T_{smp})$, covering at the same time the synchronous sampling case $t_0 = 0$.

The time dependent correction factor has to be used in order to enable the precise pulse amplitude reconstruction, as can be seen from equation 2.36. However, the amplitude can be roughly estimated using only the normalized sum of two non-zero samples $\alpha \cdot (d_1 + d_2)$. The normalization coefficient α, resulting from the sampling period to the shaper time constant ratio $T_{smp}/\tau_{\mathrm{sh}}$, is given as:

$$\alpha = \frac{\tau_{\mathrm{sh}}}{T_{smp}} e^{\frac{T_{smp} - \tau_{\mathrm{sh}}}{\tau_{\mathrm{sh}}}} . \tag{2.37}$$

The normalized sum of two non-zero samples $\alpha \cdot (d_1 + d_2)$ (without time dependent correction factor) for the normalized pulse amplitude as a function of normalized pulse starting time t_0/T_{smp}, is shown in Figure 2.30 for various $T_{smp}/\tau_{\mathrm{sh}}$ ratios. For sampling periods shorter than the shaper time constant the maximum discrepancy between the normalized sum of samples and the pulse amplitude A does not exceed few percents. In the particular case of $T_{smp} = \tau_{\mathrm{sh}}$, the maximum deviation slightly exceeds 13 %, and grows with the increasing $T_{smp}/\tau_{\mathrm{sh}}$ ratio. The calculated values of maximum deviation are shown in Table 2.4. The LumiCal readout utilizes the front-end with effective peaking

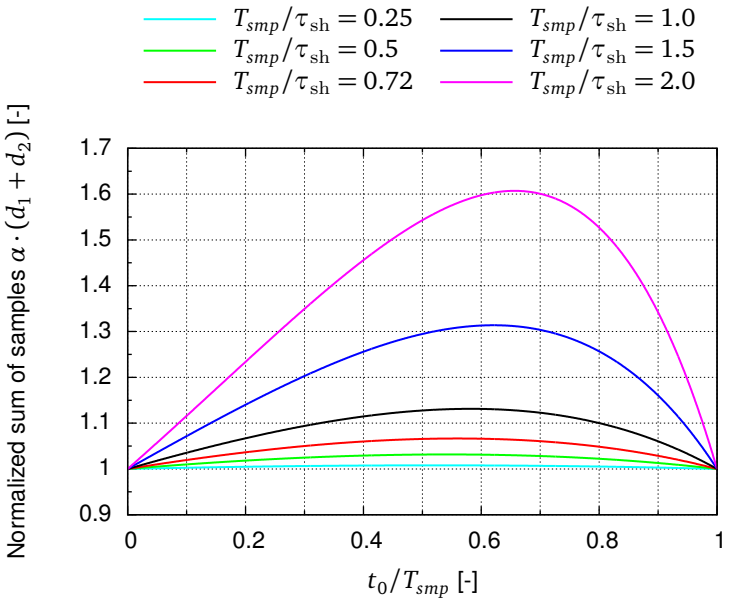


Figure 2.30: Normalized sum of two non-zero samples $\alpha(d_1 + d_2)$ (without time dependent correction factor) for different sampling periods T_{smp}.

T_{smp}/τ_{sh}	Maximum deviation [%]	t_0/T_{smp} of the maximum deviation
0.25	0.78	0.52
0.50	3.16	0.54
0.72	**6.65**	**0.56**
1.00	13.12	0.58
1.50	31.37	0.62
2.00	60.72	0.66

Table 2.4: Maximum deviations between normalized sum of two non-zero samples and the pulse amplitude for different sampling periods.

time slightly below 70 ns and the ADC sampling period of 50 ns. This results in T_{smp}/τ_{sh} ratio of around 0.72, corresponding to the maximum deviation below 7 %.

The above considerations become important when a real pulse, comprising noise and common mode disturbances, is being deconvoluted. In the ideal case, shown in Figure 2.29, all baseline samples are equal, since the noise contribution was not considered. Assuming, for simplicity, that the noise introduced by the front-end electronics has an infinite bandwidth, the pulse starting time t_0, reconstructed using equation 2.34, can obtain any value in range $(-\infty, +\infty)$. For the band-limited noise, together with finite front-end and ADC dynamic ranges, the possible pulse starting time t_0 range, obtained for the noise samples, is also limited, although much wider than the theoretical one ($t_0 \in [0, T_{smp}]$). If only the amplitude of front-end pulse is of interest, the pulse starting time t_0, calculated for any pair of two samples, can stand as initial criterion for the front-end pulse discrimination (i.e. only the pairs which result in $t_0 \in [0, T_{smp}]$ are further processed). However, in order to investigate the SNR after deconvolution process, the noise level has to be somehow estimated. Since the time dependent correction factor (equation 2.36) cannot be used for $t_0 \notin [0, T_{smp}]$, the normalized sum of samples $\alpha(d_1 + d_2)$ can be taken in order to approximate the noise. Since for the given LumiCal readout the condition $T_{smp} = 0.72\tau_{sh}$ is met, the maximum approximation error does not exceed 7 %, which is acceptable value for the noise estimation. Moreover, the normalized sum

of samples is greater (or at least equal) than the real value (as can be seen in Figure 2.30), so the noise level is overestimated, and never underestimated.

The example of the deconvolution procedure for a real LumiCal pulse, after pedestal removal and CMS procedures (channel C3 signal from Figure 2.23b), is presented in Figure 2.31. The top graph presents the sampled input pulse (red squares) with the deconvolution filter output samples (blue dots). The front-end pulse is represented after deconvolution by two non-zero samples, as expected from theory. However, the remaining samples are not exactly zero, due to the noise and common

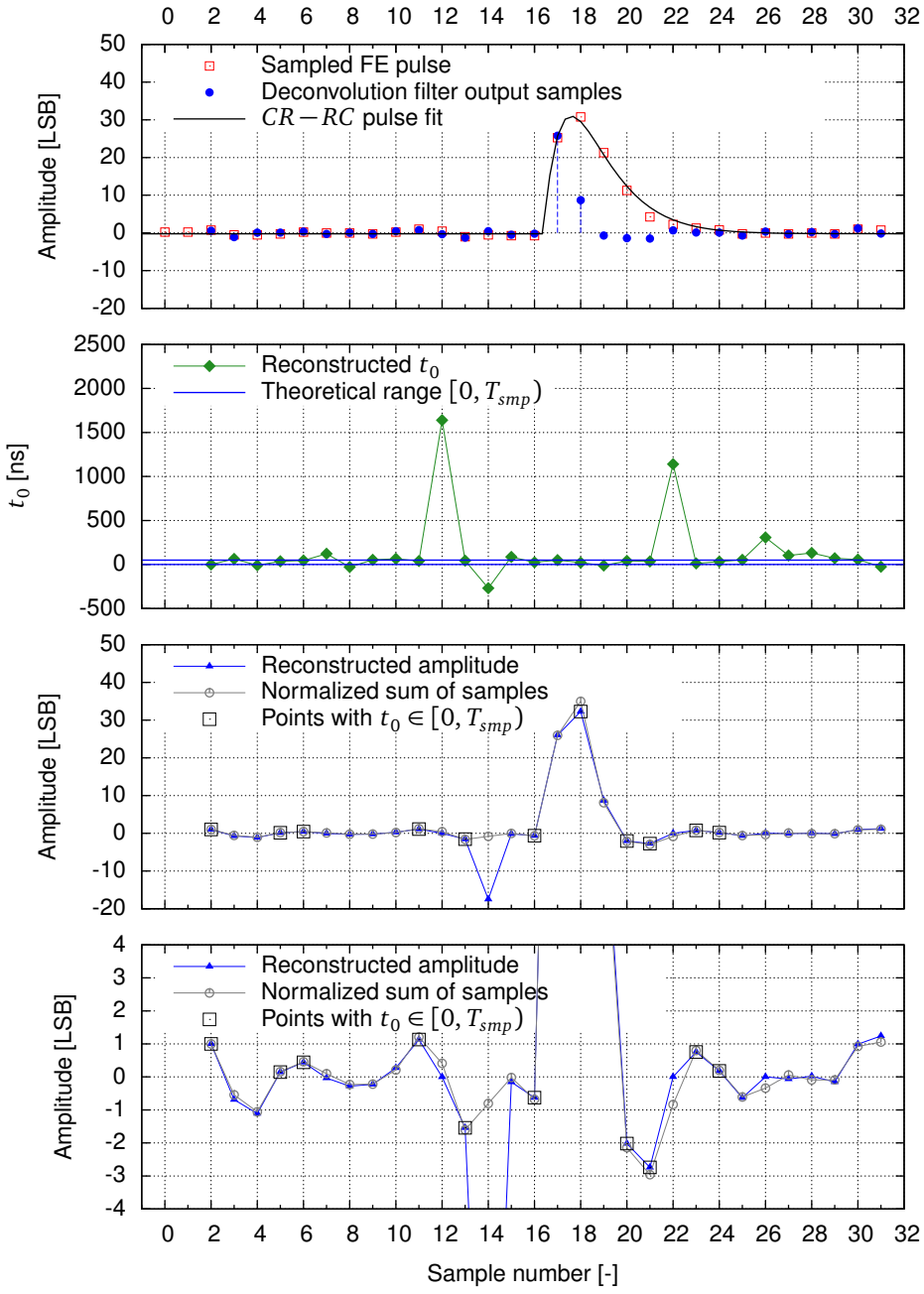


Figure 2.31: Example of the deconvolution results for real LumiCal pulse.

mode disturbances. This affects the reconstructed pulse starting time t_0, shown in the middle graph as green diamonds. The theoretical range of $[0, 50)$ ns, shown as blue lines, is exceeded by an order of magnitude for some samples. The reconstructed amplitude (with time dependent correction factor) is presented on the bottom plots as blue triangles while the normalized sum of samples – as gray circles. The points with $t_0 \in [0, T_{smp})$ are marked using black rectangles.

Due to negative sign of t_0 in the exponent of the time dependent correction factor (equation 2.36), a high positive value of t_0 makes the correction factor extremely small. Therefore, the amplitude reconstructed for a very high value of $t_0 \approx 1600$ (12th sample) is almost zeroed. Contrary to this, a negative $t_0 \approx -400$ (14th sample) increases significantly the correction factor, and the amplitude reconstructed for this sample is significantly lower than the average pedestal. In this case, the normalized sum of samples should be taken as a proper value of the 14th sample.

The theoretical $CR{-}RC$ pulse, given by equation 2.18, was fitted to the sampled front-end pulse. This fit is presented on top graph in Figure 2.31 as a black solid line. The pulse amplitude obtained from the fit is equal 31.82 ± 0.6 LSB, while the one reconstructed by the deconvolution process – 32.27 LSB. The pulse starting time t_0, achieved in both methods is also very similar, 20.5 ± 1.5 ns from the fit and 21.81 ns from the deconvolution. The convergence of the two results indicates that the deconvolution can be used for the amplitude reconstruction instead of the slow, sensitive to initial conditions, theoretical pulse fitting.

In addition to the benefits in single pulse amplitude reconstruction, the deconvolution improves the pile-up resolving capability, since the digital filter shortens effectively the pulse length [66]. However, due to low particle rate in the testbeam, the total number of pile-up-ed events was negligible. Therefore, since this problem is marginal for the performed data analysis, the deconvolution pile-up resolving capability is not discussed in this dissertation.

2.3 Testbeam results

All of the steps, discussed in Section 2.2, form a complete signal processing chain, providing the results enabling the physical data analysis. Apart from the telescope track reconstruction, described already in details, the LumiCal data processing consist of pedestal removal, CMS, deconvolution and final signal extraction procedure. The above steps were implemented in a dedicated software as a chain described in details below.

2.3.1 Initial data processing and noise performance

Initial data processing chain

The average pedestal is calculated for each channel in each event independently from the first fourteen samples, together with the corresponding standard deviation σ_{raw}. The average pedestal is then subtracted from all 32 samples of each channel in each event. The calculated standard deviation σ_{raw} is used in order to discriminate the channels containing the real sensor signal from the CMS procedure. As can be seen from Figure 2.23, common mode disturbances usually contain a single sample very far from the average pedestal, while the signal contains a few consecutive samples above the pedestal. Therefore, to exclude the real signal from the CMS procedure, without detecting mistakenly the common disturbance as a signal, the discrimination criterion was taken as follow: if at least two consecutive samples exceeds the $3\sigma_{raw}$ level, the channel is treated as containing

the real signal and excluded from the CMS procedure. In such case, the average common mode is calculated for each sample in each event, for 8 groups of the same-gain channels, as it was already described, and subtracted. After the initial processing, the first fourteen samples from each channel of each event in the given configuration, for each board separately, are divided into two data series (depending on the channel gain), in order to prepare the noise histograms for each board in the given configuration. Since two different gains (see Section 1.4.2) are implemented in each front-end ASIC, the signals are processed separately for the channels with lower (16 channels per board) and higher (also 16 channels per board) gain, until the gain unification procedure.

The initially processed data are deconvoluted using the procedure described in previous section. The deconvolution is calculated for all 32 samples data set of each channel in each event, in order to enable the noise performance comparison. Similarly to the initially processed data, the first twelve samples (each deconvolution sample needs three signal samples) from each channel of each event in a given configuration, for each board separately, are divided into two data series (depending on the channel gain), representing the overall board noise after deconvolution process. Due to the low beam particle rate the pile-up-ed events can be neglected, therefore each 32 samples length data set should correspond to one (or none) front-end pulse. In next step a single value, representing the pulse amplitude (or noise sample if no charge was deposited in the given channel), should be extracted from the data set for each channel in each event. Although the system trigger was done to set the pulse maximum at 17th sample, the maximum value position varies between 17th and 18th sample, due to the delay fluctuations in the trigger path.

The pulse maximum can be found from the position of two non-zero samples, provided by the deconvolution filter. However, as can be seen from Figure 2.31, all of the samples are in fact non-zero, due to noise and disturbances. Therefore, a standard deviation σ_{deconv} can be calculated for the first twelve deconvolution filter samples, and a discrimination criterion of a two consecutive samples above $3\sigma_{deconv}$ can be used in order to determinate the signal position. Based on this, the 17th or 18th sample of reconstructed amplitude is taken for the further analyze. If the signal cannot be found in the given channel, the 17th sample, representing the noise, is taken in order to keep the noise information.

System noise performance

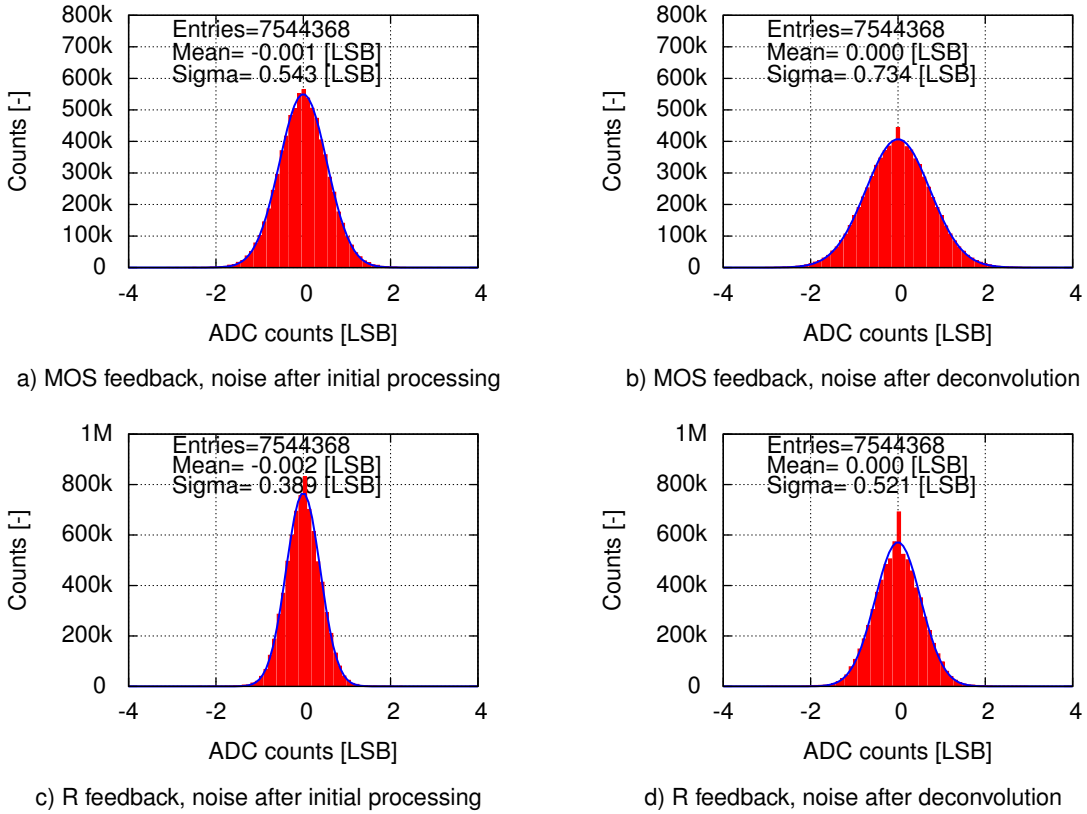
In order to assess the system noise as well as the performance of the deconvolution procedure, the noise distributions, before and after the deconvolution, were calculated based on the data sets prepared in the initial processing. In order to unambiguously distinguish the readout boards, a unique IDentification Number (IDN), generated automatically by the hardware, was assigned to each of them. The correspondence between sensors (S0-S3 in Figure 2.7, Table 2.1) and readout boards was kept unchanged during the whole testbeam, therefore a board unique IDNs will be used from now on to label the results. The correspondence between the sensor number and the board IDN is presented in Table 2.5.

Sensor number	Board IDN
S0	IDN63
S1	IDN64
S2	IDN67
S3	IDN76

Table 2.5: Correspondence between sensor number and unique board IDN.

		Higher gain channels (MOS feedback)		Lower gain channels (R feedback)	
Configuration	Board	After initial processing	After deconvolution	After initial processing	After deconvolution
1	IDN63	0.542 ± 0.002	0.731 ± 0.002	0.390 ± 0.002	0.522 ± 0.004
	IDN64	0.583 ± 0.003	0.792 ± 0.005	0.405 ± 0.002	0.538 ± 0.006
	IDN67	0.551 ± 0.005	0.746 ± 0.007	0.417 ± 0.004	0.556 ± 0.007
	IDN76	0.558 ± 0.005	0.759 ± 0.008	0.402 ± 0.002	0.536 ± 0.007
2	IDN63	0.543 ± 0.002	0.734 ± 0.003	0.389 ± 0.003	0.521 ± 0.007
	IDN64	0.588 ± 0.005	0.794 ± 0.007	0.407 ± 0.003	0.539 ± 0.007
	IDN67	0.549 ± 0.004	0.737 ± 0.008	0.423 ± 0.004	0.558 ± 0.008
	IDN76	0.552 ± 0.005	0.746 ± 0.007	0.398 ± 0.002	0.528 ± 0.007
3	IDN63	0.545 ± 0.003	0.737 ± 0.005	0.391 ± 0.004	0.525 ± 0.008
	IDN64	0.592 ± 0.006	0.797 ± 0.009	0.407 ± 0.004	0.540 ± 0.008
	IDN67	0.547 ± 0.005	0.738 ± 0.008	0.425 ± 0.003	0.564 ± 0.008

Table 2.6: σ of the Gaussian function fitted to the noise distributions before and after deconvolution. All values are expressed in [LSB].



a) MOS feedback, noise after initial processing

b) MOS feedback, noise after deconvolution

c) R feedback, noise after initial processing

d) R feedback, noise after deconvolution

Figure 2.32: Board IDN63 noise performance in the second configuration.

The exemplary distributions with Gaussian fit for the board IDN63 in the second configuration are shown in Figure 2.32. The detailed plots, for all boards in all configurations, are presented in Appendix A. The σ of the Gaussian fit, corresponding to the noise RMS values, are presented in Table 2.6. As can be seen, the deconvolution process increases the noise RMS value by around 35 %. The noise RMS values after initial processing matches the exemplary one presented for the CMS

procedure (Figure 2.27b), confirming the generality of these considerations. Since the noise samples after the deconvolution process are obtained using exactly the same procedure as the signal, the noise RMS values obtained from these distributions can be used for the SNR considerations, presented in the following section.

2.3.2 Board gain calibration

Test pulse calibration

All the data (pulse amplitudes and noise samples), collected during the testbeam and initially processed, are expressed in LSB. In order to reconstruct the charge depositions, corresponding to the extracted pulse amplitudes, the readout gain, expressed in LSB/fC, has to be determined. The gain can be measured in a direct, not correlated with the real data, way, by injecting the test pulses directly to the front-end inputs through the test capacitance. The product of the chosen test pulse amplitude and test capacitance results in the charge value injected into the front-end electronics. The front-end response, sampled and converted by the ADC, is then measured. Therefore, the ratio of the signal response, expressed in LSB, to the injected charge (in fC), gives the gain. The gain calibration values, obtained using the described procedure after the testbeam, are presented in Table 2.7. The gain is uniform for boards IDN63, IDN64 and IDN67. However, the gain of the board IDN76, damaged during the testbeam, is significantly lower. This may indicate that not all parameters affected by the FPGA malfunctioning were restored. This shows one of the cons of such boards calibration method – since the gains are measured in different environments, the values obtained in laboratory measurements can differ from the testbeam ones. Moreover, the injected gain calculation bases on an absolute value of the test capacitance. Although the matching (ratio) between capacitances (or resistances), provided by the modern CMOS technologies, is very well determined, their absolute values can vary in a wide range, even tens of percents. Since the test capacitance is built-in inside the front-end ASIC, its exact value cannot be determined, affecting the gain measurements. At last, but not least, this measurement method does not include the silicon sensor, neglecting all the additional charge collection effects.

	Board gain [LSB/fC]	
Board IDN	Higher gain (MOS feedback)	Lower gain (R feedback)
IDN63	3.01	1.45
IDN64	3.07	1.48
IDN67	3.02	1.45
IDN76	2.64	1.26

Table 2.7: Boards gain obtained by the test pulse injecting procedure.

Muon peak calibration

Since the secondary beam provided by the PS contains the muons, the boards gain can be determined in a more precise manner. The muons, interacting with matter very weakly, do not initiate the electromagnetic shower inside the LumiCal, but are traversing the detector with almost unchanged energy. Due to weak interactions, the muons act as MIPs with energy deposition inside 300 μm thick silicon sensor given by the Landau distribution (1.15), with the MPV of around 4.1 fC [46]. Therefore, an energy spectrum of a single readout channel (independently from the number of absorber

layers upstream the given sensor) contains a peak representing the charge deposited by the muons and the channel gain can be determined by finding the MPV of Landau distribution. Since the signal amplitudes are expressed in LSB, the MPV is given in the same unit, providing the gain in LSB/MIP.

Since the expected SNR for the MIPs is of the order of ten in the given readout, the noise introduced by the front-end electronics affects significantly the muon signal. Though the energy deposition in silicon sensor is given by a pure Landau distribution (1.15), the electronic noise (given by the Gaussian distribution) widens the muon peak. Therefore, in order to reconstruct the MPV of muon deposition, a convolution of Gaussian and Landau distributions (called hereinafter the LanGau distribution) has to be fitted.

In order to enable a most accurate gain calibration, the muon MPV should be fitted to the energy spectrum of each channel independently. However, since the triggered events were limited spatially by the hole scintillator (Figures 2.13 and 2.22), only a few channels gathered the sufficient statistics enabling the precise LanGau distribution fits. Since the gain between the channels is acceptably uniform [66], an average gain per board can be calculated from the energy spectrum of all equal-gain channels. The exemplary energy spectra for the board IDN63 in the second configuration are presented in Figure 2.33. The detailed plots, for all boards in all configurations, are presented in Appendix A. The obtained gains are summarized in Table 2.8.

		Higher gain (MOS feedback)		Lower gain (R feedback)	
Conf.	Board	Gain [LSB/MIP]	Gain [LSB/fC]	Gain [LSB/MIP]	Gain [LSB/fC]
1	IDN63	10.92 ± 0.08	2.66 ± 0.02	5.14 ± 0.04	1.25 ± 0.01
	IDN64	11.46 ± 0.20	2.79 ± 0.05	5.04 ± 0.05	1.23 ± 0.01
	IDN67	11.02 ± 0.09	2.69 ± 0.02	4.62 ± 0.04	1.13 ± 0.01
	IDN76	9.92 ± 0.67	2.42 ± 0.16	4.88 ± 0.03	1.19 ± 0.01
2	IDN63	11.61 ± 0.15	2.83 ± 0.04	5.03 ± 0.02	1.23 ± 0.01
	IDN64	11.56 ± 0.18	2.82 ± 0.04	5.08 ± 0.04	1.24 ± 0.01
	IDN67	10.62 ± 0.09	2.59 ± 0.02	4.25 ± 0.18	1.04 ± 0.04
	IDN76	10.58 ± 0.21	2.58 ± 0.05	4.91 ± 0.03	1.20 ± 0.01
3	IDN63	11.39 ± 0.13	2.78 ± 0.03	5.10 ± 0.06	1.24 ± 0.02
	IDN64	11.95 ± 0.21	2.91 ± 0.05	5.05 ± 0.03	1.23 ± 0.01
	IDN67	11.01 ± 0.07	2.69 ± 0.02	4.55 ± 0.04	1.11 ± 0.01

Table 2.8: Boards gain obtained from the LanGau fits to the muon peak of the channels energy distributions.

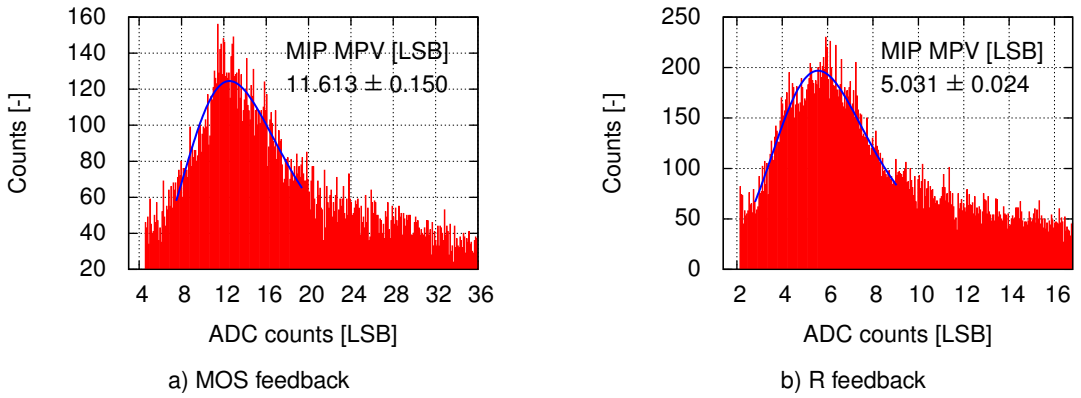


Figure 2.33: Channels energy distribution with convolution of Landau and Gauss distributions fitted to the muon peak for board IDN63 in the second configuration.

The achieved gains are rather uniform within the fit uncertainties. The ratio between gains of MOS and R feedback channels, of around 2.27, is well in line with the theoretical gain ratio, resulting from the design capacitances (see Section 1.4.2), equal to (0.5 pF)/(0.23 pF) = 2.17. The gain varies in range (9.92–11.95) [LSB/MIP] for channels with higher gain and (4.25–5.14) [LSB/MIP] for channels with lower gain. The gains are noticeably lower than the ones obtained by the calibration pulse method (Table 2.7). A possible reason can be underestimated value of the test capacitance. The gain variations and particular cases of large uncertainties results from low statistics of the collected energy distributions. In order to estimate the shower development measurement uncertainties, the average spread of MIP MPVs was assessed to 5 % of its value.

Signal-to-Noise Ratio (SNR)

Using the achieved MIP MPV (Table 2.8) and noise RMS after deconvolution process (Table 2.6), the SNR for each board in each configuration can be calculated as:

$$SNR = \frac{\text{MIP MPV [LSB]}}{RMS_{NOISE}\text{[LSB]}} \,. \tag{2.38}$$

In order to estimate the SNR before the deconvolution process, the above calculations can be performed for the noise RMS after initial processing. Though the MIP MPV before deconvolution was not determined, the presented convergence of amplitude reconstruction using the deconvolution and the $CR-RC$ pulse fit, allow to approximate the SNR after initial processing as a ratio of MIP MPV achieved from deconvolution to the noise RMS after initial processing. The calculated SNRs, both after initial processing and deconvolution, are presented in Figure 2.34.

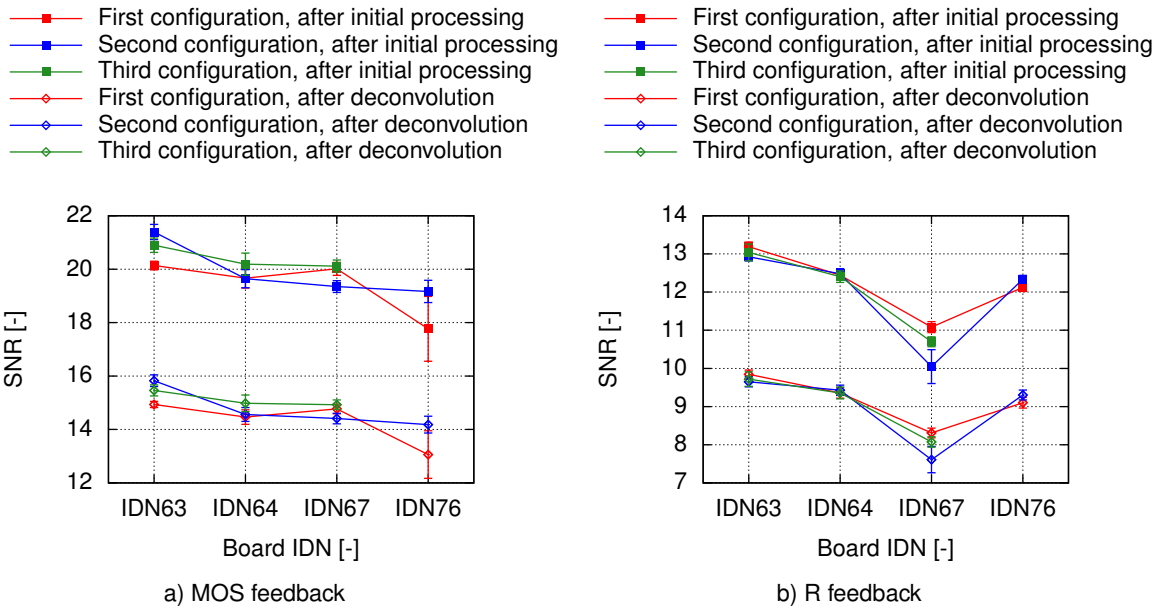


Figure 2.34: Detailed SNR of all boards in all configurations.

The SNR of the R feedback channels (with lower gain) is substantially lower than for the MOS feedback channels. This can be easily explained, since the MIP MPV depends directly on the feedback capacitance and, therefore, the channel gain (with 2.27 ratio between the channels), while the noise introduced by the readout electronics comprises a number of components in a signal processing

chain. The ratio between the measured noise of MOS and R feedback channels is only 1.4 in average, which results in the ratio of $(2.27/1.4) = 1.62$ between the SNRs achieved for different channel types. A noticeable reduction in SNR can be found after the deconvolution process. Regardless the channel gain, the deconvolution reduces the SNR by factor 1.35, due to the noise RMS increase. However, even the lowest SNR values achieved for the R feedback are still sufficient for further data processing.

2.3.3 Position reconstruction

The particles impact point on the first LumiCal plane was calculated from the tracks reconstructed in the telescope, as it was described in Section 2.2.1. To analyze the LumiCal position reconstruction ability, the projected tracks have to be combined with the LumiCal data. Since only the position reconstruction is of interest in this section, the events (tracks and LumiCal hit positions) related to muons or high energy electrons which do not initiate the shower before the first LumiCal sensor, may be investigated. These particles, acting as MIPs, deposit their energy into a single LumiCal sensor pad in the majority of cases. Therefore, the events with signal above 3 times noise RMS in only one LumiCal pad were selected. The data from the first LumiCal sensor S0, regardless the configuration, combined with the telescope tracks are presented in Figure 2.35.

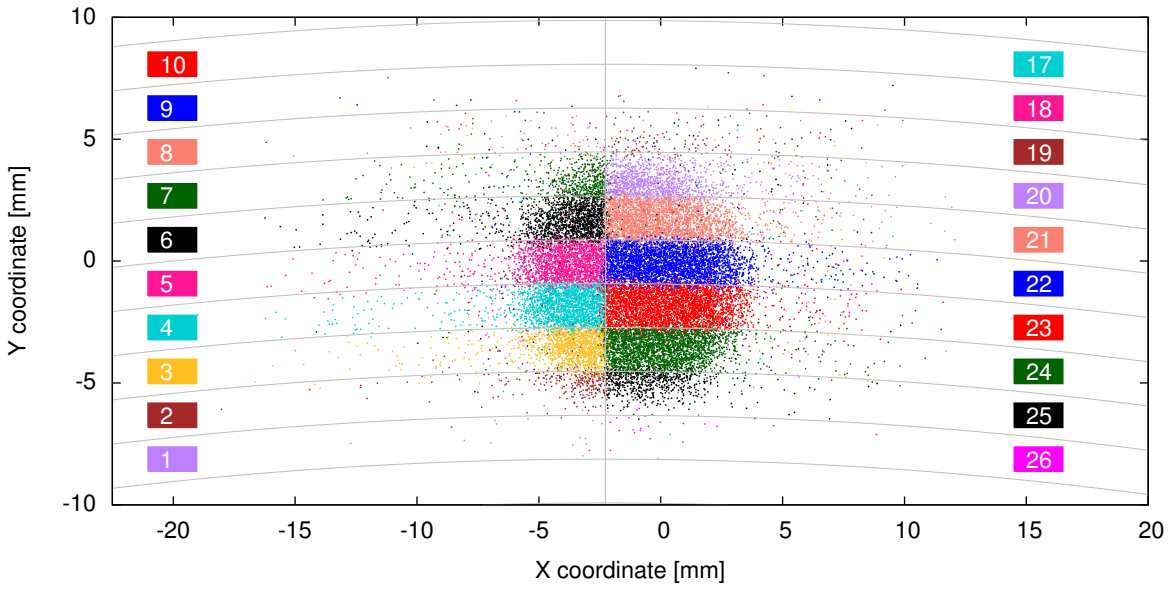


Figure 2.35: Reconstructed position of beam particle impact point combined with signals registered in LumiCal sensor pads.

The structure of the LumiCal sensor (outlined in gray) is very well reflected by the reconstructed points. Moreover, the beam profile determined by the hole scintillator can be clearly seen. One should note that only a part of LumiCal sensor is presented in Figure 2.35. The omitted channels (C0, C11-C16, C27-C31) were located sufficiently far away from the beam center and did not register significant number of hits.

2.3.4 Shower development

The shower developed in the LumiCal prototype can be analyzed under a number of aspects. The precise luminosity measurement, based on the Bhabha events, requires the shower energy and the polar angle θ reconstruction, as it was discussed in Section 1.3.1. In this dissertation the analysis of the shower energy depositions is presented.

Energy spectra

Neglecting the spatial dependency, the shower energy sampled by a particular sensor can be represented, for a given event, as a sum of charges deposited in all detector pads (in order to measure the shower polar angle, the signals registered by the sensor pads have to be clustered, enabling the shower center position reconstruction). An exemplary spectrum of energy deposited in the whole instrumented area of board IDN64 (sensor S1) in the second configuration (corresponding to five radiation lengths X_0 in the tungsten absorber) is shown in Figure 2.36.

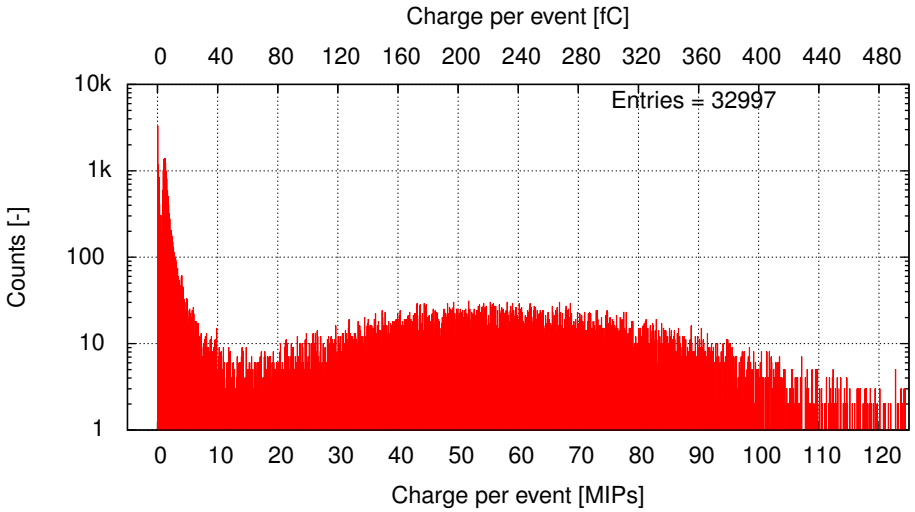


Figure 2.36: Exemplary spectrum of energy deposited in the whole instrumented area of board IDN64 (sensor S1) in the second configuration (corresponding to five radiation lengths X_0 in the tungsten absorber).

Apart from the depositions related to shower development, the two dominant components, related to the noise and muons depositions, can be found in the presented spectrum. Since the muons are not correlated with shower development, their depositions (as well as the noise contribution) should be excluded from the spectra. An efficient criterion rejecting the muon events can be found since the shower development was sampled at different radiation lengths simultaneously. In such case, the energy deposited by the muon traversing the LumiCal volume should be similar in all sensor layers, remaining in average close to a single MIP, contrary to the depositions related to shower development. Therefore, by requiring the energy deposited per single layer, averaged over all sensors, below 3 MIPs, with individual sensor depositions also below 3 MIPs in at least three of the four layers (two of three in third configuration), the muon events can be selected and excluded from the further processing. An exemplary spectrum corresponding to the one presented in Figure 2.36, after the muon cut, is shown in Figure 2.37. As can be seen from the presented spectra, the proposed muon cut suppresses sufficiently both the noise and the muon signal, without affecting the low depositions related to the shower development.

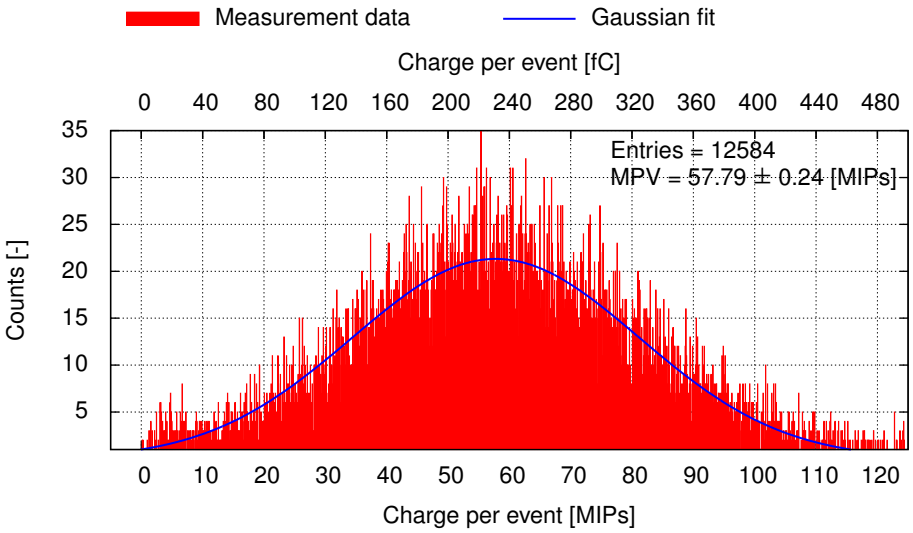


Figure 2.37: Exemplary spectrum of energy deposited in the whole instrumented area of board IDN64 (sensor S1) in the second configuration (corresponding to five radiation lengths X_0 in the tungsten absorber) after the muons cut.

Shower development

To present the overall shower development, the energy deposition in a particular layer (corresponding to certain number of radiation lengths X_0) can be characterized by two quantities – the MPV, represented by the Gaussian distribution center value, or the mean deposition, achieved as an average over all registered events. The fitted Gaussian distribution for the exemplary spectrum is shown in Figure 2.37. The detailed plots for all boards in all configurations are presented in Appendix A. The calculated MPVs and mean depositions for all boards in all configurations are summarized in Table 2.9. The mean depositions in function of number of radiation lengths X_0 in absorber are presented in Figure 2.38. The measurement uncertainty were estimated to 5 % of the values based on the standard deviation of the averaged board gain. The depositions obtained from different sensors located at the same radiation length in different configurations (see Table 2.1 for details) are very similar, well within the estimated uncertainties.

Configuration	Board	X_0	MPV [MIPs]	Mean deposition [MIPs]
1	IDN63	1	3.38	8.31
	IDN64	3	35.78	39.43
	IDN67	5	58.12	60.26
	IDN76	7	55.87	58.08
2	IDN63	3	34.08	38.01
	IDN64	5	57.80	59.01
	IDN67	7	56.54	58.65
	IDN76	9	37.59	40.47
3	IDN63	4	49.28	52.42
	IDN64	6	58.95	60.91
	IDN67	8	46.18	49.16

Table 2.9: MPVs and mean depositions of the shower development.

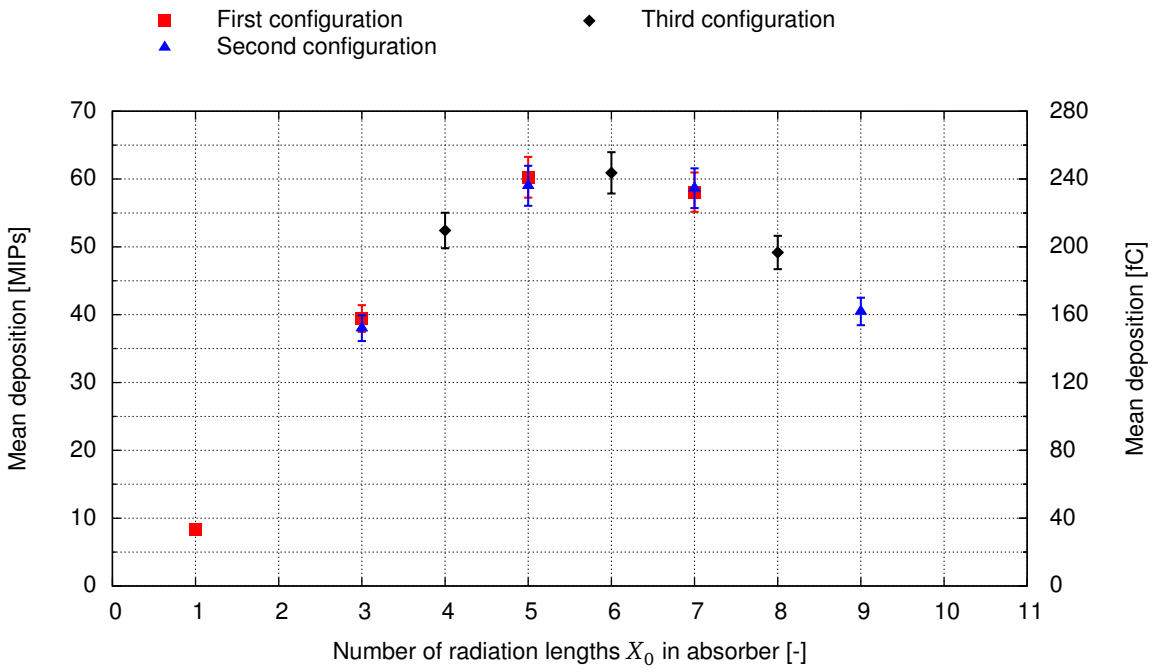


Figure 2.38: Mean energy deposited in the instrumented area as a function of the tungsten absorber thickness expressed in radiation lengths.

In order to verify the experimental results the MC simulations of a shower development in the LumiCal sensor, with geometry given by the testbeam setup, were performed for initial electrons energy of 5 GeV, using DD4Hep and Geant4 simulation environments [77, 78]. The comparison of the mean depositions achieved from experimental data and the MC simulations is shown in Figure 2.39. Since the experimental data, as well as the MC results, achieved in different configurations for the same X_0 are almost the same, the average values are presented in Figure 2.39 for clarity.

In general, the experimental results remain in good agreement with the MC results. The measured shower maximum is located around the 6th radiation length X_0, in agreement with the simulations. The discrepancy between the experimental data and the ideal MC simulations (red dots in Figure 2.39) on the shower tail results from ideal setup assumptions taken in the ideal MC simulations. As can be seen from Figure 2.35, the center of the beam was located close to the lower edge of the instrumented sensor area. Since the expected Molière radius for the LumiCal is around 12 mm, a part of the shower may be deposited in the unreadable sensor area. Taking into account a rather flat beam distribution (Figure 2.22), a significant number of showers was initiated by the electrons incoming closer to the instrumented area edge than to the beam center. This effect is illustrated in Figure 2.40, where an effective Molière radius of a shower initiated by the electron incoming close to the lower boundary of the beam is presented together with the readable sensor area. Since the shower develops longitudinally as a cone, it deposits almost all the energy within the instrumented region at the initial development stages. Approaching the shower maximum, a noticeable fraction of the energy begins to be deposited outside the readable area, reducing the measured mean deposition per layer with increasing radiation length.

In order to confirm this assumption, the beam spread as well as the readout limitations need to be implemented into the MC simulations. The first, preliminary results of MC taking into account these issues are presented in Figure 2.39 as MC1 (green triangles, achieved using DD4Hep environment [77]) and MC2 (blue diamonds, achieved from Geant4 environment [78]). Since the precise

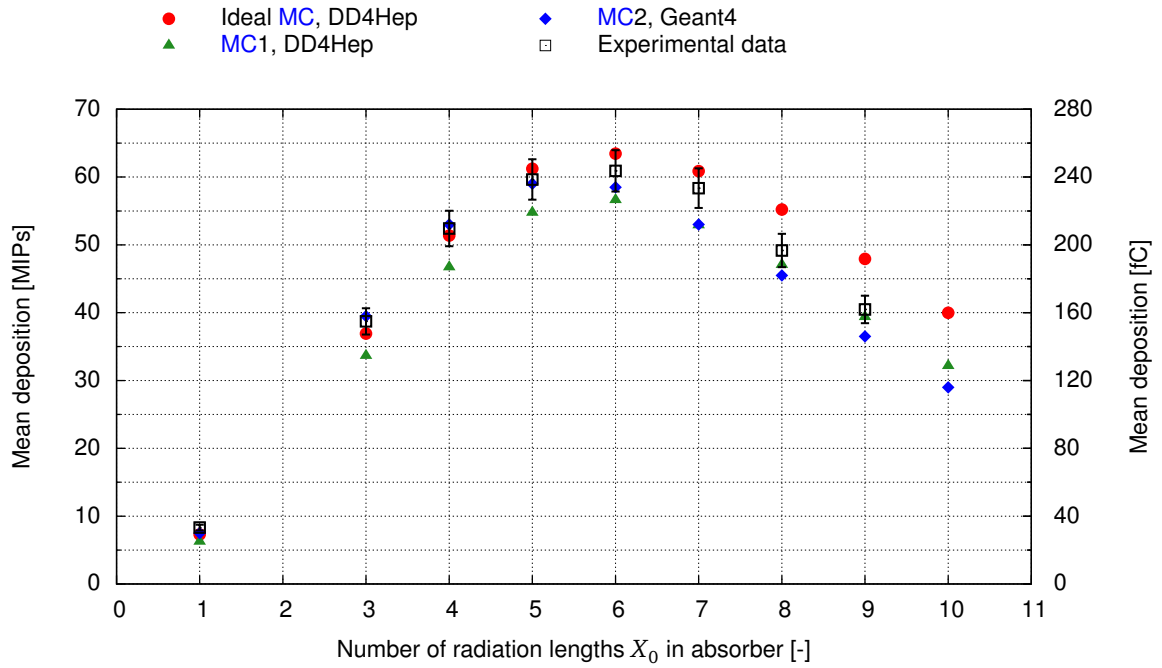


Figure 2.39: Comparison of experimental and MC simulations results of mean energy deposited in the instrumented area as a function of the tungsten absorber thickness expressed in radiation lengths.

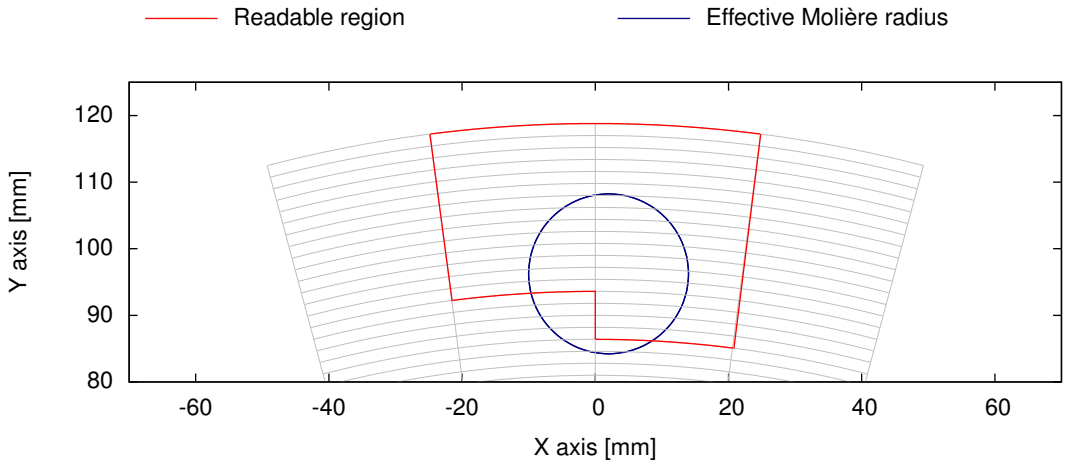
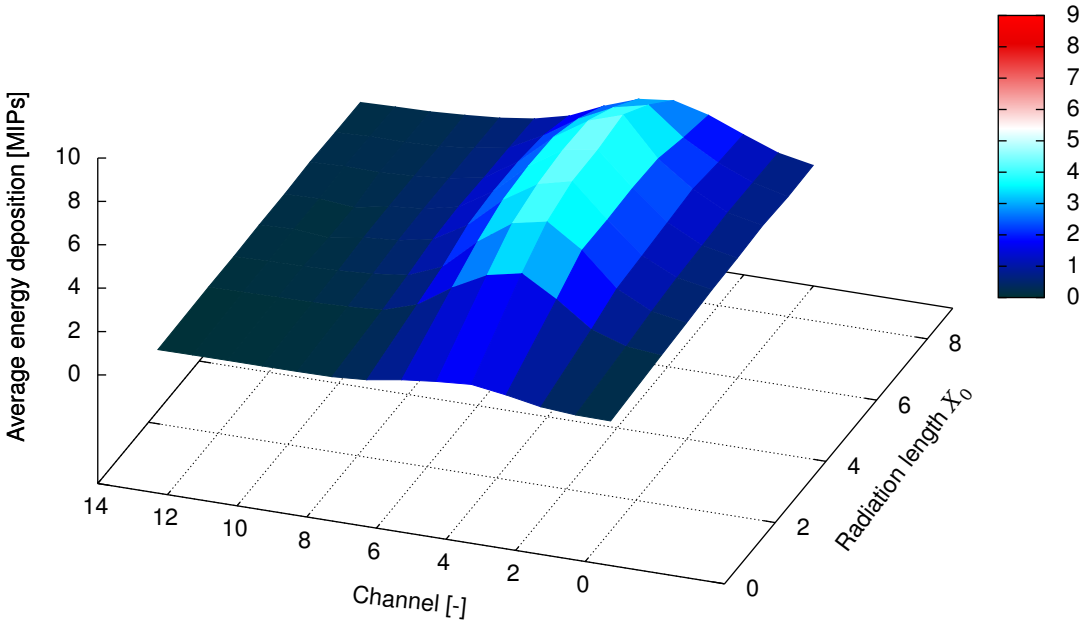


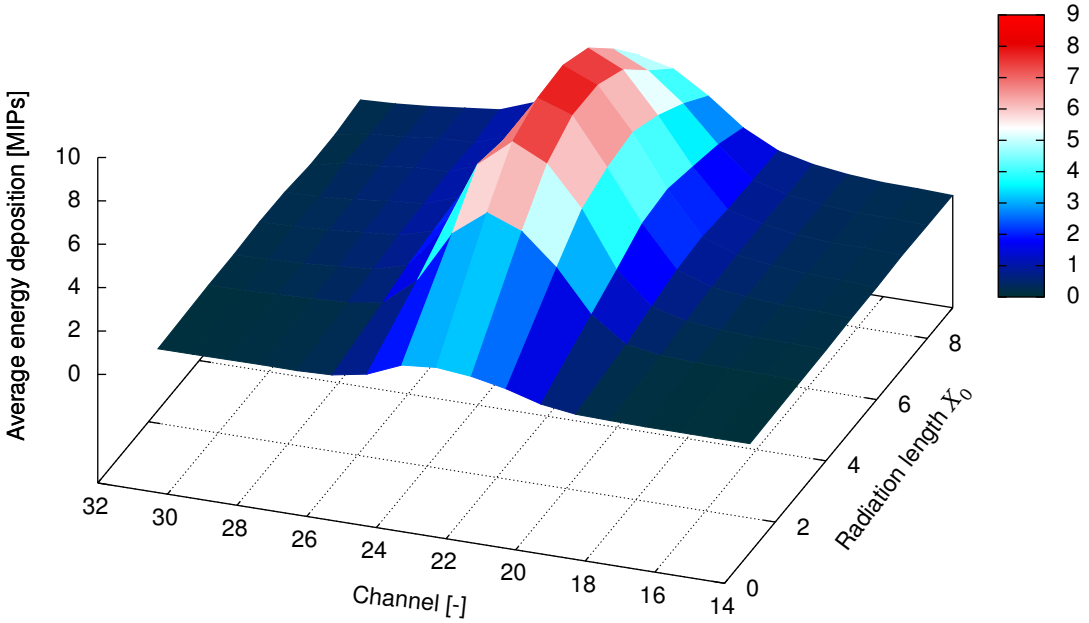
Figure 2.40: Readable region of the sensor at single layer LumiCal readout prototype.

implementation of the total instrumentation geometry into the MC simulation setup is non-trivial, some discrepancies between the newest MC results and the experimental data may be still found. However, the experimental results obtained with the procedure discussed in this dissertation remains within boundaries determined by the ideal and the newest MC simulations.

In order to illustrate the spatial shower development, the three-dimensional profiles of the deposited charge were calculated. An average charge deposition in each sensor pad was calculated as a sum of depositions from all events in the given configuration, divided by the number of events. The profiles are presented in Figure 2.41, for the left tail (channels 0-14, Figure 2.41a) and the right tail (channels 15-31, Figure 2.41b) of the LumiCal sensor separately.



a) Left tail



b) Right tail

Figure 2.41: Averaged 3D profile of the electromagnetic showers.

Although the polar angle reconstruction capability was not discussed, since the related analysis were still ongoing at the time, the presented experimental results indicate that the obtained shape, at least qualitatively seems very reasonable. To complete the results presented and discussed in this dissertation, the MC comprising a more precise geometrical setup description, as well as polar angle reconstruction, are foreseen. However, the basic aims of the presented testbeam are already fulfilled by the analysis presented in this dissertation.

Chapter 3

Development of new readout electronics

The continuous development of HEP experiments and their detectors constantly rises the requirements for the readout electronics. A growing segmentation of radiation sensors, induced for example by the particle flow reconstruction algorithm foreseen in future linear collider detector system (see Section 1.2), results in increasing number of readout channels in the same area, and so increases the readout density. Simultaneously, a higher luminosity of future experiments (linear collider or LHC) increases both the detector occupancy (due to a higher event rate) and the total radiation dose deposited in the readout electronics. The first effect, related to a larger amount of data processed by readout in each event, requires a faster and more effective data processing. The second one rises the demands on radiation hardness of readout ASICs, in order to ensure a proper operation at higher radiation levels for the entire experiment lifetime.

Regardless of the continuous development of readout architectures, the main limitations of the design performance are imposed by the chosen CMOS technology. The technology-dependent parameters, such like intrinsic gain of transistors, digital cells (inverters, logic gates, flip-flops) propagation times, and power consumption, provide the constraints on the overall design performance, which cannot be exceeded by implementation of modern, even more efficient architectures. Also the radiation hardness depends mainly on the chosen technology, primarily on the gate oxide thickness, and can be improved only in a limited way by a dedicated design techniques, like enclosed gate transistors.

New generations of deep sub-micron CMOS technologies open up new opportunities for the development of readout electronics. The key technology parameter, a minimum length of the MOS transistor channel, decreases continuously with the technology development, entailing the improvement of the overall speed and power consumption. The gate oxide thickness, decreasing simultaneously with the channel length, results in higher radiation hardness of the modern, deep sub-micron CMOS technologies, what makes them an ideal candidate for the future readout electronics designs.

In order to improve the performance of the existing LumiCal readout electronics, a dedicated ASICs, both the front-end and the ADC one, were developed in modern deep sub-micron CMOS technologies. The first generation of these ASICs, utilized in the existing readout module (see Section 1.4.2), were developed in cheaper, moderately sub-micron AMS 350 nm technology. The newer deep sub-micron technologies, with improved key parameters, may provide a new opportunities for the LumiCal readout. A two modern CMOS 130 nm technologies, called hereinafter the CMOS 130 nm process A and the CMOS 130 nm process B, were investigated and compared with the AMS 350 nm. The promising results of these studies, discussed in the following section, enabled the development of new readout ASIC prototypes, which are the main topic of this chapter.

3.1 Technology comparison

3.1.1 Analogue parameters

As it was discussed, modern technologies offer higher speed and lower power, which are very important for the analogue circuits performance. But, apart from these obvious advantages, a key issue in analogue circuits functionality is their ability for signal amplification. To compare the analogue behavior of the three technologies (AMS 350 nm, CMOS 130 nm process A and CMOS 130 nm process B) one of the most important parameters, the intrinsic gain, was chosen.

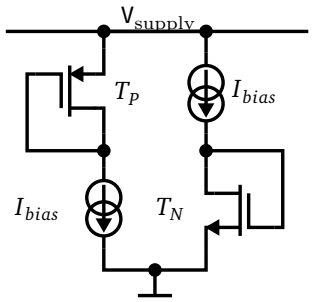


Figure 3.1: Schematic for the intrinsic gain simulations.

In order to determine the intrinsic gain, the schematic presented in Figure 3.1 was used (left for PMOS, right for NMOS). The intrinsic gain is therefore defined as a product of the transistor transconductance g_m and the drain to source resistance r_{ds}. The simulations were performed for various W/L ratios with two different channel lengths - the minimum possible length in a given technology L_{min} and an arbitrary chosen L_{arb} set to be around 2.5 times larger than L_{min}. For plots clarity, only two W/L ratios, 4 and 40, are presented. The minimum and arbitrary channel lengths with corresponding channel width W at given W/L ratio are presented in Table 3.1.

	AMS 350 nm	CMOS 130 nm process A	CMOS 130 nm process B
L_{min}	350 nm	120 nm	130 nm
W/L = 4	1.4 μm	480 nm	520 nm
W/L = 40	14.0 μm	4.8 μm	5.2 μm
L_{arb}	850 nm	300 nm	300 nm
W/L = 4	3.4 μm	1.2 μm	1.2 μm
W/L = 40	34.0 μm	12.0 μm	12.0 μm

Table 3.1: Channel width for minimum L_{min} and arbitrary L_{arb} channel lengths.

The comparison of the intrinsic gain in all three technologies for minimum channel length L_{min} is presented in Figures 3.2 and 3.3 for the NMOS and PMOS transistor, respectively. The difference between the AMS 350 nm and the modern CMOS 130 nm process A or CMOS 130 nm process B technologies can be clearly seen. The intrinsic gain of NMOS transistor in the AMS 350 nm reaches the value of around 90 V/V for drain current i_d below 1 μA, while in the two modern technologies it is reduced by factor 4.5 in the CMOS 130 nm process B technology and by factor 7.5 in the CMOS 130 nm process A. Similar behavior can be found for PMOS transistor, where the intrinsic gain in AMS 350 nm for low drain current is of around 34 V/V, while in the modern technologies it is 1.3 times smaller in CMOS 130 nm process B and 2.4 times in CMOS 130 nm process A. Increasing the channel length to the arbitrary values L_{arb}, presented in Figures 3.4 and 3.5 for the NMOS and

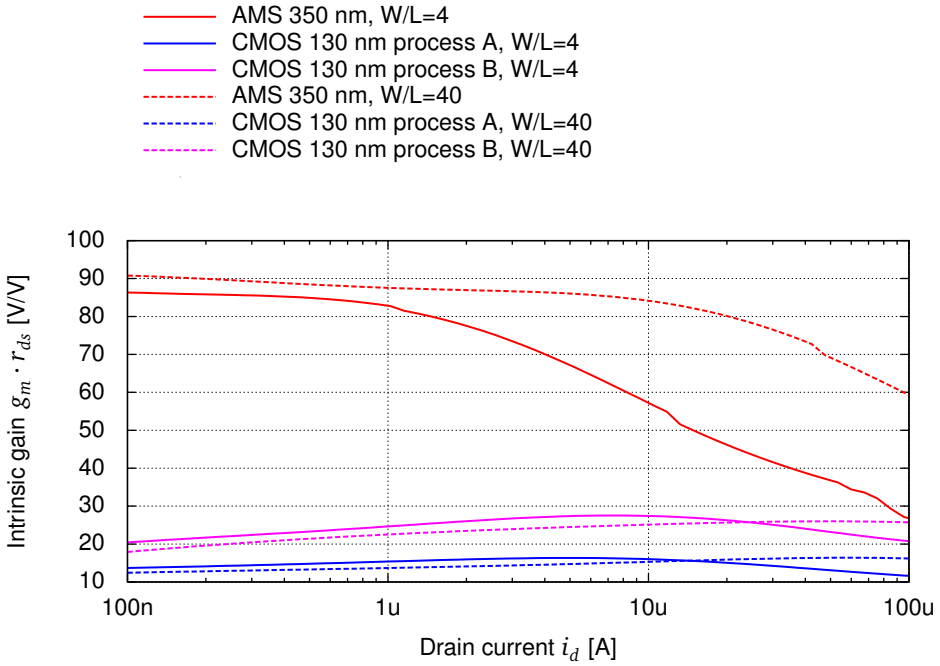


Figure 3.2: Comparison of the intrinsic gain $g_m \cdot r_{ds}$ of the NMOS transistor for minimum channel length L_{min}.

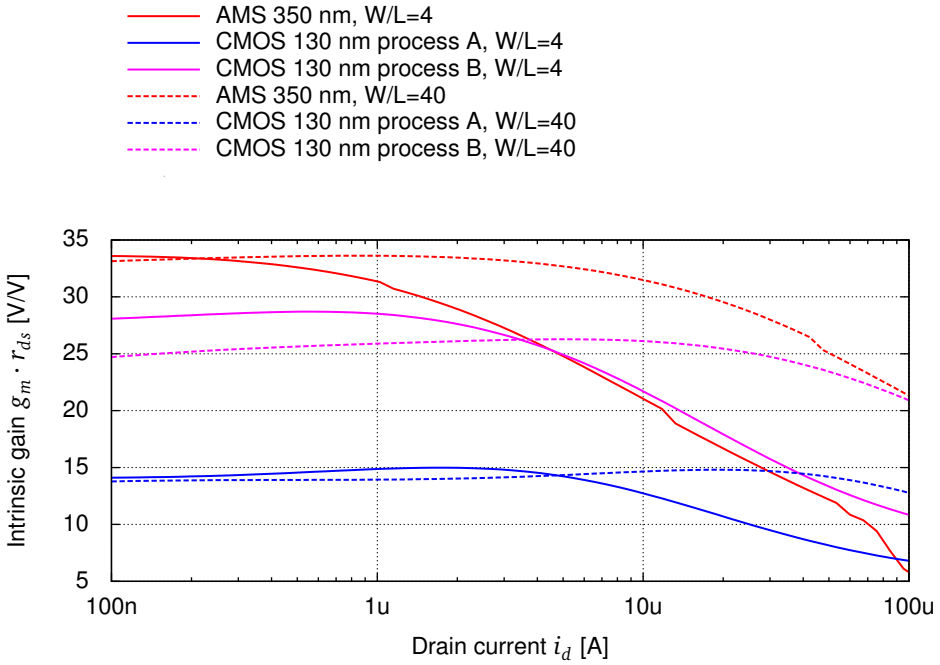


Figure 3.3: Comparison of the intrinsic gain $g_m \cdot r_{ds}$ of the PMOS transistor for minimum channel length L_{min}.

PMOS transistor respectively, highly increases the differences between the AMS 350 nm and the modern technologies. Since the intrinsic gain is significantly lower in the modern technologies, a more complex analogue circuitry need to be designed in order to make up for this disadvantage.

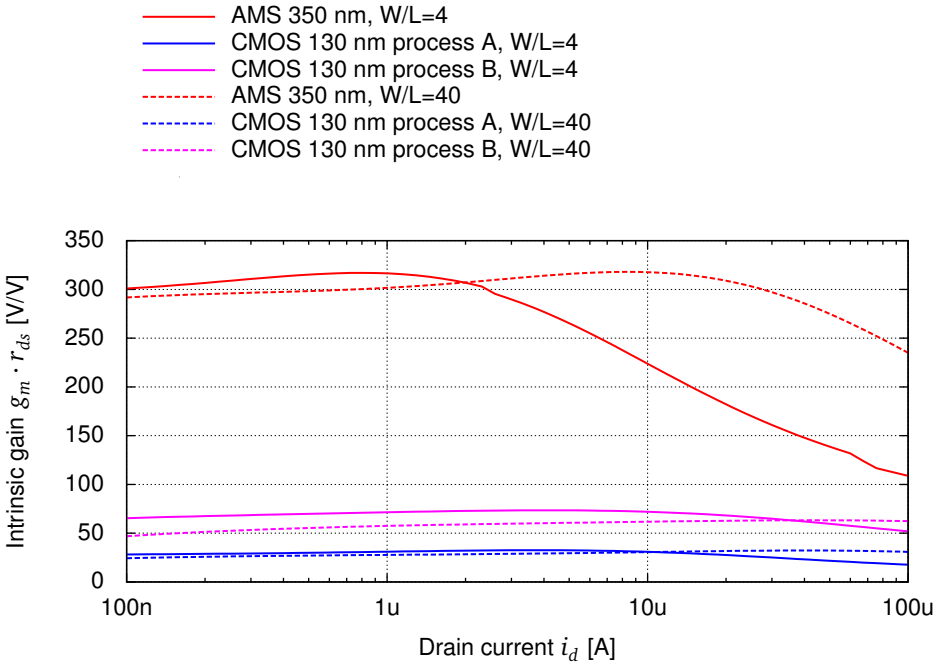


Figure 3.4: Comparison of the intrinsic gain $g_m \cdot r_{ds}$ of the NMOS transistor for arbitrary chosen channel length L_{arb}.

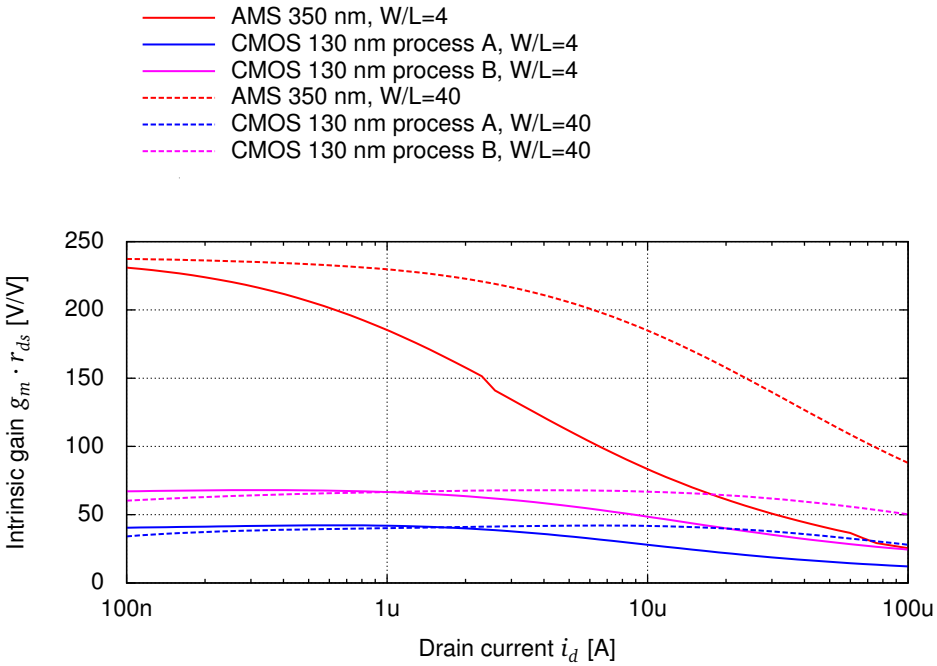


Figure 3.5: Comparison of the intrinsic gain $g_m \cdot r_{ds}$ of the PMOS transistor for arbitrary chosen channel length L_{arb}.

3.1.2 Digital circuits

To characterize digital features of the technologies, propagation delay t_{del}, current I, and power consumption P per single clock period of a ten chained inverters and a static D-type flip-flop, presented in Figure 3.6, were simulated. Since the propagation delay does not fully characterize the D-type flip-flop, a maximum operating frequency f_{max} of a single-bit counter configuration was also found

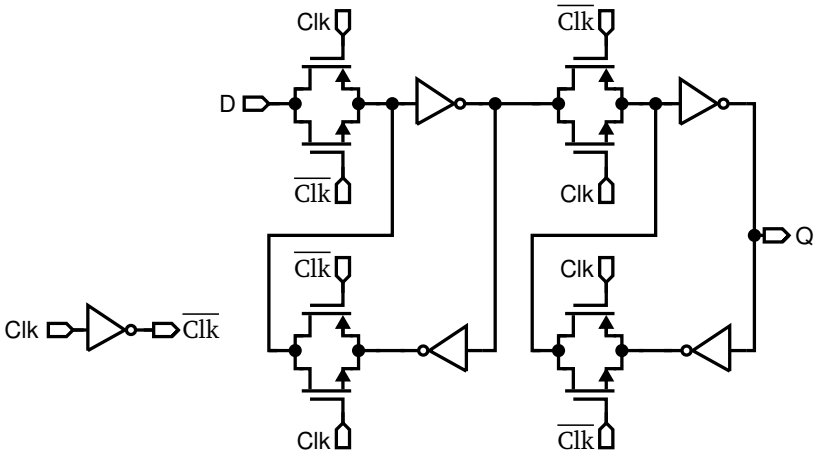


Figure 3.6: Schematic of the static D-type flip-flop.

Parameter	AMS 350 nm	CMOS 130 nm process A	CMOS 130 nm process B
Propagation delay t_{del}	617.7 ps	208.4 ps	224.3 ps
Current consumption I	1.603 μA	0.165 μA	0.228 μA
Supply voltage V_{sup}	3.3 V	1.2 V	1.2 V
Power consumption P	5.290 μW	0.198 μW	0.274 μW

Table 3.2: Propagation delay, current and power consumption of the ten chained inverters.

Parameter	AMS 350 nm	CMOS 130 nm process A	CMOS 130 nm process B
Propagation delay t_{del}	271.3 ps	87.8 ps	88.6 ps
Maximum frequency f_{max}	1.4 GHz	3.75 GHz	3.6 GHz
Current consumption I	1.155 μA	0.118 μA	0.442 μA
Supply voltage V_{sup}	3.3 V	1.2 V	1.2 V
Power consumption P	3.812 μW	0.142 μW	0.530 μW

Table 3.3: Propagation delay, maximum frequency, current and power consumption of D-type flip-flop.

in each technology. The simulations results are presented in Tables 3.2 and 3.3 for the inverters chain and D-type flip-flop respectively. It can be clearly seen that the modern technologies are both much faster and much more power efficient than the older AMS 350 nm technology. The propagation delays in the CMOS 130 nm process A and CMOS 130 nm process B are around three times smaller than in the AMS 350 nm, while the current consumption I is almost one order of magnitude smaller comparing to the AMS 350 nm technology. Furthermore, the ratio of 3 between the voltage supply V_{sup} in modern and older technologies, results in reduced power consumption by around one order of magnitude for modern technologies. It must be noted that the maximum frequency f_{max} presented in Table 3.3 can be significantly smaller in more complicated digital circuits since the setup and hold times of the flip-flops as well as the propagation delays of the logic gates have to be taken into account.

3.2 Frond-end electronics (FE)

As was shown in previous sections, moving from the AMS 350 nm to one of the modern technologies, such as CMOS 130 nm process A or CMOS 130 nm process B, significantly reduces the power con-

sumption and increases the speed of the circuits. Despite the lowered intrinsic gain, the transition to modern technologies can be considered as a significant step forward in the development of the readout of the LumiCal detector. To explore the possibilities given by the CMOS 130 nm process A, an 8-channel prototype of the front-end electronics was developed using the classical architecture, comprising a charge sensitive preamplifier followed by a Pole-Zero Cancellation (PZC) circuit, and by a CR-RC shaper. The chosen architecture, shown in Figure 3.7, is very similar to the one previously used for the prototype fabricated in the AMS 350 nm technology.

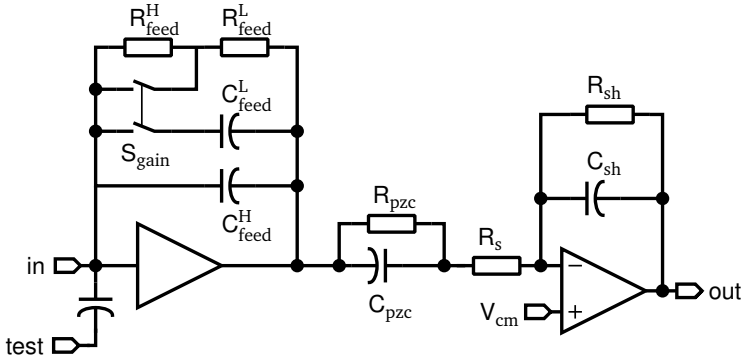


Figure 3.7: Simplified schematic of a front-end electronics for the LumiCal.

In order to simplify the deconvolution procedure, described in details in Section 2.2.2, a very simple 1^{st} order semi-gaussian shaping was implemented. The shaper peaking time T_{pk} was set to 50 ns to resolve signals from subsequent bunches within a period of about 350 ns. The pair of coupled switches S_{gain} allows to choose one of two implemented modes - the calibration mode or the physics mode. In the first one, corresponding to high preamplifier gain, the relativistic muons signals can be detected. In other words, the front-end circuit is sensitive to MIPs with low energy depositions. In the physics mode, corresponding to low preamplifier gain, a high energy depositions from electromagnetic shower can be processed, which means that the upper limit of the front-end dynamic range should be at least 6 pC. A wide range of capacitive load, from 5 pF up to 35 pF, connected to a single front-end channel, is expected from the proposed sensor geometry. Since in the ILC experiment 200 ms pause is foreseen between bunch trains, the power pulsing feature, i.e. the capability of reducing the power consumption to almost zero between the bunch trains, is strongly requested. The ratio between the bunch length (1 ms) and the gap between them (200 ms) allows to reduce the average power consumption by about two orders of magnitude. Therefore, the requirements on power dissipation for the readout electronics may be fulfilled even with a peak power of the front-end electronics of a few mW.

The proposed CR-RC shaping with two real poles is obtained using a simple R_{pzc}-C_{pzc} network of the PZC and a two pole shaper circuit. Assuming an ideal amplifier, the preamplifier transfer function can be written as follow:

$$\frac{U_{out}(s)}{I_{in}(s)} = \frac{1}{C_{feed}} \times \frac{1}{s + \frac{1}{R_{feed} C_{feed}}}, \tag{3.1}$$

where R_{feed} and C_{feed} can be, by changing the coupled switches S_{gain}, set to:

$$R_{feed} = \begin{cases} R^H_{feed} + R^L_{feed} & \text{in the high gain mode,} \\ R^L_{feed} & \text{in the low gain mode;} \end{cases}$$

$$C_{\text{feed}} = \begin{cases} C^{\text{H}}_{\text{feed}} & \text{in the high gain mode,} \\ C^{\text{H}}_{\text{feed}} + C^{\text{L}}_{\text{feed}} & \text{in the low gain mode.} \end{cases} \tag{3.2}$$

The transfer function of the shaper, including the PZC network, can be written as:

$$\frac{U_{\text{out}}(s)}{U_{\text{in}}(s)} = \frac{1}{R_s C_{\text{sh}}} \times \frac{s + \frac{1}{R_{\text{pzc}} C_{\text{pzc}}}}{s + \frac{R_s + R_{\text{pzc}}}{R_s R_{\text{pzc}} C_{\text{pzc}}}} \times \frac{1}{s + \frac{1}{R_{\text{sh}} C_{\text{sh}}}} \,. \tag{3.3}$$

To achieve the correct operation of PZC circuit, the preamplifier feedback time constant $\tau_{\text{feed}} = R_{\text{feed}} C_{\text{feed}}$ should be equal to $\tau_{\text{pzc}} = R_{\text{pzc}} C_{\text{pzc}}$, i.e. the pole from the preamplifier transfer function 3.1 should be canceled by the zero from the shaper transfer function 3.3. To simplify the PZC circuit, τ_{feed} is the same in both gain modes, i.e.:

$$\tau_{\text{feed}} = \left(R^{\text{H}}_{\text{feed}} + R^{\text{L}}_{\text{feed}}\right) C^{\text{H}}_{\text{feed}} = R^{\text{L}}_{\text{feed}} \left(C^{\text{H}}_{\text{feed}} + C^{\text{L}}_{\text{feed}}\right) = \tau_{\text{pzc}} \,. \tag{3.4}$$

The feedback capacitance C_{feed} changes from 0.5 pF in the calibration mode to 20 pF in the physics mode, and the time constant τ_{feed} is set to around 400 ns. The CR-RC shaping with peaking time $T_{pk} = 50$ ns is obtained by setting two poles of the shaper transfer function 3.3 equal:

$$\tau_{\text{sh}} = R_{\text{sh}} C_{\text{sh}} = \frac{R_s R_{\text{pzc}}}{R_s + R_{\text{pzc}}} C_{\text{pzc}} \,. \tag{3.5}$$

Keeping the time constants as defined in 3.4 and 3.5 the transfer function of the full circuit presented in Figure 3.7 can be written as the product of preamplifier 3.1 and shaper 3.3 transfer functions:

$$\frac{U_{\text{out}}(s)}{I_{\text{in}}(s)} = \frac{1}{R_s C_{\text{feed}} C_{\text{sh}}} \times \frac{1}{\left(s + \frac{1}{\tau_{\text{sh}}}\right)^2} \,. \tag{3.6}$$

3.2.1 Amplifiers design

Preamplifier

A simplified preamplifier schematic diagram is presented in Figure 3.8. The input stage of the preamplifier is an NMOS transistor $\mathtt{M}_1$ with cascode transistor $\mathtt{M}_2$. The current source loads are designed as a folded cascodes comprising $\mathtt{M}_3$ and $\mathtt{M}_4$ transistors. The high value of current flowing through the $\mathtt{M}_1$ transistor is needed since a high transconductance g_{m1} is highly required to obtain a high gain and a low preamplifier noise. On the other hand, to achieve a high load resistance r_{ds3}, the current in the current source load $\mathtt{M}_3$ should be rather low. These conditions can be achieved by splitting the high current from $\mathtt{M}_1$ transistor into two branches i_{load} and i_{branch}. Lower value of i_{load} results in higher r_{ds3} resistance while the transconductance g_{m1} of $\mathtt{M}_1$ transistor is driven by the sum of the two current branches $i_{load} + i_{branch}$. The low value of i_{load} results also in reduced load capability of $\mathtt{Out}_{\text{cas}}$ output of the cascode amplifier. Since the preamplifier feedback contains the resistance $\mathtt{R}_{\text{feed}}$, which is rather small in the physics mode, the source follower $\mathtt{M}_5$ was added to buffer the cascode amplifier output. Since the intrinsic gain in the CMOS 130 nm process A is very low, as was shown in Section 3.1.1, all cascodes $\mathtt{M}_2$, $\mathtt{M}_3$ and $\mathtt{M}_4$ use additional boosting amplifiers ($\mathtt{M}_{12}$, $\mathtt{M}_{13}$ and $\mathtt{M}_{14}$, respectively) to increase the overall gain.

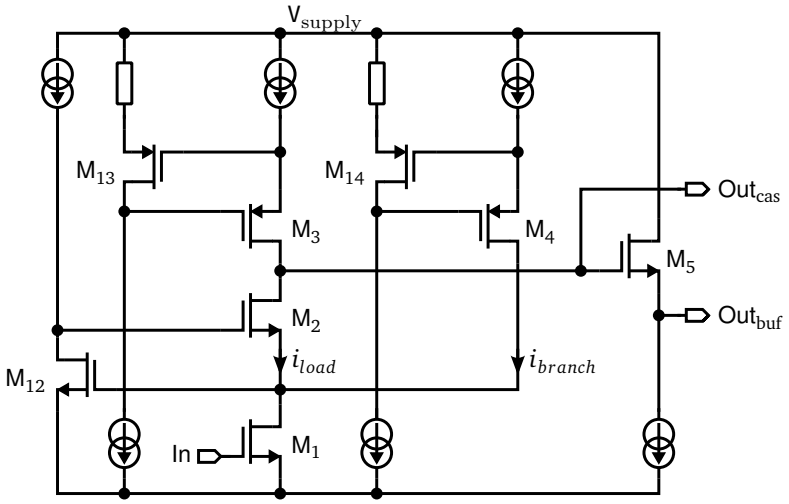


Figure 3.8: Simplified schematic diagram of the preamplifier.

Shaper

The shaper amplifier is designed using the Recycled Folded Cascode (RFC) amplifier configuration [79] for better power-bandwidth efficiency. A simplified schematic diagram of the shaper amplifier is presented in Figure 3.9. In comparison to a conventional Folded Cascode (FC) amplifier, the RFC configuration allows to increase both the low frequency gain and the bandwidth of the amplifier. If the channel length of transistor M_9, denoted as W_9, is K times larger than W_7 and, analogously, W_{10} is K times larger than W_8, the current I_b will be split into two branches, one comprising M_3 and M_9 and the second comprising M_1, M_6, and M_8, with factor K between them. The current flowing through the M_{12}, M_{14} and M_{16} is a function of current gain K and is equal to $I_{out} = (K-1)I_b/2$. Therefore, the amplifier transconductance G_m can be written as $g_{m1}(K+1)$. Assuming that in conventional FC architecture the transconductance of input transistor will be two times higher than g_{m1}, the transconductance G_m of the RFC architecture with current gain $K = 3$ is two times higher than for the FC at the same power (the G_m of the RFC is equal $g_{m1}(3+1)$, while the FC one $2g_{m1}$). This means that the Gain–Bandwidth Product (GBW) of RFC is also two times higher than for the FC. Without considering the output impedance R_{out}, the low frequency gain is therefore enhanced by 6 dB in the

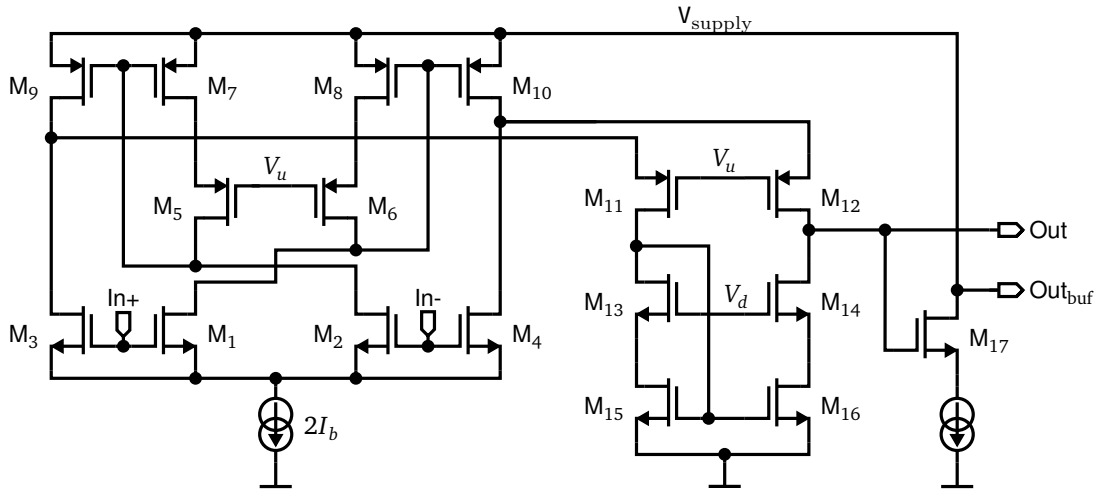


Figure 3.9: Simplified schematic diagram of the shaper amplifier.

RFC. However, the R_{out} is also improved in the RFC comparing to the FC. In both configurations the R_{out} can be written as:

$$R_{out} \cong g_{m12} r_{ds12} (r_{ds4} || r_{ds10}) || g_{m14} r_{ds14} r_{ds16} \,, \tag{3.7}$$

but since the current in the branch comprising M_4 and M_{10} is smaller than similar current in the FC architecture, the r_{ds4} and r_{ds10} are increased in the RFC and the overall low frequency gain can be enhanced by 8 – 10 dB comparing to the FC.

Simulation results

To prove the stability of the designed front-end, the frequency response of the preamplifier, shown in Figure 3.10 and the shaper, shown in Figure 3.11, were simulated. Since the gain mode does not affect the shaper frequency response, only one Bode plot is shown for the shaper, unlike the preamplifier, where a difference between the gain modes can be observed. The most important parameters obtained from the frequency simulations are presented in Table 3.4. The phase and gain margins of the preamplifier remain within the safe limits in both gain modes, exceeding the values

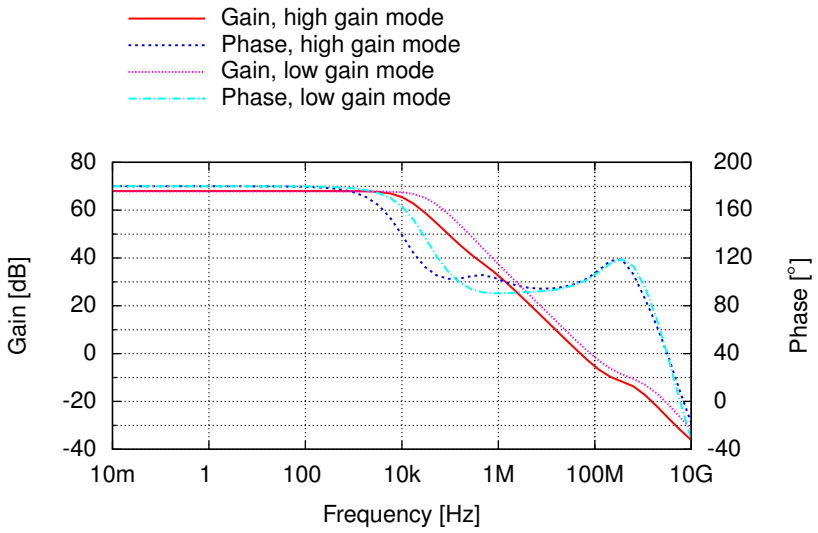


Figure 3.10: Bode plot of the preamplifier in both gain modes.

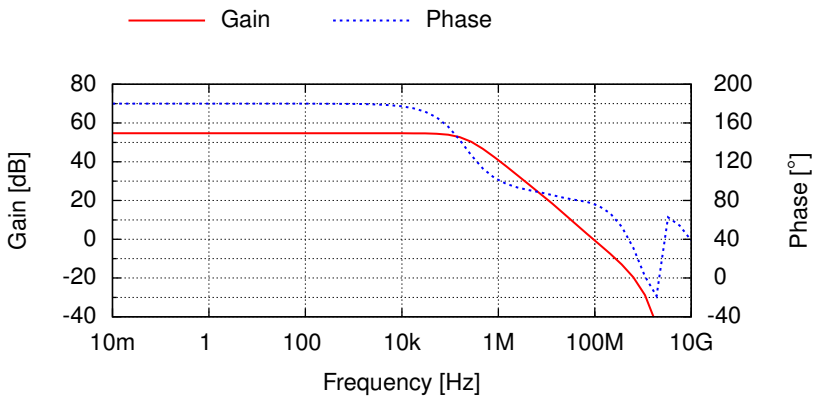


Figure 3.11: Bode plot of the shaper circuit.

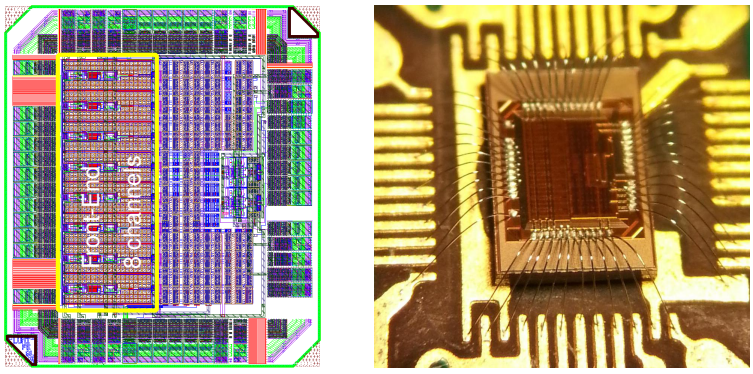
	Preamplifier		Shaper
Parameter	High gain	Low gain	Both gains
Low frequency gain [dB]	68.0	67.9	54.7
GBW [MHz]	54.5	87.4	100.5
Phase margin [°]	100.0	103.4	76.7
Phase minimum [°]	94.3	90.5	–
Gain margin [dB]	-33.2	-26.6	-30.1

Table 3.4: Amplifiers stability parameters.

of 100°and -25 dB respectively. Since the phase of the preamplifier is not a monotonic function in the range where the gain is higher than 0 dB, the phase minimum in this range was also calculated and it is also safe with the value of 90°. The gain margin of the shaper amplifier is very similar to the preamplifier and the phase margin of around 76° is still acceptable. It is not shown here, but to verify the design, the stability of the internal boosting amplifiers (M_{12}, M_{13} and M_{14}, shown in Figure 3.9) was also simulated.

3.2.2 Front-end electronics measurements

The prototype ASIC, comprising 8 front-end channels was designed and fabricated in the CMOS 130 nm process A technology. The layout of the ASIC is shown in Figure 3.12a and the fabricated prototype, glued and bonded on the PCB, on Figure 3.12b. The area occupied by the whole ASIC is 720 μm × 1500 μm, while the area of a single channel is 46 μm × 425 μm.

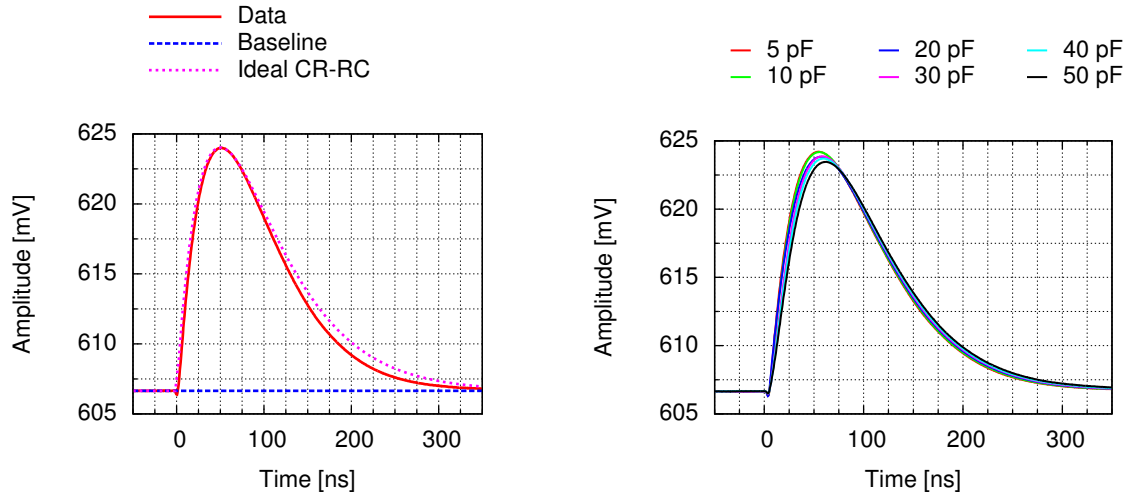


a) Layout b) Photograph

Figure 3.12: Front-end prototype ASIC.

In order to verify the front-end operation a dedicated measurement setup was used. As a source of test pulses an arbitrary waveform generator, Agilent 81150A, was used. All biasing currents were supplied by Agilent Semiconductor Analyzer B1500A. The measurements of amplitude were performed with Agilent MSO7104B scope. All instruments were controlled by a PC via General Purpose Interface Bus (GPIB) and Local Area Network (LAN) interfaces. All discussed measurements were done injecting signal through an internal test input capacitance and with an external input capacitance simulating the sensor.

In Figure 3.13a an example pulse response in the calibration mode is shown for 10 pF input capacitance and 4 fC input charge. The peaking time and pulse shape are in a very good agreement

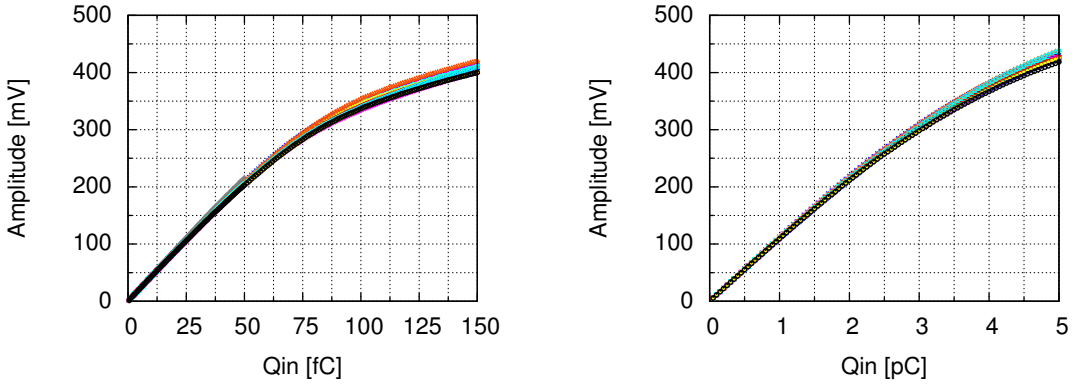


a) Example pulse shape at 10 pF input capacitance

b) Pulse shapes for different input capacitances

Figure 3.13: Pulse response of the front-end.

with the simulations. The difference between the ideal CR-RC shape, also shown in Figure 3.13a, and the obtained pulse results mainly from the non-ideality of shaper amplifier, what will be discussed later in Section 3.2.3. The pulses measured for the input capacitances in the range of 5 – 50 pF, shown in Figure 3.13b, show that the charge sensitivity of the front-end is good enough. The relative difference of charge gain for the highest and the lowest input capacitance is lower than 6 %. The peaking time depends linearly on the input capacitance, and changes from 50 ns to 57 ns for the lowest and highest capacitances respectively.



a) Calibration mode (high gain)

b) Physics mode (low gain)

Figure 3.14: Front-end gain and linearity measurements.

The measurement of the front-end linearity was done for two prototype ASICs in both gain modes, and the results are presented in Figure 3.14. To simplify the plots, the channels from the first measured prototype are hereinafter labeled as channels 0 – 7 and the channels from the second one as 8 – 15. The average gain in the calibration mode is 4.2 mV/fC and in the physics mode 105 mV/pC. The variations of the gain between channels are below 10 % and are, together with the obtained gain values and dynamic ranges, in very good agreement with the simulations.

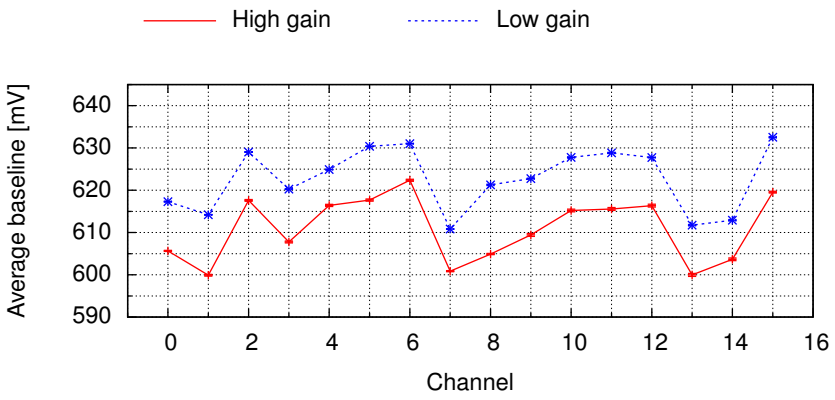
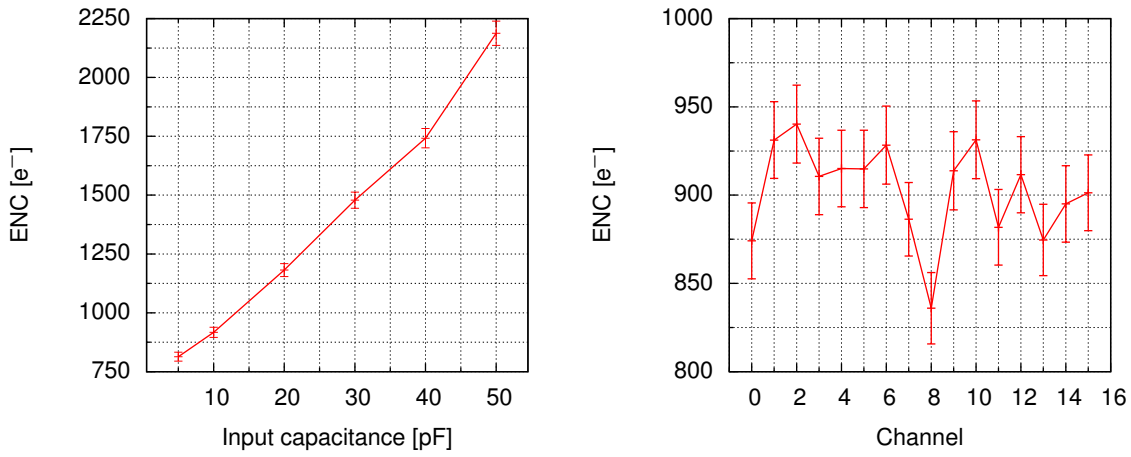


Figure 3.15: Baseline spread between the channels.

The baseline spread, shown in Figure 3.15, is moderate with the maximum value of 25 mV. It was verified by the MC simulations that this spread is caused by the offset spread of the shaper amplifier. It have to be noticed that this effect may require an additional baseline trim DAC added in the signal path. However, since the baseline spread does not change in time, it can be easily removed by the pedestal subtraction procedure.



a) ENC versus input capacitance

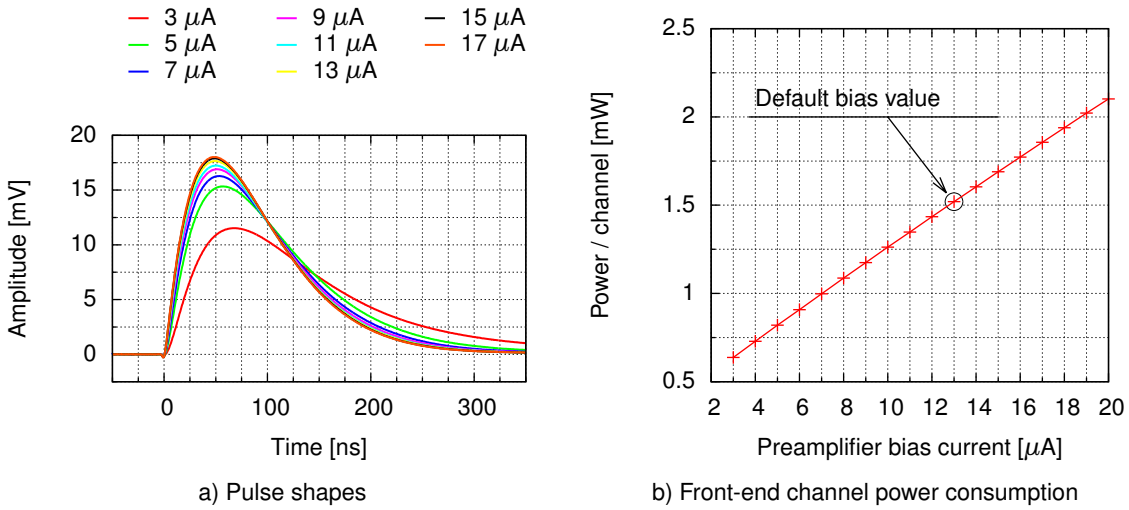
b) ENC spread at 10 pF input capacitance

Figure 3.16: ENC in the calibration mode (high gain) measurements.

To verify the noise performance of the prototype ASIC, the Equivalent Noise Charge (ENC) was calculated from the gain and noise measurements. In Figure 3.16a the ENC dependence on the input capacitance is shown in the calibration mode. The specified value of ENC below 1000 e^- at 10 pF of input capacitance is clearly met here. Even for the highest input capacitance of 50 pF, the ENC equal to 2200 e^- allows to keep the SNR for single MIP above 10. The spreed of ENC between channels at 10 pF of input capacitance is shown in Figure 3.16b. The lower values for side channels 0 and 8 can be an artifact caused by the parasitic capacitance between the input of the side channel and the test pulse path. The ENC for all the channels remains below 950 e^-.

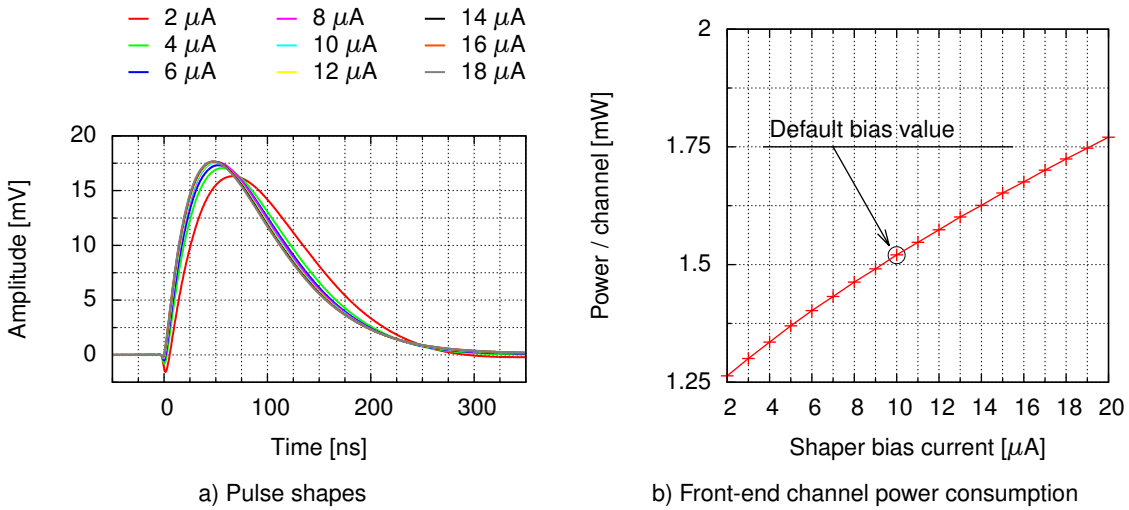
The power consumption requirements for the LumiCal are not very restrictive since the power pulsing can be used, as it was already discussed. The power pulsing was implemented in the designed prototype as a dedicated control circuit which switches off the biasing currents of the preamplifier

and shaper amplifiers. This allows to reduce the power consumption to almost zero (apart from the leakage currents) during the switch off phase. It was experimentally verified that the whole front-end circuit recovery time from this phase is of the order of single μs which is negligible comparing to the 200 ms gap between the bunches in the ILC experiment. The nominal biasing value corresponds to 1.55 mW peak power consumption of single front-end channel. The detailed measurements of peak power were done for different bias currents taking into account their influence on the front-end performance. In Figure 3.17a the effect of the preamplifier bias current on the pulse shape is presented, together with the corresponding peak power consumption, shown in Figure 3.17b. A large power saving, by almost factor of 2, is possible with reduced preamplifier bias current from the nominal value of 13 μA to 5 μA. As it can be seen from Figure 3.17a, such change does not affect significantly the front-end performance since the gain and peaking time for the lowered bias current differ by 15 % compared to the default bias values. Similar analysis can be done for the shaper bias



a) Pulse shapes b) Front-end channel power consumption

Figure 3.17: Front-end performance vs preamplifier bias current at 10 pF input capacitance.



a) Pulse shapes b) Front-end channel power consumption

Figure 3.18: Front-end performance vs shaper bias current at 10 pF input capacitance.

current as it is shown in Figure 3.18. The default bias value of 10 μA can be lowered even to 4 μA almost without any impact on the pulse shape shown in Figure 3.18a. The peaking time increases by 10 % while the gain is lowered only by 3 %. Setting both biasing currents to the proposed lower values allows to reduce the peak power consumption by a factor of 2.5 to the value of 0.6 mW. Such change would result in increase of ENC from 950 e^- to less than 1100 e^-, which is still acceptable. Assuming the use of power pulsing with a duty factor of about 0.01 the averaged power consumption below 10 μW per channel may be easily obtained.

3.2.3 Pulse shape considerations

As it was previously shown in Figure 3.13a, the obtained pulse shape differs from an ideal CR-RC shape, described by equation 3.6. The mentioned formula was derived assuming ideal amplifiers in the preamplifier and shaper circuits, i.e. amplifiers with infinite low frequency gain k and infinite bandwidth. Since the shaper amplifier parameters are far from this assumption, as it was shown in Figure 3.11, the ideal shaper amplifier presented in Figure 3.7 should be replaced by more realistic model described with finite low frequency gain and a single pole transfer function $A(s)$ as follows:

$$A(s) = \frac{k\omega_a}{s + \omega_a}\,, \tag{3.8}$$

where k is low frequency gain and ω_a is pole of real amplifier transfer function, which may be deduced from Figure 3.11, to be equal to $1.25 \cdot 10^6$ rad/s. With this assumption the simplified schematic of the LumiCal front-end, presented in Figure 3.7, can be replaced with the one shown in Figure 3.19. Since the transfer function of the shaper including PZC network does not depend

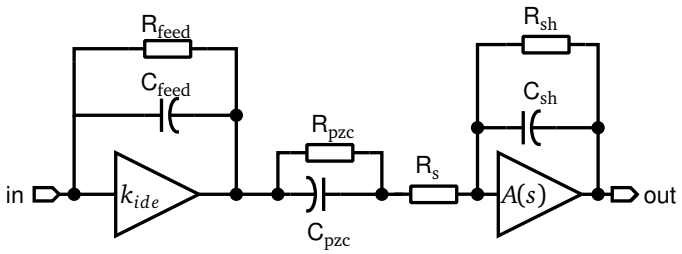


Figure 3.19: Simplified schematic of a front-end electronics for the LumiCal with real shaper amplifier model.

on the gain mode, the simplified preamplifier feedback circuit was used for these considerations. Introducing the denotations 3.9, the transfer function of the whole front-end, given by equation 3.6 for ideal amplifier, can be rewritten as 3.10:

$$\begin{aligned}
\omega_{feed} &= \frac{1}{R_{feed}C_{feed}}\,, & \omega_{pzc} &= \frac{1}{R_{pzc}C_{pzc}}\,,\\
\omega_{sh2} &= \frac{1}{R_{sh}C_{sh}}\,, & \omega_{sh1} &= \frac{R_{pzc}+R_s}{R_sR_{pzc}C_{pzc}}\,,\\
\omega_{ssh} &= \frac{1}{R_sC_{sh}}\,,
\end{aligned} \tag{3.9}$$

$$\frac{U_{out}(s)}{I_{in}(s)} = \frac{1}{R_sC_{sh}C_{feed}} \times \frac{1}{(s+\omega_{feed})} \times \frac{(s+\omega_{pzc})}{(s+\omega_{sh1})\cdot(s+\omega_{sh2})}\,. \tag{3.10}$$

With $\omega_{feed}=\omega_{pzc}$, as it is required for the PZC, and $\omega_{sh}=\omega_{sh1}=\omega_{sh2}$, the denominator of equation 3.10 has a double real root $(-\omega_{sh})$ what corresponds to the ideal CR-RC shape in the time domain.

Using realistic transfer function 3.8 of the shaper amplifier, the transfer function of the circuit presented in Figure 3.19 can be written as:

$$\frac{U_{out}(s)}{I_{in}(s)}=\frac{1}{R_s C_{sh} C_{feed}}\times\frac{1}{(s+\omega_{feed})}\times\frac{1}{\left(1+\frac{1}{k}\right)}\times\frac{(s+\omega_{pzc})}{\frac{1}{\omega_a(k+1)}s^3+\left[1+\frac{\omega_{sh1}+\omega_{sh2}+\omega_{ssh}}{\omega_a(k+1)}\right]s^2+\left[\frac{\omega_{sh1}\omega_{sh2}+\omega_{pzc}\omega_{ssh}}{\omega_a(k+1)}+\frac{\omega_{ssh}}{(k+1)}+\omega_{sh1}+\omega_{sh2}\right]s+\frac{\omega_{pzc}\omega_{ssh}}{(k+1)}+\omega_{sh1}\omega_{sh2}}. \tag{3.11}$$

It needs to be noted that transfer function 3.11 can be easily reduced to ideal one 3.10 if the low frequency gain of shaper amplifier $k\to\infty$. By assuming $\omega_{feed}=\omega_{pzc}$, the poles of transfer function 3.11 are given by roots of the cubic equation. Since the general formulas for these roots are rather complicated, the calculations were done numerically. In this case one real s_1 and two complex conjugate $s_{2,3}$ roots can be found as follow:

$$s_1=-8.959\cdot10^8\left[\frac{\text{rad}}{\text{s}}\right],\qquad s_{2,3}=-1.988\cdot10^7\pm8.369\cdot10^6 j\left[\frac{\text{rad}}{\text{s}}\right], \tag{3.12}$$

and the pulse in the time domain will be in general described as:

$$p(t)=e^{\Re(s_{2,3})t}\left\{2A\sin\left[\Im(s_{2,3})\right]-2B\cos\left[\Im(s_{2,3})\right]\right\}+e^{s_1 t}. \tag{3.13}$$

The pulse shape described by equation 3.13, together with the real pulse obtained from the measurements for 4 fC of input charge, are shown in Figure 3.20. Since both curves are in very good agreement, it may be concluded that the non-ideality of the shaper amplifier is responsible for the observed pulse shape.

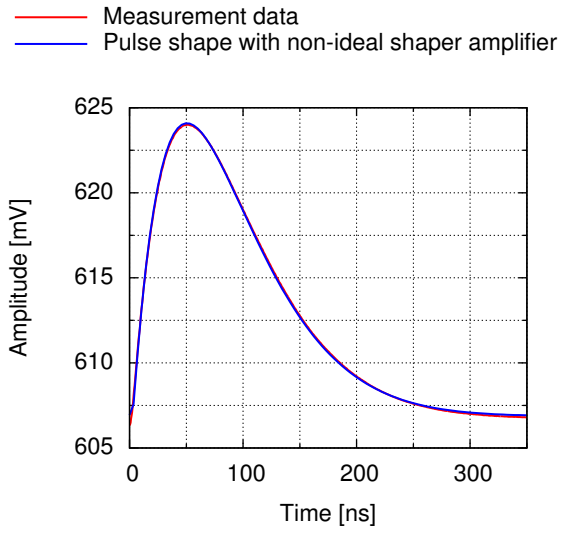


Figure 3.20: Front-end pulse with real shaper amplifier.

3.3 Successive Approximation Register (SAR) ADC

For the existing LumiCal readout, a 10-bit ADC prototype was previously designed and fabricated in the AMS 350 nm technology, using the pipeline architecture [63]. Since the resolution of pipeline ADC depends mainly on the precision of signal multiplication by two in each pipeline stage, the amplifier with high enough (corresponding to the desired resolution) open loop gain was necessary. In the existing design, a telescopic cascode amplifier, providing more than 100 dB open loop gain, was used. However, the power consumption of a high-gain analogue amplifier is rather high and cannot be easily decreased without performance degradation. On the other hand, the pipeline architecture offers a very high maximum sampling rate, not limited by the speed of a digital circuitry. Therefore the pipeline architecture was well suited for the technology with high intrinsic gain and limited digital speed such as the AMS 350 nm.

As it was previously shown, modern technologies suffer from significantly lower intrinsic gain while offering substantially higher maximum frequency for digital circuits. For this reason a SAR architecture was proposed for a new 10-bit ADC prototype as a more suitable for modern technologies. Since the SAR architecture comprises almost only digital or mixed-mode circuits, low intrinsic gain does not have large influence on the SAR performance. The maximum sample rate of the SAR is limited mainly by digital part, so the technology offering higher operation frequency is greatly appreciated.

3.3.1 Basics of SAR architecture

The successive approximation is a widely used algorithm for finding the unknown input value by approaching it with exponentially decreasing steps. The guessed value is increased/decreased in each step i by $1/2^i$ fraction of an arbitrary chosen reference value, greater than the largest possible input value. The precision of the successive approximation algorithm, defined as the difference between the input and the guessed value, depends of the number n of executed steps and is equal to $1/2^n$ fraction of the reference value.

The basic SAR ADC architecture, shown in Figure 3.21a, comprises a S&H circuit which stores the input sample during conversion, a DAC providing the guessed value, a comparator, and a control logic. An example of conversion process for a 3-bit SAR ADC is shown in Figure 3.21b. The complete process comprises the initial, so-called sampling, phase and a bit processing phase, repeated n times

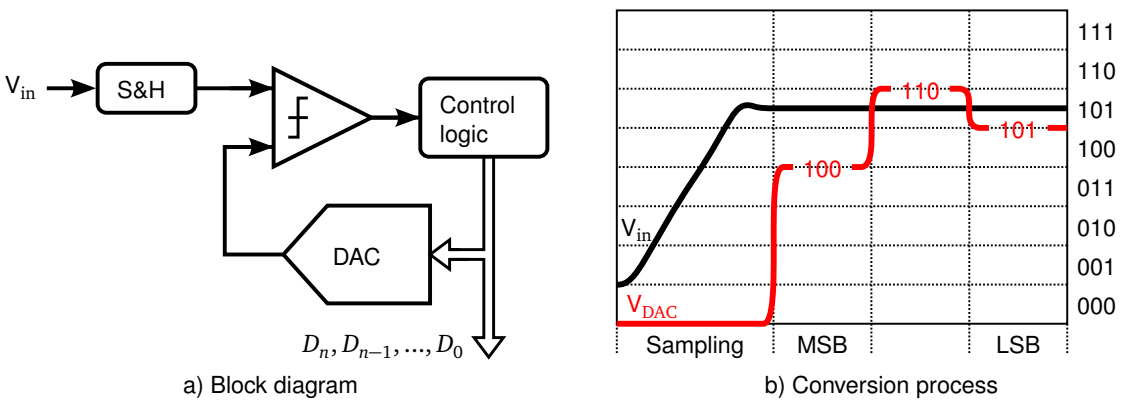


Figure 3.21: Fundamentals of SAR ADC.

for n-bit ADC. In the sampling phase, the input voltage V_{in} is stored into the S&H circuit. The initial guess value V_{DAC} is prepared by setting the DAC to the half of the reference voltage, what corresponds to a middle output code *100*. The processing phase corresponding to bit i starts with the comparison of the stored input and DAC voltages. Depending on the comparison result, the DAC voltage is changed as follows:

- if $V_{in} > V_{DAC}$, bit i, preset to *1* in previous phase, remains unchanged and bit $(i-1)$ is set to *1*, resulting in increasing DAC voltage;
- if $V_{in} < V_{DAC}$, bit i is zeroed and bit $(i-1)$ is set to *1*, resulting in decreasing DAC voltage.

In the presented example, in the first bit processing phase (corresponding to the bit n, the Most Significant Bit (MSB)), the V_{DAC} value is lower than V_{in}. Therefore the DAC voltage is changed by setting the $(n-1)$th bit to *1*, resulting in output code equal to *110*, and increasing the V_{DAC} by one quarter of the reference voltage. In the second bit processing phase, the V_{DAC} is greater than V_{in}, therefore the $(n-1)$th bit of output code is reset to *0* and the $(n-2)$th, the LSB is preset to *1*. The current value of the V_{DAC} voltage is thereby decreased by one-eighth of reference voltage. In the last phase, called LSB phase, the voltages are compared resulting in LSB value, equal *1* in this example (since $V_{in} > V_{DAC}$), and the conversion ends without presetting the DAC voltage.

3.3.2 Capacitive DAC in SAR ADC

The basic SAR architecture presented above has two major cons - require a S&H circuit containing usually a high open loop gain analogue amplifier and utilizes the energy inefficient DAC switching scheme. Since the capacitive DAC array can be used for setting the V_{DAC} voltage, the first of the cons can be easily improved by using the DAC also as the input signal sampling capacitance. The conventional architecture of capacitive DAC, comprising 2^n unit capacitances C_u connected in parallel, is presented in Figure 3.22. During the sampling phase the top node V_x of the DAC array is connected to ground by S_{reset} switch, while the bottom planes of all capacitors are connected to the input voltage V_{in} by their S_i and S_{sample} switches. After that, the S_{reset} opens and the bottom planes of the capacitors are connected to ground by S_i switches resulting in the top node voltage equal to $V_x = -V_{in}$. By switching the S_n, the bottom plate of MSB capacitor is connected to the reference voltage V_{ref}, thereby:

$$V_x = -V_{in} + \frac{2^{n-1}C_u}{2^n C_u} V_{ref} = -V_{in} + \frac{V_{ref}}{2} . \tag{3.14}$$

The general formula describing the top node voltage V_x^i before the ith bit comparison can be ex-

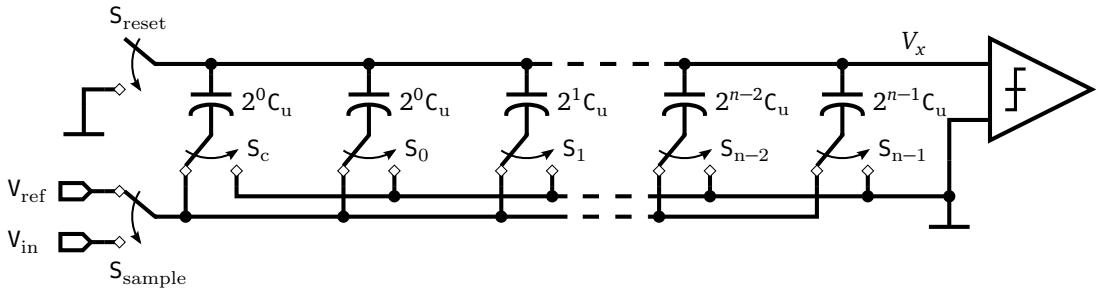


Figure 3.22: Conventional capacitive DAC.

pressed as:

$$V_x^i = -\mathrm{V_{in}} + \frac{1}{2^n}\left[\sum_{k=i+1}^{n-1} D_k \cdot 2^k \mathrm{V_{ref}} + 2^i \mathrm{V_{ref}}\right] . \tag{3.15}$$

The switch $\mathtt{S_c}$ during the whole conversion remains connected to ground, since its unit capacitance $\mathtt{C_u}$ is not directly involved in the conversion, but it is needed to complete the sum of capacitances to 2^n to provide a binary scaling.

Comparison of DAC switching schemes

The second of the cons results from the presetting the DAC voltage before each comparison. In the boundary case, when the input voltage $\mathtt{V_{in}}$ is very low, in each phase i of the conversion the DAC voltage is increased by setting the ith bit to *1* and then decreased by the same value by resetting the ith bit to *0*. This means that, for n-bit ADC, the DAC voltage is changed $2 \cdot n$ times, resulting in large unnecessary energy losses. In the recent years the switching energy losses were significantly improved by optimizing the capacitance DAC configurations and switching schemes. In this work the following schemes were chosen for comparison: already presented Conventional [80, 81], Energy saving [82], Monotonic switching [81, 83], Merge Capacitor Switching (MCS) [83, 84], Early Reset MCS (EMCS) [85], Asymmetric MCS (AMCS) [86, 87], Tri-level switching [88], Switchback Algorithm (SBA) [89], Improved SBA [90] and $\mathtt{V_{cm}}$-based monotonic [91]. Since the design presented in this section comprises a differential architecture, all schemes will be considered as differential. To compare the switching schemes, the sum of energy taken from the reference voltage sources in function of output ADC code was calculated and is shown in Figures 3.23 and 3.24. Each component of these sums was calculated based on the flow of charge occurring during the DAC switching. The energy $\Delta E_{2\to1}$ taken from the source providing a constant voltage $v_{ref}(t) = \mathrm{V_{ref}}$ during the transition of duration $\Delta t = t_2 - t_1$ can be written as [80]:

$$\Delta E_{2\to1} = \int_{t_1}^{t_2} i_{ref}(t) \cdot v_{ref}(t) dt = \mathrm{V_{ref}} \int_{Q(t_1)}^{Q(t_2)} \frac{dQ}{dt} dt = \mathrm{V_{ref}} \int_{t_1}^{t_2} dQ . \tag{3.16}$$

Since the charge Q stored in a capacitor is a product of capacitance C and voltage across it V, equation 3.16 can be rewritten as:

$$\Delta E_{2\to1} = C \cdot V_{ref} \left[V(t_2) - V(t_1)\right] . \tag{3.17}$$

The energies shown in Figures 3.23 and 3.24 are therefore sums of all energies $\Delta E_{2\to1}$ from transitions needed to obtain a 10-bit wide ADC output code. These energies can be averaged over the codes to obtain an average energy per conversion $\overline{E}$ useful for a fast comparison of the switching schemes, presented in Table 3.5. The efficiency E_{eff} of each scheme, compared to the conventional one treated as the reference, shown in this table, was calculated as:

$$E_{eff} = 1 - \frac{\overline{E}}{\overline{E}_{conventional}} . \tag{3.18}$$

In the differential architecture, the DAC network, as shown in Figure 3.22, is doubled providing two top node voltages - positive $V_{x,p}^i$ and negative $V_{x,n}^i$, connected to comparator inputs. The comparator input common mode voltage $V_{cm,cmp}^i$ for each bit i during the conversion can be calculated as:

$$V_{cm,cmp}^i = \frac{1}{2}\left(V_{x,p}^i + V_{x,n}^i\right) . \tag{3.19}$$

As it will be shown later, this parameter is crucial for the comparator architecture. In the conventional switching scheme the comparator input common mode voltage is constant during the whole conversion and equal to half of the reference voltage, which allows to simplify the comparator design.

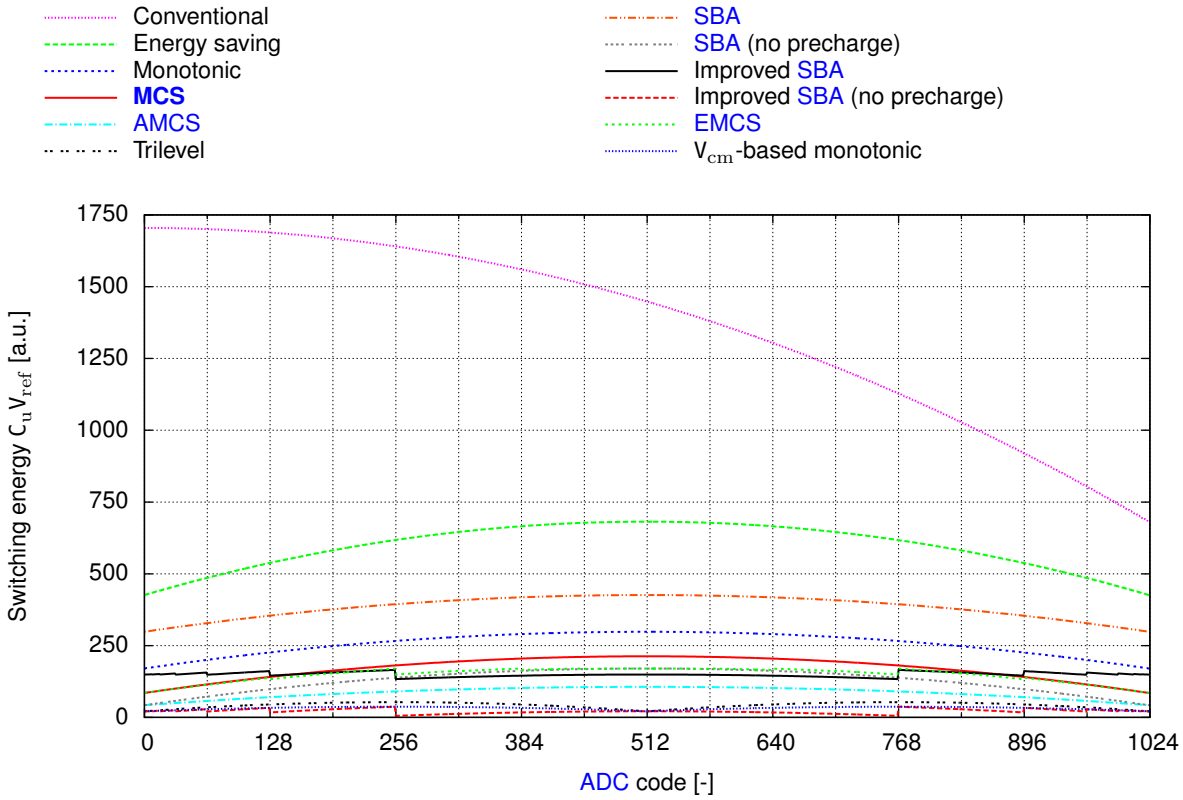


Figure 3.23: SAR switching energy for different switching schemes.

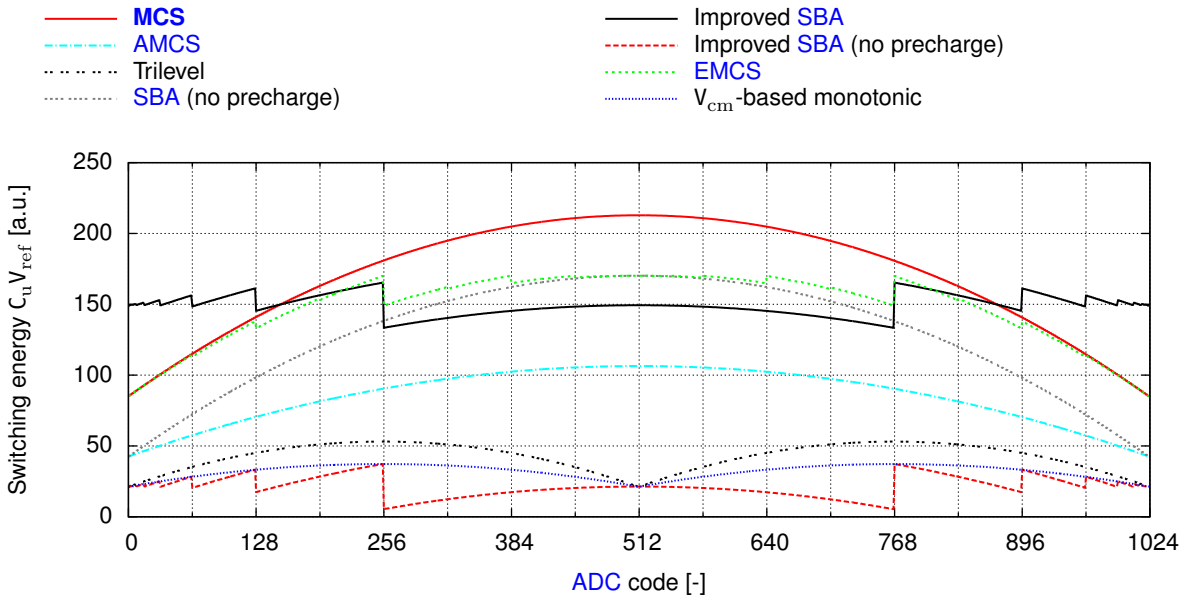


Figure 3.24: SAR switching energy for different switching schemes.

Algorithm	Average energy $\overline{E}$ [a.u.]	Efficiency E_{eff} [%]	No. of unit capacitances C_u	Comparator common mode voltage $V^i_{cm,cmp}$
Conventional	1363.3	-	$2 \cdot 2^n$	constant
Energy saving	596.3	56.3	$2 \cdot 2^n$	constant
SBA	383.5	71.9	$2 \cdot 2^{n-1}$	variable
Monotonic switching	255.5	81.3	$2 \cdot 2^{n-1}$	variable
Improved SBA	173.6	87.3	$2 \cdot 2^{n-2}$	variable
MCS	170.2	87.5	$2 \cdot 2^{n-1}$	constant
EMCS	148.8	89.1	$2 \cdot 2^{n-1}$	constant
SBA, no precharge	127.5	90.7	$2 \cdot 2^{n-1}$	variable
AMCS	85.1	93.8	$2 \cdot 2^{n-2}$	constant
Improved SBA, no precharge	45.6	96.7	$2 \cdot 2^{n-2}$	variable
Tri-level switching	42.4	96.9	$2 \cdot 2^{n-2}$	variable
V_{cm}-based monotonic	31.9	97.7	$2 \cdot 2^{n-2}$	variable

Table 3.5: Brief summary of the presented DAC switching schemes for 10-bit ADC.

However, some of the presented schemes utilize a variable input common mode resulting in higher requirements for the comparator. Therefore, a constant or a variable common mode implementation is also shown in Table 3.5.

Some of the presented switching schemes utilize the top plane sampling in which the input signals $V_{in,p}$ and $V_{in,n}$ are connected during the sampling phase to the top nodes ($V_{x,p}$ and $V_{x,n}$) instead of bottom planes, as was shown for the conventional switching scheme in Figure 3.22. The top plane sampling allows to perform the MSB comparison without any DAC switching, so only $2 \cdot 2^{n-1}$ unit capacitances C_u are needed in total, two times less than in the conventional scheme requiring $2 \cdot 2^n$ C_u. Therefore, the total number of capacitances required by the presented schemes, is listed also in Table 3.5.

For the SAR ADC project, presented in this section, the MCS switching scheme was used. As can be seen from Table 3.5, a more energy efficient schemes are possible, but only two of them, the EMCS and AMCS have a constant common mode voltage, which was considered a basic requirement for the switching scheme, and both of them were proposed after the first ADC prototype was designed.

MCS and split binary-weighted architecture

The chosen MCS switching scheme, beside the already described top plane sampling, uses three reference voltage levels (top V_{ref}, bottom V_{low} and middle V_{cm}), instead of two used by the conventional one. Typically, to obtain the maximum possible dynamic range, the V_{low} is ground, the V_{ref} is equal to supply voltage (1.2 V in both, CMOS 130 nm process A and CMOS 130 nm process B technologies) and the V_{cm} is set to half of the reference voltage V_{ref}. The schematic of the differential DAC utilizing the MCS switching scheme is presented in Figure 3.25. During the sampling phase, the input voltages $V_{in,p}$ and $V_{in,n}$ are connected to the top nodes $V_{x,p}$ and $V_{x,n}$ through the sampling switches S_{sample}, while the bottom planes of all capacitors are connected to V_{cm} voltage. After the sampling the first comparison is done resulting in MSB equal one if $V_{x,p} = V_{in,p} > V_{in,n} = V_{x,n}$ or zero otherwise. Assuming that $V_{x,p} < V_{x,n}$ (MSB=*0*), the $S_{n-2,p}$ connects the bottom plate of MSB capacitance $2^{n-2}C_u$ to the reference voltage V_{ref}, disconnecting it simultaneously from V_{cm}, resulting in increasing $V_{x,p}$

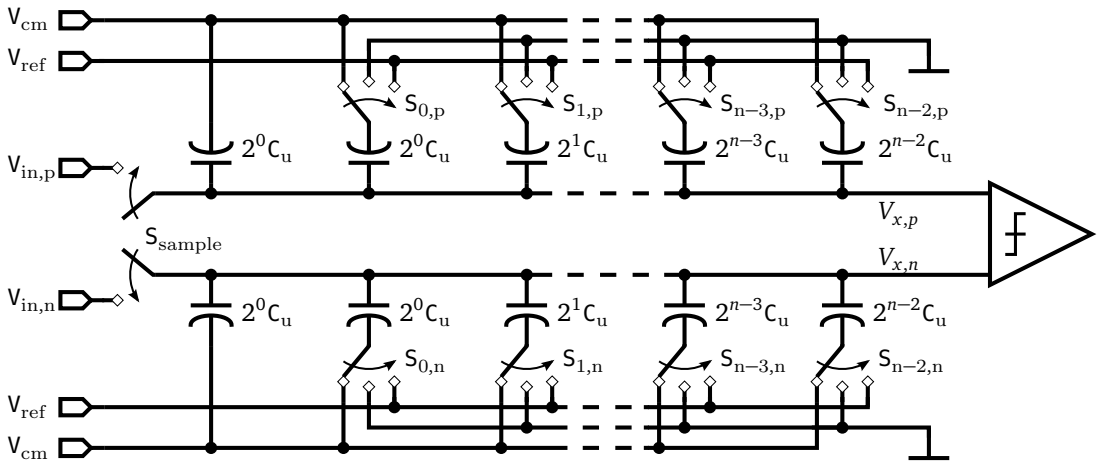


Figure 3.25: Differential DAC utilizes MCS switching scheme.

by one quarter of reference voltage, while $S_{n-2,n}$ connects bottom plate of its capacitance to ground, decreasing $V_{x,n}$ by one quarter of reference voltage. The differential voltage $V_{x,diff}$ can be therefore written as:

$$V_{x,diff} = V_{x,p} - V_{x,n} = \left(v_{in,p} + \frac{V_{ref}}{4}\right) - \left(V_{in,n} - \frac{V_{ref}}{4}\right) = V_{in,diff} + \frac{V_{ref}}{2}, \tag{3.20}$$

and is equal to the voltage V_x for conventional scheme (equation 3.14).

The 10-bit ADC with differential DAC in the MCS switching scheme requires 1024 unit capacitances C_u. The minimum value of C_u is determined by thermal noise of the total DAC capacitance and matching between capacitances in the given technology. The both issues are discussed in details in the next section, however, one general remark has to be given here. For a 10-bit ADC, the value of unit capacitance C_u, resulting from these considerations, is significantly lower than the minimum capacitance available in CMOS 130 nm process A and CMOS 130 nm process B. To enable the energy and area savings, the effective unit capacitance can be reduced by using the split binary-weighted architecture for DAC, shown in single-ended implementation in Figure 3.26. The DAC is split into two L-bits and M-bits binary-weighted arrays, where $(n-1) = M+L$ for the MCS scheme. The value of the bridge capacitor C_s and complement capacitance C_{cl} have to be chosen in order to provide a binary scaled changes of DAC voltage V_x during switching, both in M-bits and L-bits sub-arrays. In order to determinate the C_s and C_{cl} values, a general formula describing the DAC output voltage change ΔV_x in any of the conversion steps has to be derived. The total capacitances C_M and C_L of

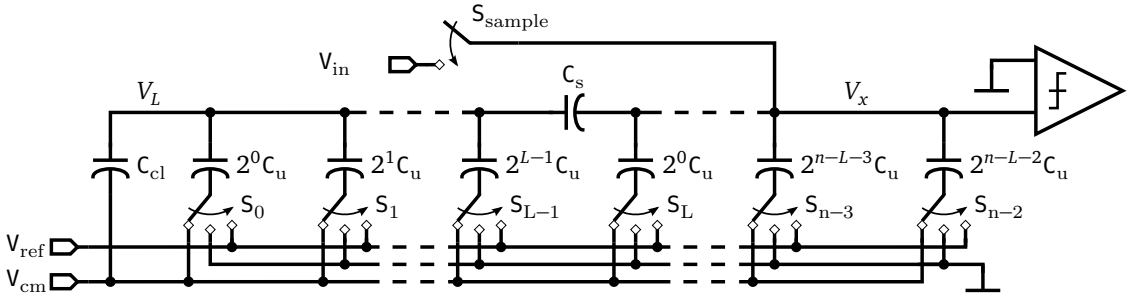


Figure 3.26: Single ended, split binary-weighted DAC.

the M-bit and L-bit sub-arrays can be expressed as:

$$C_M = \sum_{i=0}^{n-L-2} 2^i \mathrm{C_u} = \left(2^{n-L-1}-1\right)\mathrm{C_u}\,,$$
$$C_L = \sum_{i=0}^{L-1} 2^i \mathrm{C_u} + \mathrm{C_{cl}} = \left(2^{L}-1\right)\mathrm{C_u} + \mathrm{C_{cl}}\,. \tag{3.21}$$

When processing bit k, the switch $\mathtt{S}_\mathrm{k}$ changes the bottom plate voltage at the corresponding capacitance from $\mathtt{V}_\mathrm{cm}$ to $\mathtt{V}_\mathrm{ref}$ or to ground. Without loosing the generality, this change can be denoted as ΔV_k, regardless its value. If switch $\mathtt{S}_\mathrm{k}$ is located in M-bits sub-array the DAC output voltage change $\Delta V_x^{M,k}$ can be expressed as:

$$\Delta V_x^{M,k} = \Delta V_k \cdot \frac{2^{k-L}\mathrm{C_u}}{C_M + \frac{C_L \mathrm{C_s}}{C_L + \mathrm{C_s}}} \qquad k \in (L, n-2)\,. \tag{3.22}$$

For the L-bit sub-array, the corresponding voltage change $\Delta V_x^{L,k}$ can be written as:

$$\Delta V_x^{L,k} = \Delta V_k \cdot \frac{2^{k}\mathrm{C_u} \cdot \mathrm{C_s}}{C_L + \mathrm{C_s}} \cdot \frac{1}{C_M + \frac{C_L \mathrm{C_s}}{C_L + \mathrm{C_s}}} \qquad k \in (0, L-1)\,. \tag{3.23}$$

The equations 3.22 and 3.23 can be rewritten by denoting their common component as:

$$K = \Delta V_k \cdot \frac{1}{C_M + \frac{C_L \mathrm{C_s}}{C_L + \mathrm{C_s}}}\,, \tag{3.24}$$

what leads to the forms:

$$\begin{aligned} \Delta V_x^{M,k} &= K \cdot \left[2^{k-L}\mathrm{C_u}\right] && k \in (L, n-2)\,, \\ \Delta V_x^{L,k} &= K \cdot \left[2^{k}\mathrm{C_u}\right] \cdot \frac{\mathrm{C_s}}{C_L + \mathrm{C_s}} && k \in (0, L-1)\,. \end{aligned} \tag{3.25}$$

As can be seen from the above equations, $\Delta V_x^{M,k} = 2\Delta V_x^{M,k-1}$ and $\Delta V_x^{L,k} = 2\Delta V_x^{L,k-1}$ for any k. In order to ensure the binary scaled changes over the whole array (comprising both the M-bit and L-bit sub-arrays), a following condition has to be met:

$$\Delta V_x^{M,k}\Big|_{k=L} = 2\Delta V_x^{L,k}\Big|_{k=L-1}\,, \tag{3.26}$$

what can be written as:

$$K \cdot \left[2^0 \mathrm{C_u}\right] = 2 \cdot K \cdot \left[2^{L-1}\mathrm{C_u}\right] \cdot \frac{\mathrm{C_s}}{C_L + \mathrm{C_s}}\,,$$
$$1 = 2^L \frac{\mathrm{C_s}}{C_L + \mathrm{C_s}}\,, \tag{3.27}$$

leading to the formula for the bridge capacitance $\mathtt{C}_\mathrm{s}$:

$$\mathrm{C_s} = \frac{C_L}{2^L - 1}\,. \tag{3.28}$$

For the exemplary split architecture presented in Figure 3.26 the total capacitance of L-bits sub-array is given by the equation 3.21 and so the bridge capacitance should be equal to:

$$\mathrm{C_s} = \frac{\left(2^L - 1\right)\mathrm{C_u} + \mathrm{C_{cl}}}{2^L - 1} = \mathrm{C_u} + \frac{\mathrm{C_{cl}}}{2^L - 1} \,. \tag{3.29}$$

To ensure a proper matching of the bridge capacitance and all others DAC capacitances, which is required to avoid ADC nonlinearities, the bridge capacitance has to be equal to an integer multiple of unit capacitance $\mathrm{C_u}$. For the given architecture, this condition can be easily met by putting the $\mathrm{C_{cl}}$= 0. However, a more complex split binary-weighted architectures can be considered. Although this was not discussed, the parasitic capacitance on the V_L node of L-bit sub-array degrades the ADC linearity. In order to reduce this effect, the bridge capacitance $\mathrm{C_s}$ may be increased to $2\mathrm{C_u}$ by putting the complement capacitance $\mathrm{C_{cl}}$=$(2^L - 1)\mathrm{C_u}$. This increases the L-bit sub-array total capacitance C_L, but allows to compensate the parasitic capacitance by properly chosen $\mathrm{C_{cl}}$ value. Therefore, by slightly decreasing the complement capacitance value, the parasitics effect can be almost completely removed by setting the sum of $\mathrm{C_{cl}}$ and parasitic capacitance equal to $(2^L - 1)\mathrm{C_u}$.

Unit capacitance considerations

The value of unit capacitance $\mathrm{C_u}$ has to be set respectively to its matching properties. The standard deviation σ_u of the mismatch between two capacitances $\mathrm{C_u}$ can be expressed using its layout geometrical parameters as follow [92]:

$$\mathrm{C_u} = K_C \cdot A_u \,, \tag{3.30}$$

$$\frac{\sigma_u}{\mathrm{C_u}} = \frac{1}{\sqrt{2}} \cdot \frac{K_\sigma}{\sqrt{A_u}} \,, \tag{3.31}$$

where K_C is capacitance density [fF/μm^2], K_σ is matching parameter (technology dependent) [%·μm] and A_u is area of capacitor $\mathrm{C_u}$ [μm^2]. Basing on these equations, the sigma of Differential Nonlinearity (DNL) σ_{DNL} for a conventional DAC can be calculated as [92]:

$$\sigma_{DNL} = \sqrt{2^n - 1} \cdot \frac{\sigma_u}{\mathrm{C_u}} \qquad [LSB] \,. \tag{3.32}$$

Typically, condition $3 \cdot \sigma_{DNL}$ <LSB should be set to achieve the required linearity, what, by combining equations 3.31 and 3.32 for the MCS switching scheme, gives:

$$3\sqrt{2^{n-1} - 1} \cdot \frac{1}{\sqrt{2}} \cdot K_\sigma \cdot \sqrt{\frac{K_C}{\mathrm{C_u}}} < 1 \,. \tag{3.33}$$

Since in the differential architecture the signal is doubled while the nonlinearity introduced by the mismatch is only $\sqrt{2}$ times higher, the minimum unit capacitance can be $\sqrt{2}$ smaller than in a single-ended case presented in equation 3.33. Keeping this in mind, the condition for the minimum value of unit capacitance $\mathrm{C_u}$ can be written as:

$$\mathrm{C_u} > \frac{9}{2\sqrt{2}} \left(2^{n-1} - 1\right) K_\sigma^2 K_c \,. \tag{3.34}$$

The equation similar to 3.34 for the split binary-weighted DAC can be derived under assumption that $L < M$ and the mismatch of M-bit DAC will be the main contribution to the overall nonlinearity error. In such case equation 3.32 can be rewritten as [92]:

$$\sigma_{DNL,M} = \sqrt{2^{n-L-1} - 1} \cdot \frac{\sigma_u}{\mathrm{C_u}} \cdot \frac{\mathrm{V_{ref}}}{2^{n-L-1}} \,. \tag{3.35}$$

Therefore, the minimum unit capacitance in split binary-weighted DAC C_u can be expressed as [92]:

$$C_u > \frac{9}{2\sqrt{2}} \cdot 2^{2L} \left(2^{n-L-1} - 1\right) K_\sigma^2 K_c \ . \tag{3.36}$$

In the CMOS 130 nm process A technology the capacitance density is equal to K_C=2.05 fF/μm^2, while the matching parameter K_σ=4.12 %·μm. Therefore, the minimum unit capacitance $C_{u,split}$ can be calculated for different DAC split networks between L-bit and M-bit, where $L+M=(n-1)=9$ for 10-bit ADC. The number of unit capacitances C_u required in each split configuration and the DAC capacitance seen on each of the differential inputs, expressed as:

$$C_{in} = 2^{n-L-1} C_u \ , \tag{3.37}$$

were also calculated. The approximated area occupied by the DAC was estimated as a product of unit capacitances number and area occupied by single unit capacitance. It has to be noted that this estimation is based only on the capacitance density K_c, and does not take into account additional area required for the routing. Since a minimum possible capacitance is 60 fF, which is quite large, two of them can be connected in series resulting in a minimum possible C_u capacitance of 30 fC. Though the minimum value of the unit capacitance C_u, given by equation 3.36 resulting from the matching considerations, may be significantly smaller for some split configurations, the lowest achievable unit capacitance C_u^{real} is always limited to 30 fC. Therefore, both the matching-dependent unit capacitance C_u and obtainable C_u^{real} are presented, and the DAC total capacitance and its area are calculated for the second one. The calculated parameters are presented in Table 3.6. As can be seen from this table, the optimum area can be obtained for the $M=6$ and $L=3$ split. The minimum unit capacitance C_u=C_u^{real}=44.6 fC was slightly relaxed to 40 fC implemented as serial connection of two 80 fC capacitors. For these reasons the $M=6$ and $L=3$ split was chosen for the ADC design in the CMOS 130 nm process A technology.

M	L	C_u [fF]	C_u^{real} [fF]	No. of C_u	C_{in} [pF]	≈Area [μm^2]
9	0	5.7	30.0	1024	15.36	14 985
8	1	11.3	30.0	514	7.68	7 522
7	2	22.5	30.0	262	3.84	3 834
6	**3**	**44.6**	**44.6**	**142**	**2.86**	**3 092**
5	4	87.9	87.9	94	2.81	4 029

Table 3.6: DAC parameters for different split networks in CMOS 130 nm process A technology.

Unfortunately, the matching parameter K_σ is not specified in CMOS 130 nm process B technology, so the precise calculation of minimum unit capacitance C_u is not possible. But since the capacitance density K_C in this technology, equal to 1.55 fF/μm^2, is 1.33 times smaller than in CMOS 130 nm process A, the C_u is also, from the equation 3.36, 1.33 smaller and equal 33.3 fF, under the assumption that matching parameters in both technologies are equal. To test the matching in CMOS 130 nm process B, the C_u was set to minimum available 26.2 fF. The results obtained from the MC simulations show that the condition $3 \cdot \sigma_{DNL}$ <LSB is still met even for such small unit capacitance, what shows that matching parameter K_σ in CMOS 130 nm process B is better than in CMOS 130 nm process A. With the C_u=26.2 fF the DAC input capacitance C_{in} in CMOS 130 nm process B is equal to 1.68 pF, and the estimated area is approximately 2400 μm^2.

The thermal noise $\overline{V_{noise}^2}$ for temperature T of capacitive DAC with total capacitance C_{tot} can be written as follows:

$$\overline{V_{noise}^2} = \frac{k_B T}{C_{tot}}, \tag{3.38}$$

where k_B is Boltzmann constant. Similarly to the matching case, the condition $3\sqrt{\overline{V_{noise}^2}} < 0.5\text{LSB}$ can be set. Since $\text{LSB}=\text{V}_{\text{ref}}/2^n$, the minimum total DAC capacitance due to the thermal noise can be expressed as:

$$C_{tot} > 36 \cdot \frac{2^{2n} k_B T}{\text{V}_{\text{ref}}^2}. \tag{3.39}$$

For V_{ref}=1.2 V and n = 10-bit resolution, the minimum total capacitance in room temperature T=293 K is equal to 26.5 fF and is comparable to the unit capacitance in CMOS 130 nm process B technology. Since the total DAC capacitance in both technologies is three orders of magnitude greater than the unit capacitance, the influence of thermal noise is negligible.

3.3.3 Chosen SAR ADC architecture

The block diagram of the designed 10-bit SAR ADC is presented in Figure 3.27. Since the designs in both CMOS 130 nm technologies, aside irrelevant details, are almost identical, they are presented together. The SAR ADC comprises a split DAC discussed in details in previous section, a pair of bootstrapped sampling switches, a dynamic comparator, and an asynchronous control logic.

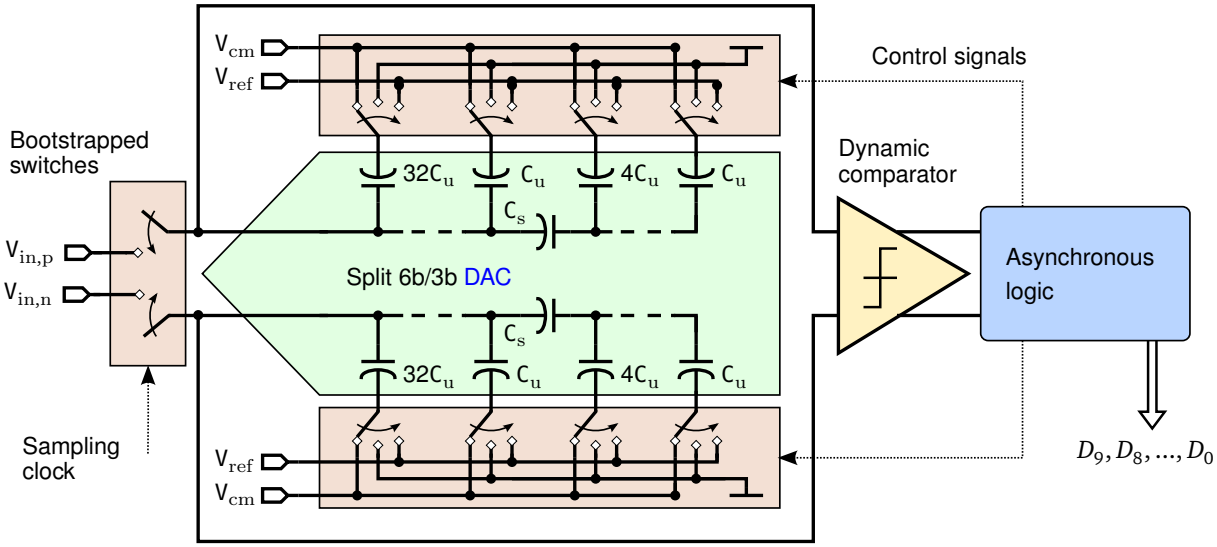


Figure 3.27: Block diagram of the 10-bit SAR ADC.

Bootstrap switch

To increase the linearity of the ADC bootstrapped switches [93], presented in Figure 3.28, were used as sampling circuit. The bootstrapped architecture allows to both, significantly reduce the resistance of sampling switch M_1 and equalize the charge injection into DAC array for different input voltages V_{in}. Both of these effects strongly depend on the source – gate voltage V_{gs1} of the M_1 transistor, so it

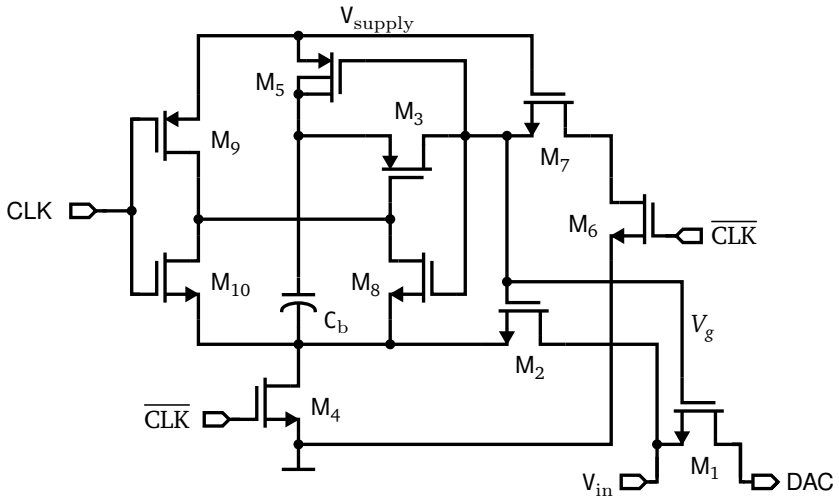


Figure 3.28: Schematic of bootstrapped switch.

should be kept constant for any input voltage. Since V_{gs1} can be written as:

$$V_{gs1} = V_g - \mathrm{V_{in}}\,, \tag{3.40}$$

the V_g voltage should be equal $\mathrm{V_{in}} + \mathrm{V_{supply}}$, to achieve the lowest switch resistance at $V_{gs1} = \mathrm{V_{supply}}$. To obtain that, in the preset phase, shown in Figure 3.29a, the $\mathtt{C_b}$ capacitor is charged to $\mathtt{V_{supply}}$ voltage through switches $\mathtt{S_3}$ and $\mathtt{S_4}$. At the same time, the gate of the sampling transistor $\mathtt{M_1}$ is tied to ground through $\mathtt{S_5}$ switch, keeping the $V_{gs1} \leq 0$ V. During the sampling phase, shown in Figure 3.29b, the capacitor $\mathtt{C_b}$ is connected between the source and gate of $\mathtt{M_1}$ transistor through $\mathtt{S_1}$ and $\mathtt{S_2}$ switches, setting the $V_g = \mathrm{V_{in}} + \mathrm{V_{supply}}$ as required. In the actual implementation (Figure 3.28), the $\mathtt{M_2}$, $\mathtt{M_3}$, $\mathtt{M_4}$, $\mathtt{M_5}$, and $\mathtt{M_6}$ correspond to the $\mathtt{S_1}$, $\mathtt{S_2}$, $\mathtt{S_3}$, $\mathtt{S_4}$, and $\mathtt{S_5}$ switches from Figure 3.29. Since, in the extreme case of $\mathrm{V_{in}} = \mathrm{V_{supply}}$, the V_g voltage in the sampling phase is equal $2 \cdot \mathrm{V_{supply}}$, additional transistors $\mathtt{M_7}$–$\mathtt{M_{10}}$ are needed to ensure that voltage across any transistor does not exceed the maximum value allowed in given technology, typically $1.25 \cdot \mathrm{V_{supply}}$. In particular, it should be noted that the body of the $\mathtt{M_5}$ is connected to its drain instead of source. This is due to the fact that in the sampling phase the drain potential of the $\mathtt{M_5}$ can reach $2 \cdot \mathrm{V_{supply}}$, exceeding the source potential. Since the $\mathtt{M_5}$ is a PMOS transistor, its body has to be tied to the highest potential to avoid the forward bias of the drain – body and source – body diodes.

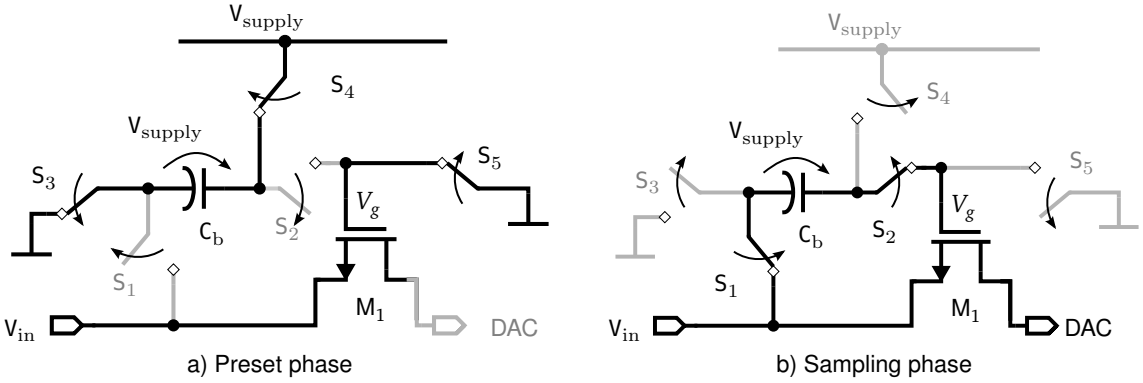


Figure 3.29: Simplified scheme of bootstrapped switch operation.

Dynamic comparator

A comparator is usually the only component with a static power consumption in the SAR ADC architecture. To eliminate completely the static power and to reduce further the power consumption, a dynamic comparator, which dissipates power only during bit cycling process, was designed. The solution with two gain stages and an output-latch stage, providing high enough precision was chosen [94] and is presented in Figure 3.30. During the reset phase (`active` low), transistors M_3 and M_4 are shorted and provide supply voltage to inverters I_1 and I_2. Transistors M_{14} and M_{15} disable the data latch M_8-M_{11} while the M_{12} and M_{13} force the high logic level (*1*) on the outputs $V_{out,p}$ and $V_{out,n}$. On the beginning of the compare phase (just after the rising edge of signal `active`), the input pair transistors M_1 and M_2 start to conduct currents $i_{in,n}$ and $i_{in,p}$ depending on the input voltages $V_{in,n}$ and $V_{in,p}$. The higher of these voltages results in higher corresponding current and higher slew rate at the input of respective inverter I_1 or I_2. Assuming $V_{in,n} < V_{in,p} \Rightarrow i_{in,n} < i_{in,p}$, the slew rate of rising edge on the output of inverter I_2 is higher than on I_1. Therefore, the M_6 transistor is switched on earlier than M_7, storing the comparison result in M_8-M_{11} latch through M_{10} transistor. In the above example, the output voltages $V_{out,p}$, $V_{out,n}$ are then equal to *1* and *0* respectively, indicating that $V_{in,n} < V_{in,p}$. The comparison result is stored in data latch until the next reset phase, independently on the changes of input voltages. It has to be noticed that a small difference between input voltages results in a very similar slew rates what significantly increases the comparator response time. On the other side, to reduce the capacitance load on drains of M_6 and M_7, the dimensions of M_{14} and M_{15} should be rather small, what, together with a low intrinsic gain, results in a large reset time needed for preparing the comparator for the next comparison.

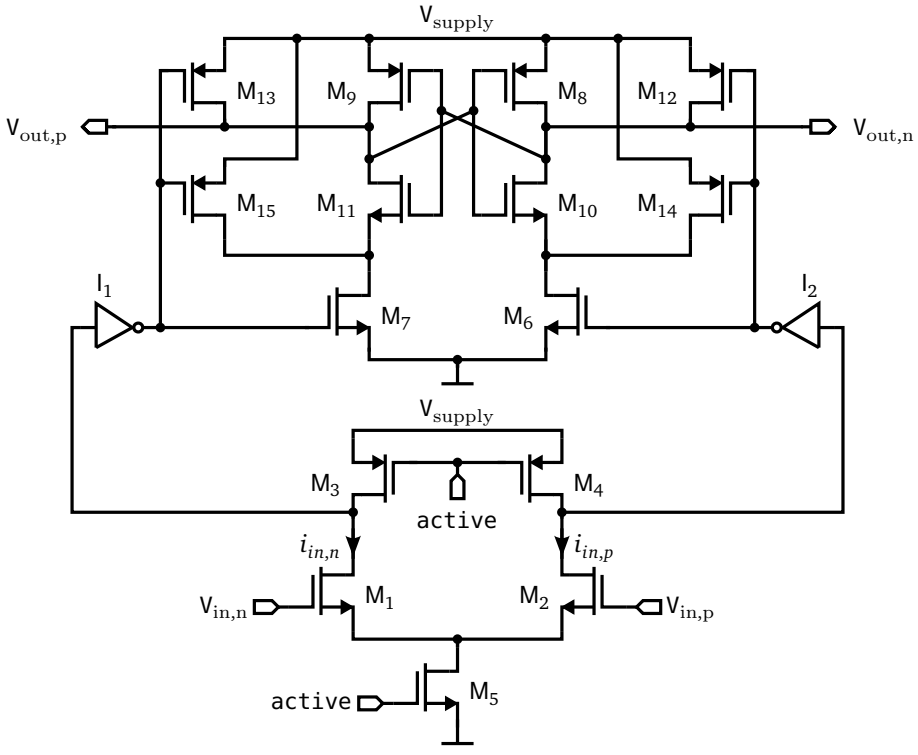


Figure 3.30: Schematic of dynamic comparator.

Control logic

The control logic for SAR ADC can be implemented as synchronous, driven by fast external clock, as well as asynchronous. The first implementation has two major cons: the speed is limited by the frequency of external clock and additional power is consumed by the clock distribution circuitry. Since for n-bit ADC the same circuit is used n times in SAR architecture, an external clock driving synchronous logic has to be at least n times faster than the sampling clock. Aside some more sophisticated realizations, all the actions performed for each bit processing may require more than one clock cycle per bit, multiplying the needed clock frequency even more. It was shown that for SAR architecture, the asynchronous implementation is much more efficient [95] because significantly higher sampling rates together with lower power consumption can be obtained. Since asynchronous logic is driven, as it will be shown later, by a sequence of events, it requires only sampling signal determining the conversion beginning and no other clock is needed for bit cycling. Furthermore, the conversion process is completely independent from any external clock, so the sampling signal can be unevenly distributed in time, if only the distance between consecutive samples is longer than the conversion length. This also means that the ADC can be stopped and will not consume power (equivalently to power pulsing feature in Frond-end electronics (FE) circuit) just by absence of sampling signal. To obtain a maximum possible sampling rate, any inadvisable delay in the data flow has to be reduced as it is multiplied n times for n-bit ADC, increasing the total conversion length. For this reason, a dynamic logic was chosen for both internal registers and data flow control circuit. To make it even faster and more power efficient, the complete control logic layout was drawn and optimized manually without using any standard logic cells and automated tools.

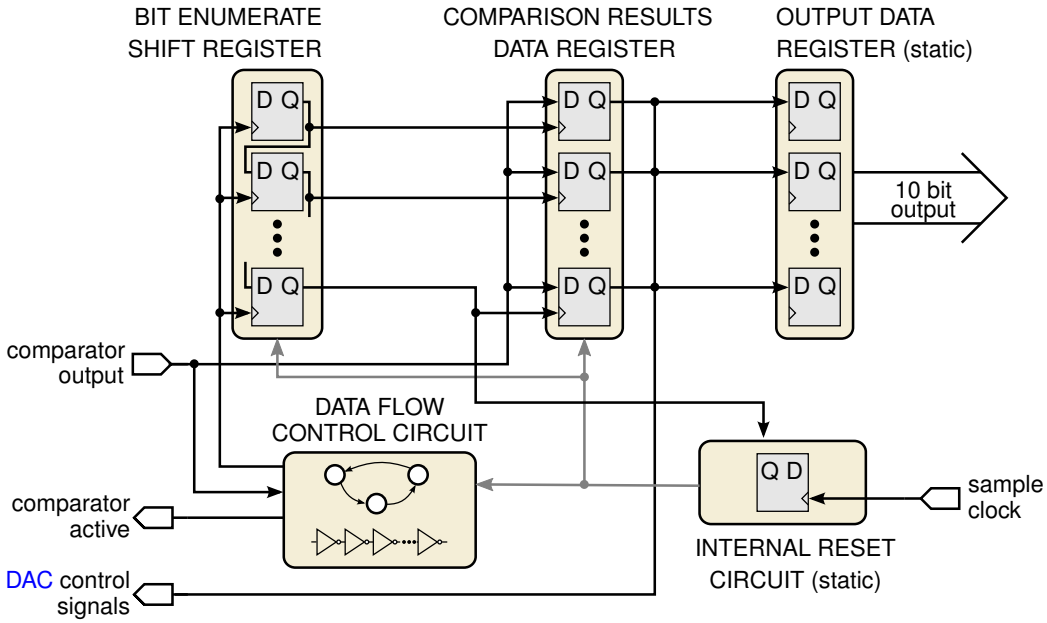


Figure 3.31: Diagram of the SAR ADC control logic.

The diagram of SAR ADC control logic is shown in Figure 3.31. It contains two registers based on dynamic flip-flops, one static register, a data flow control circuit (also dynamic) and an internal reset circuit (static). The dynamic flip-flops were used in two internal registers to achieve above 40 MHz sampling frequency. The first of these registers is a shift register which enumerates the bits during conversion while the second one stores the comparison result during the conversion. Since, as it was already mentioned, the ADC can be stopped at any time by absence of sampling signals, the

dynamic registers have to be reset by internal (static) circuit just after the conversion end to avoid a direct path current. To allow the subsequent logic to read safely the conversion result, without stringent time constraints, the data stored in the dynamic register during the conversion is moved to a static output register where it remains available until the next conversion ends.

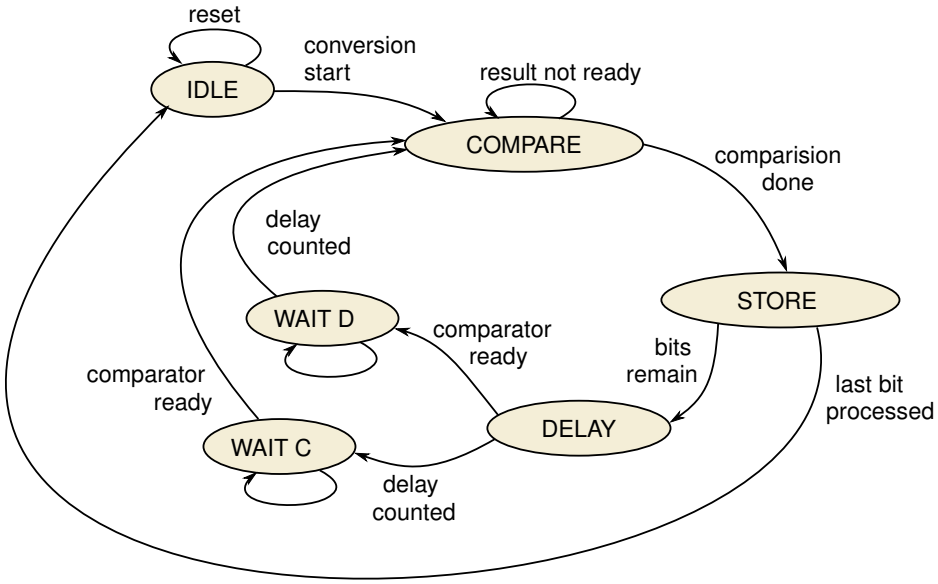


Figure 3.32: State diagram of the data flow FSM.

The data flow control circuit is realized as a Finite State Machine (FSM) with state diagram shown in Figure 3.32. On the beginning the ADC remains in self reset state. The conversion begins just after the sampling bootstrapped switches disconnect the inputs from the DAC, as it was shown for the MCS switching scheme, and the first comparison is performed. Since the outputs of the comparator $V_{out,p}$, $V_{out,n}$ are always in high state *11* in the reset phase and are equal *10* or *01* (according to the input voltages) when the comparison is completed, the distinction between the finished and ongoing comparison can be done by simple logical conjunction of the comparator outputs. In fact, since during the comparison the forbidden state *00* can appear on the comparator outputs, a logical Exclusive Alternative (XOR) is used to ensure that this incorrect state is not recognized as a valid result. The result is then stored in the internal data register and the completed bit is counted by the enumerating register. Assuming that one or more bits are still not processed, the two values from internal registers are then combined to create a proper control signals for the analogue reference switches in the DAC array. Simultaneously, the reset signal is sent to the comparator to prepare it for the next operation.

Since the capacitive DAC is recharged by a non-zero resistance analogue switches, its output voltage changes, in first approximation, as in a typical single pole R–C circuit. As the next comparison cannot be done until the DAC output voltage reaches the target value with sufficiently high precision, some fixed delay needs to be counted down before performing the next action. Otherwise the comparison result can be corrupted, what is called a settling error. This fixed delay is implemented as a chain of inverters with programmable length, which allows to control the delay via external command. In addition, since the recharged capacitances are decreasing for the subsequent bits during the conversion, the DAC output voltage settling time shortens. Thus a long fixed delay, suitable for the largest capacitances, results in unnecessary time waste during the last bits processing. To avoid this waste, the length of delay inverters chain is, independently from external settings, controlled by internal logic to obtain the optimal delay depending on the bit enumerating register.

This more sophisticated solution is implemented only in the first two prototypes, fabricated in CMOS 130 nm process A. In the third one (fabricated in CMOS 130 nm process B), a simplified delay circuit is used in order to ensure a proper operation of the FSM. However, the time waste during the last bits processing cannot be therefore avoided, and the maximum sampling frequency is limited in comparison to the first two prototypes.

Since the comparator requires non-negligible amount of time to accomplish the reset phase, two conditions need to be fulfilled: the comparator has to be ready for the next comparison and the fixed delay has to be counted down. Depending on the order of events, the FSM passes through the WAIT D state, if the comparator is ready before the delay was counted, or WAIT C state otherwise. When both conditions are met, the next comparison is performed, starting thereby the next bit processing. The complete cycle is repeated nine times while the last tenth cycle is interrupted just after the comparison since the bit enumerating register reaches its final value. After processing the last bit, the result is sent to the output data register, and the internal reset is sent to the control logic preparing the entire ADC for next conversion.

Clocking schemes

The main difference in control logic circuit between the first prototype fabricated in CMOS 130 nm process A and the last two (one in CMOS 130 nm process A, one in CMOS 130 nm process B) is the bootstrapped switches control. Since the duration of the sampling phase for given DAC input capacitance C_{in} (Table 3.6) has to be at least 4–5 ns, in the first prototype an additional dedicated circuit, based on CMOS thyristor concept [96] shown in Figure 3.33, was used. This circuit provides a positive pulse on the rising edge of the sampling signal with a duration time steered by external reference current $\mathtt{I}_{\mathrm{ref}}$. Therefore, the conversion starts after the sampling phase ends, on the falling edge of the bootstrap control signal, as shown in Figure 3.34a. Unfortunately, the pulse width provided by the delay thyristor circuit varies between the conversions due to a large jitter which significantly degrades the ADC performance, as it will be shown in the next section. To avoid this internally introduced jitter, an external sampling signal can define a conversion start moment, as it is shown in Figure 3.34b. In the two last prototypes, the sampling phase begins just after the conversion ends and continues until the next rising edge of the sampling signal. Since the sampling signal can be, in general, asynchronous, there is one disadvantage – if the gap between two consecutive samples is long, the charge stored on the bootstrapped switch capacitor $\mathtt{C}_{\mathrm{b}}$ (Figure 3.28) can be lost due

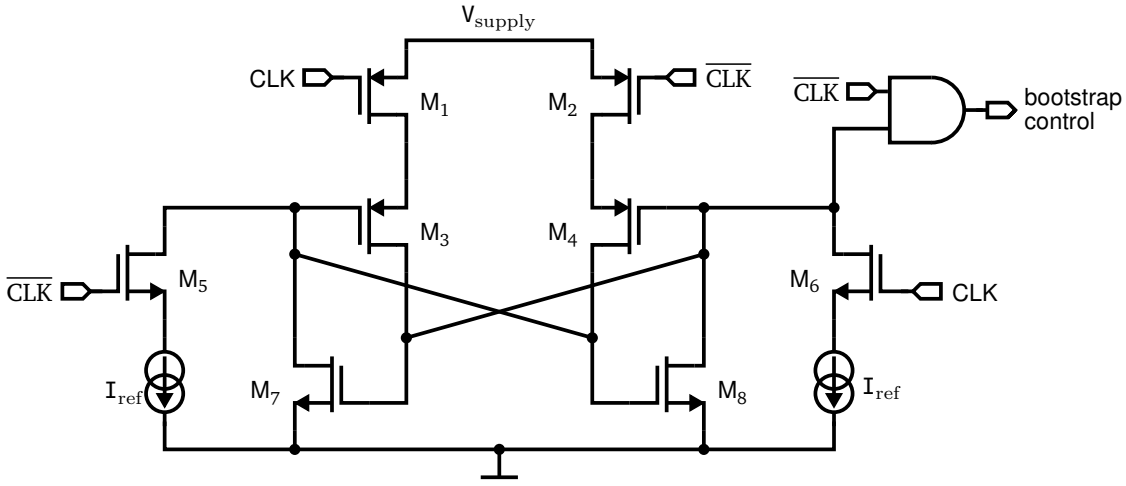


Figure 3.33: Simplified schematic of the delay thyristor circuit.

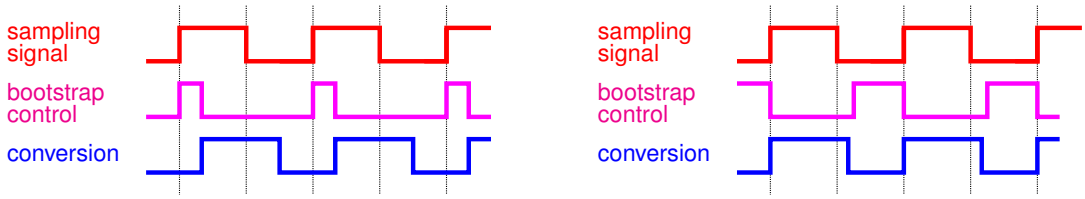


Figure 3.34: SAR clocking schemes.

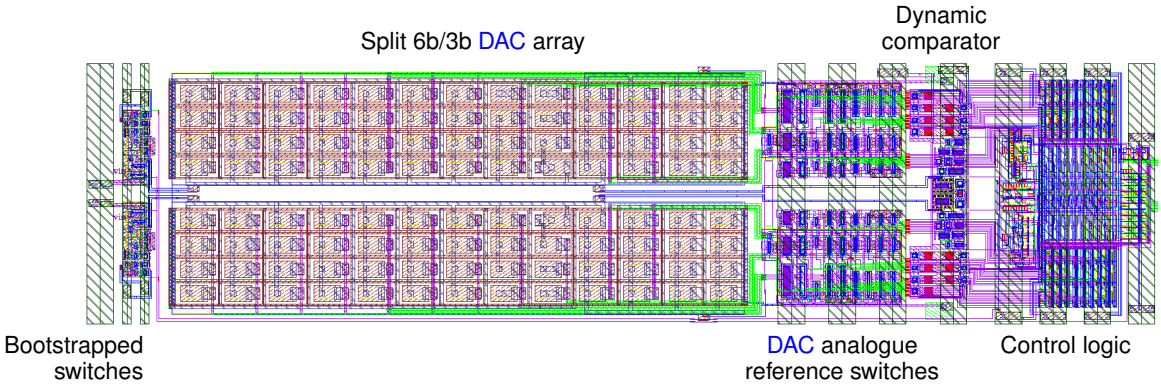
to leakage currents and the first sample can be corrupted due to incorrect bootstrap operation. For most applications this effects is not important.

Since the dynamic parameters of the first ADC prototype were degraded by the delay thyristor circuit, to determinate the ADC performance the measurements with this circuit disabled were also performed. In such operation, the sampling phase occupies half of the sampling clock period (due to internal ASIC logic limitations only a 50 % duty cycle clock could be provided) significantly reducing the maximum sampling frequency of the whole ADC. However, in this configuration the influence of the delay thyristor circuit could be neglected, showing the real ADC performance.

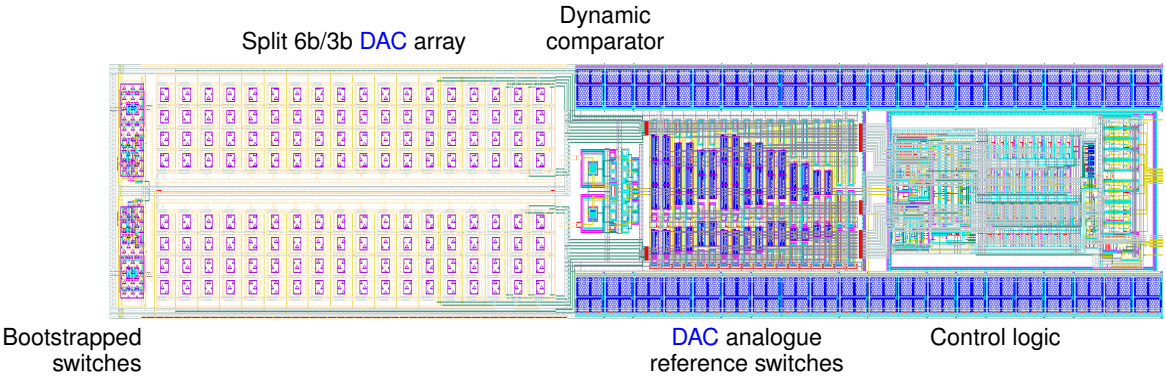
3.3.4 Measurements of prototype SAR ADCs

The three prototype SAR ADC ASICs were designed and fabricated in the CMOS 130 nm process A (two ASICs) and CMOS 130 nm process B (one ASIC) technologies. The layout of the SAR ADC channel in CMOS 130 nm process A is shown in Figure 3.35a, the channel layout in CMOS 130 nm process B in Figure 3.35b, and the fabricated prototypes are shown in Figure 3.35c. The area occupied by a single ADC channel is 146 μm × 600 μm in the CMOS 130 nm process A and 80 μm × 580 μm in the CMOS 130 nm process B.

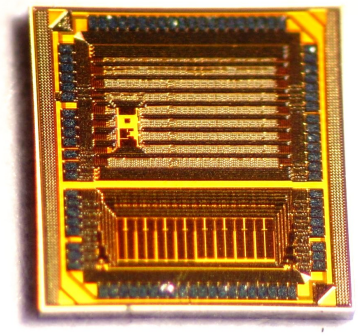
To verify the ADC performance a dedicated test setup, with DAQ based on a FPGA, was developed. The core of the setup is seen in Figure 3.36. The setup delivers the input signal and clock to the ASIC, and acquires the ADC output bits (ten parallel differential outputs) in the Scalable Low-Voltage Signaling (SLVS) standard. To reduce the development time, the test setup was based on a Digilent Genesys evaluation board containing the Virtex-5 FPGA with the Xilinx MicroBlaze soft core processor. A dedicated PCB, comprising the ADC ASIC and other required supporting circuitry, was designed as a mezzanine board. To ensure a low jitter of the sampling clock, as well as a clean input sinusoidal signal in the dynamic measurements, the Agilent 81150A generator was used as the source of clock and a fully differential input signal. In order to filter a high frequency noise a fully differential low pass filter was added between the generator and the ADC. The ADC ASIC uses four external voltages: analogue and digital power supplies which are set to 1.2 V, reference voltage V_{ref} which is also set to 1.2 V (ADC design was optimized to have V_{ref} equal to other power supplies), and common voltage V_{cm} set to 0.6 V. For the measurements all 1.2 V supply voltages (analogue, digital, V_{ref}) were connected together and taken from a single Low Drop-Out (LDO) regulator. The V_{cm} was obtained from the same source by voltage divider. The ADC input signal range depends on V_{ref} value, and its maximum amplitude is always slightly lower than V_{ref} because of parasitic capacitances in the DAC arrays.



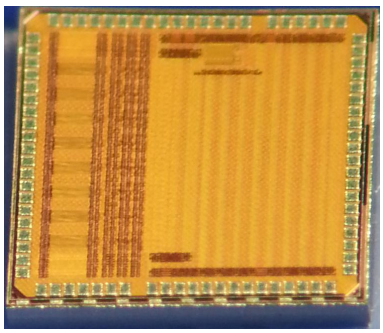
a) Layout in CMOS 130 nm process A technology



b) Layout in CMOS 130 nm process B technology



c) CMOS 130 nm process A prototype photograph



d) CMOS 130 nm process B prototype photograph

Figure 3.35: SAR ADC prototype ASIC.

Measurement theory

The ADC static performance is commonly quantified with the Integral Nonlinearity (INL) and the Differential Nonlinearity (DNL) measurements. Both parameters are obtained with the histogramming method [97].

To determine the dynamic parameters of an ADC, such as noise performance, dynamic linearity, harmonic distortions and influence of internally introduced jitter, the dynamic metrics are calculated. Since the result $y(t)$ of the sampling process can be described in time domain as a product of the

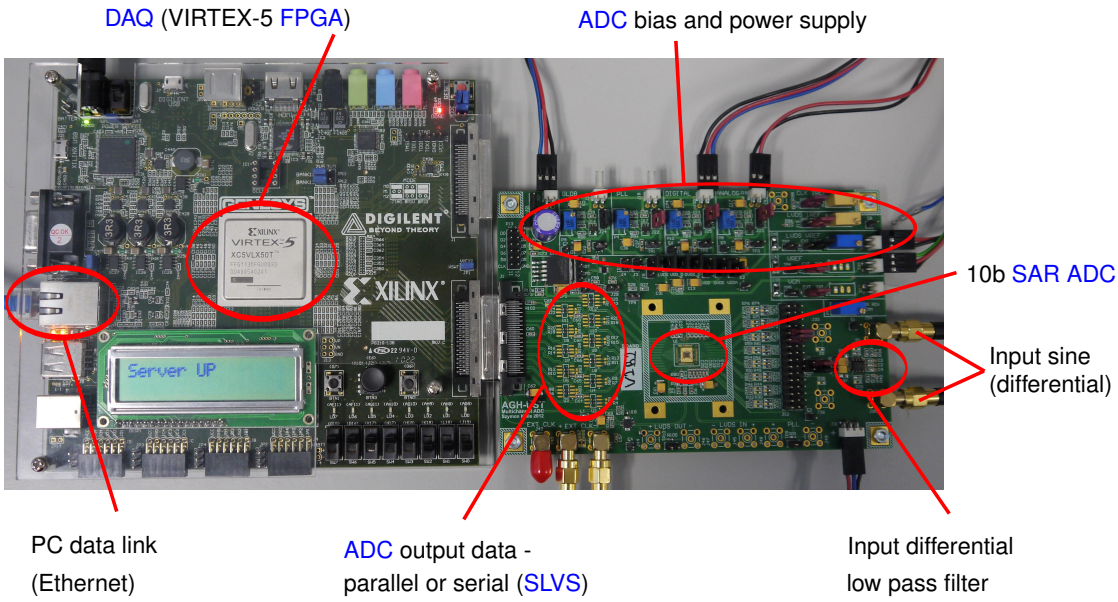


Figure 3.36: Main components of the ADC test setup: FPGA based evaluation board (left), dedicated PCB with the ADC ASIC (right).

input signal $x(t)$ and the sampling unit impulse signal $\delta_u(t)$ as follows [98]:

$$y(t)=\sum_{n=-\infty}^{\infty} x(t)\cdot\delta_u(t-nT_s)\,, \tag{3.41}$$

where T_s is sampling period, the Fourier transform of the ADC output data is given as the convolution of transforms of the input signal and the ADC transfer function T_{ADC}:

$$\mathfrak{F}[y(t)]=\mathfrak{F}[x(t)\cdot T_{ADC}]=\mathfrak{F}[x(t)]\otimes\mathfrak{F}[T_{ADC}]\,. \tag{3.42}$$

Since the ADC data are defined in discrete time domain, the Discrete Fourier Transform (DFT) should be used in equation 3.42 instead of continuous Fourier transform. The convolution given by 3.42 can be easily resolved if a single tone signal is used. Since the base frequency f_{base} of N samples length DFT with sampling frequency $f_s=1/T_s$ is defined as:

$$f_{base}=\frac{f_s}{N}\,, \tag{3.43}$$

the DFT of pure sine signal with frequency equal to one of the fundamental frequencies $k\cdot f_{base}$, where $k\in(0,N/2)$, is a simple Kronecker delta δ_k:

$$\mathfrak{F}[x(t)]=\mathfrak{F}[\sin(k\cdot f_{base})]=\delta_k;\qquad k\in(0,N/2)\,. \tag{3.44}$$

Based on the discrete convolution of a finite sample series definition:

$$(f\otimes g)[n]=\sum_{m=0}^{N} f[m]g[n-m]=\sum_{m=0}^{N} f[n-m]g[m]\,, \tag{3.45}$$

and Kronecker delta property:

$$\sum_{m=0}^{N}\delta_k f[m]\equiv f[k]\qquad \forall_{k\in[0,N]}\,, \tag{3.46}$$

equation 3.42 for input signal defined as 3.44 can be rewritten as follow:

$$\mathfrak{F}[y(t)]=\mathfrak{F}[x(t)\cdot T_{ADC}]=\mathfrak{F}[sin(k\cdot f_{base})\cdot T_{ADC}]=$$
$$=\mathfrak{F}[sin(k\cdot f_{base})]\otimes\mathfrak{F}[T_{ADC}]=\delta_k\otimes\mathfrak{F}[T_{ADC}]=\mathfrak{F}[T_{ADC}]\ . \tag{3.47}$$

Therefore, by applying a pure sine function as the ADC input signal and calculating a DFT from the N output code series, the Fourier transform of the ADC transfer function can be obtained. An example spectrum acquired from this type of measurement, for 10 MHz sampling frequency and input signal near to the Nyquist frequency (<5 MHz), is presented in Figure 3.37. The nonlinearity of ADC reveals as harmonic distortions of the input signal, i.e. as consecutive integral multiples of the signal frequency f_{sig}, while the noise level introduced by the ADC circuitry (both, quantization and real) can be reconstructed from the DFT spectrum with removed input signal harmonic frequencies. According to the standard [97], the first ten input signal harmonics should be determined. These harmonics are highlighted in example spectrum shown in Figure 3.37. A five dynamic metrics, a Total Harmonic Distortion (THD), a Signal to Non Harmonic Ratio (SNHR), a Spurious Free Dynamic Range (SFDR), a Signal to Noise and Distortion Ratio (SINAD), and an Effective Number Of Bits (ENOB) are defined by the standard [97] describing, respectively, the signal degradation introduced by harmonic distortions, the noise, the highest spurious signal, the noise and harmonic distortion, and the overall ADC quality. For an ideal 10-bit ADC, the ENOB is equal to 10 while the corresponding SINAD equals 61.96 dB.

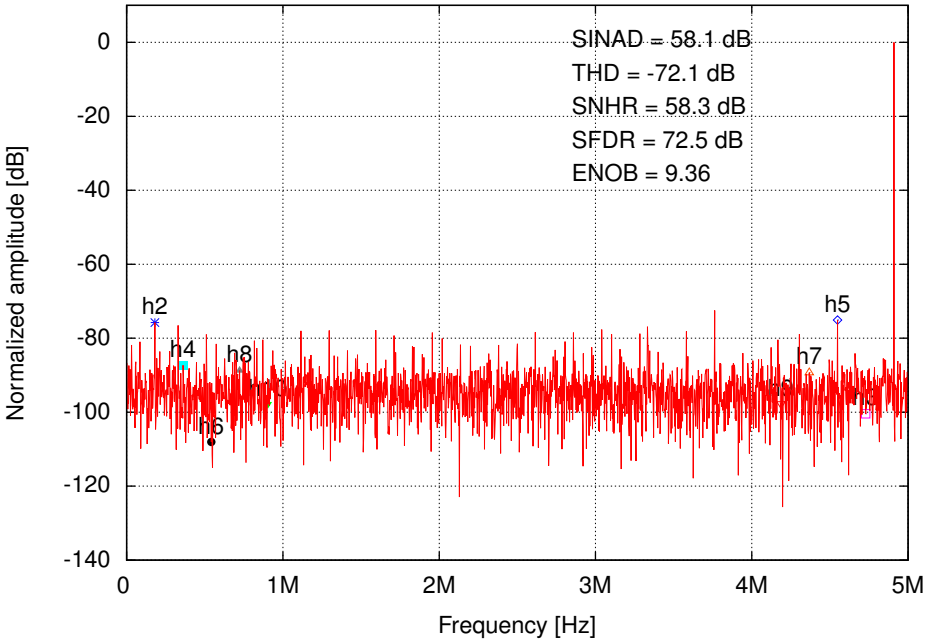


Figure 3.37: Example DFT spectrum for 10-bit ADC.

First ADC prototype in CMOS 130 nm process A technology

The transfer function of the first ADC prototype manufactured in CMOS 130 nm process A technology, called hereinafter ADC_A_V1, is shown in Figure 3.38, while the corresponding static parameters (INL and DNL) in Figure 3.39. Since the transfer function of all prototypes is very similar and does

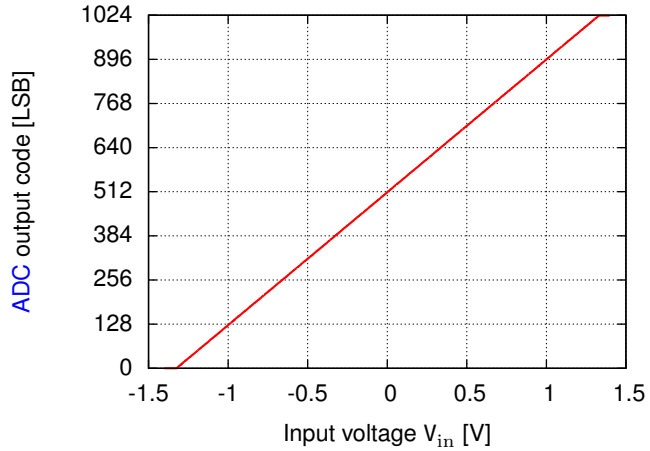


Figure 3.38: Transfer function of the ADC_A_V1 prototype at 10 MHz sampling frequency.

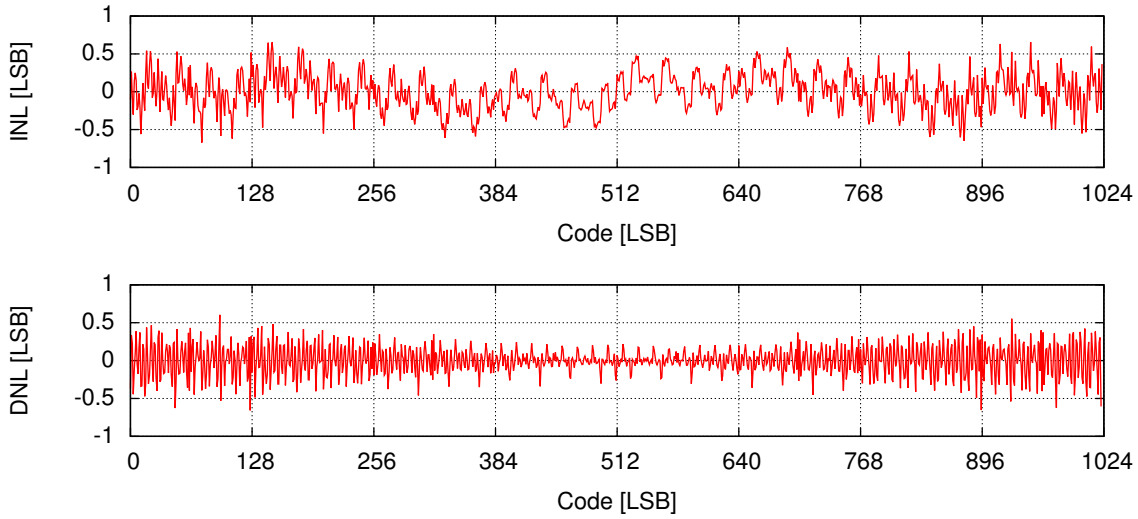


Figure 3.39: Static measurement result of the ADC_A_V1 prototype at 10 MHz sampling frequency.

not show the detailed performance, it will not be shown for the remaining prototypes. The static performance of the ADC_A_V1 is quite satisfactory, since the DNL remains in range (-0.684,0.741) LSB while the INL does not exceed (-0.787,0.746) LSB. A static ENOB corresponding to this measurement is 9.64 LSB.

As it was discussed during the ADC design (see Section 3.3.3), the settling error reduces the overall ADC performance. In order to avoid it, a proper settling delay has to be set. The static measurements results shown above were obtained with the settling delay set to 2. To determine the influence of settling error, static parameters were measured for four different settling delays. The detailed results are presented in Appendix B. Here it may be only concluded that a significant settling error can be clearly seen for settling delay lower than 2, while the difference in performance between settling delay equal 2 and 3 is negligible.

Dependence of static parameters on sampling frequency is shown Figure 3.40. This measurement was done with delay thyristor circuit enabled, since its jitter does not affect static measurements. Therefore, the sampling frequency above 40 MHz was possible to obtain without any signif-

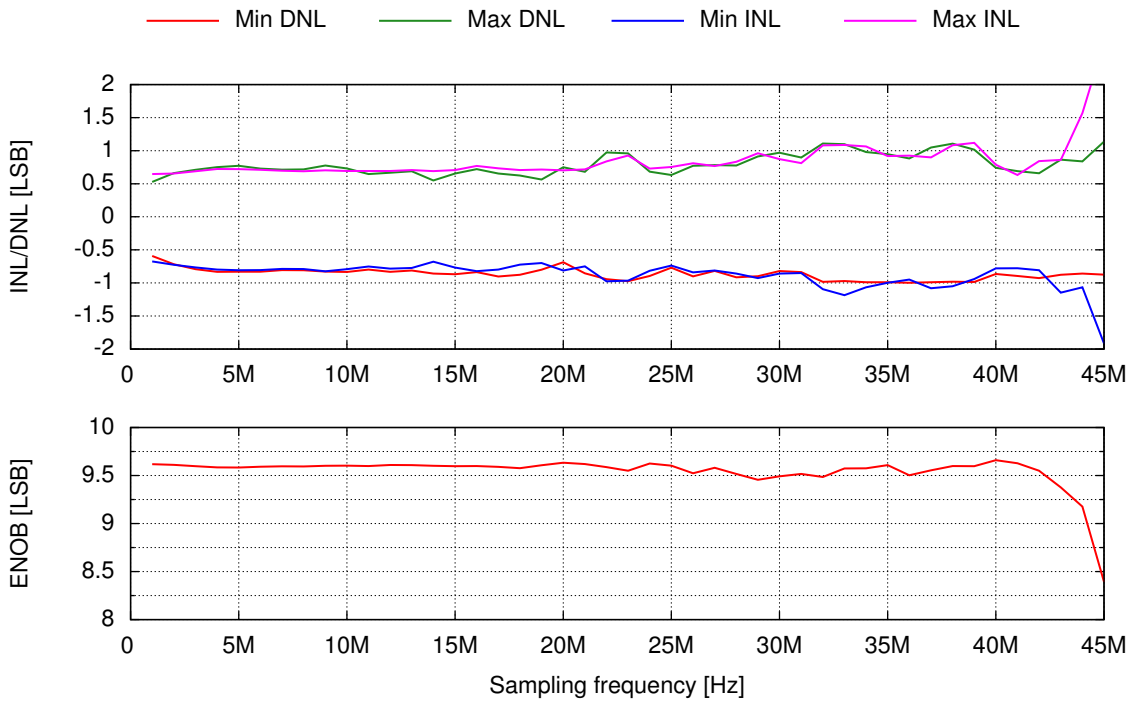


Figure 3.40: Static measurement result of the ADC_A_V1 prototype versus sampling frequency with enabled delay thyristor circuit.

icant performance degradation. Above 42 MHz the parameters begin to degrade indicating that the maximum sampling frequency was exceeded. A similar measurement with disabled delay thyristor was also performed and the results are presented in Appendix B. Since in this configuration the ADC may use only half of the clock period for the conversion, the maximum sampling frequency should be significantly lower. The INL, DNL results presented in Appendix B are quantitatively very similar to the ones shown in Figure 3.40 but the maximum sampling frequency is limited to around 25 MHz.

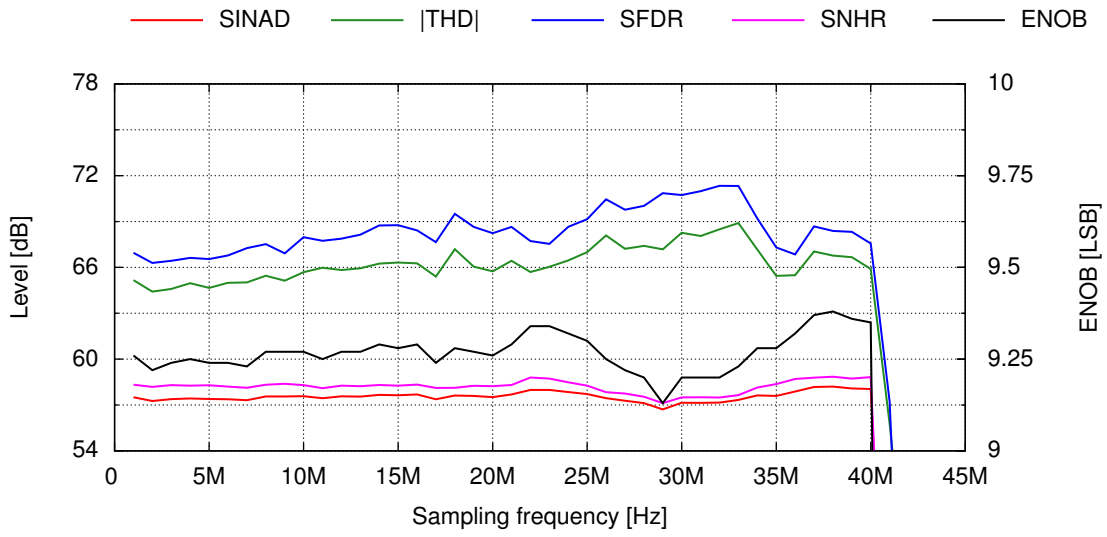


Figure 3.41: Dynamic measurement result of the ADC_A_V1 prototype versus sampling frequency at 0.2 Nyquist input sine frequency with enabled delay thyristor circuit.

To determinate the dynamic performance of the ADC_A_V1, the dynamic measurements for various sampling frequencies, with input sine frequency fixed at 0.2 Nyquist, were done and their results are shown in Figure 3.41. Up to 40 MHz sampling frequency the ENOB above 9.2 LSB was obtained and, comparing to the static measurements (Figure 3.40), a decrease of 0.3 LSB can be found. Since the jitter influence increases with growing input signal frequency, the dynamic parameters were measured at maximum sampling frequency of 40 MHz for different input frequencies. It was found that the ENOB degrades with a growing input frequency. The detailed results are presented in Appendix B.

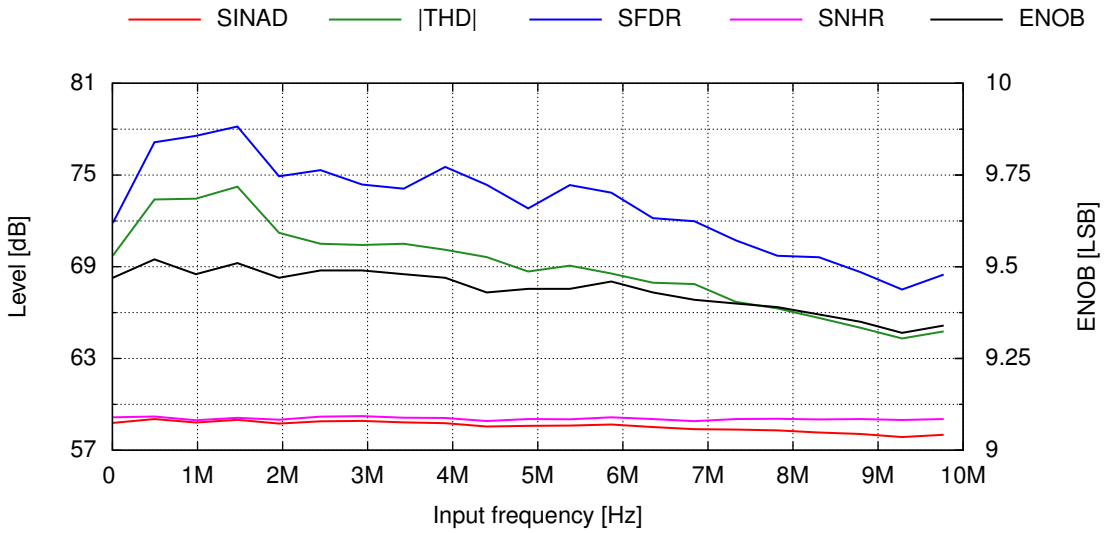


Figure 3.42: Dynamic measurement result of the ADC_A_V1 prototype versus input frequency at 20 MHz sampling frequency with disabled delay thyristor circuit.

Since the jitter introduced by the delay thyristor circuit was considered the main source of the dynamic performance loss, a similar measurements, with this circuit disabled, were done and are presented in Appendix B. Alike the static measurements, the maximum sampling frequency was also limited in this case, but the expected ENOB improvement, up to 9.5 LSB, was found. The dynamic parameters were measured also in function of input frequency at 20 MHz sampling frequency. The

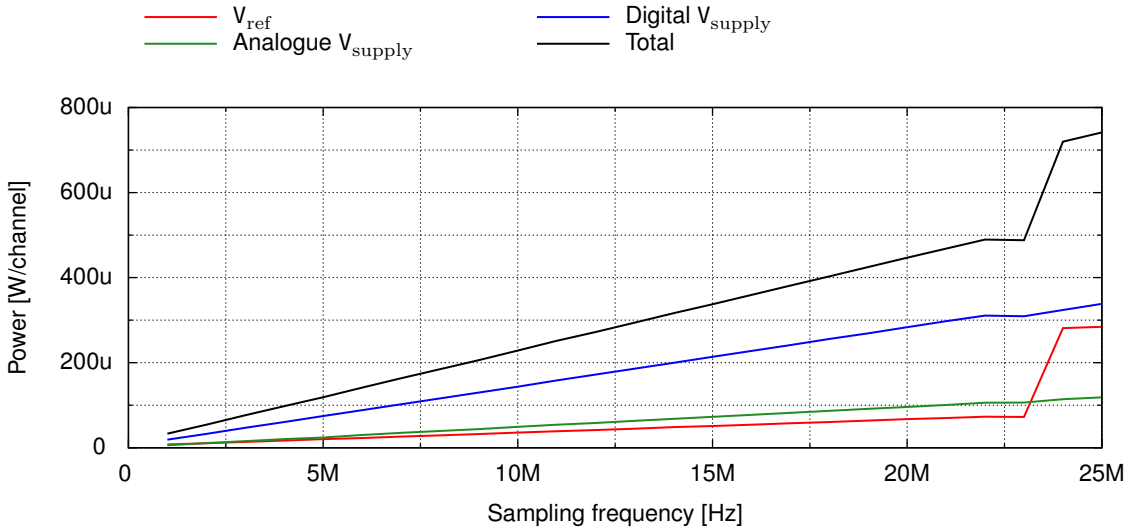


Figure 3.43: ADC_A_V1 prototype with disabled delay thyristor circuit power consumption.

results are shown in Figure 3.42. Up to Nyquist frequency the ENOB above 9.3 LSB was obtained without significant parameters degradation.

The ADC_A_V1 power consumption with disabled delay thyristor circuit is presented in Figure 3.43. The power consumption scales linearly with sampling frequency up to its maximum value of 21 MHz where the reference voltage V_{ref} power consumption increases rapidly due to overlapping conversions. At 20 MHz sampling frequency the ADC consumes 0.45 mW.

Second ADC prototype in CMOS 130 nm process A technology

The static measurements results of the second ADC prototype, fabricated also in CMOS 130 nm process A technology and called hereinafter ADC_A_V2, are shown in Figure 3.44. The performance is very similar to the previous version, since the static ENOB is equal to 9.5 while the DNL and INL remain in ranges (-0.797,0.563) LSB and (-0.553,0.623) LSB respectively.

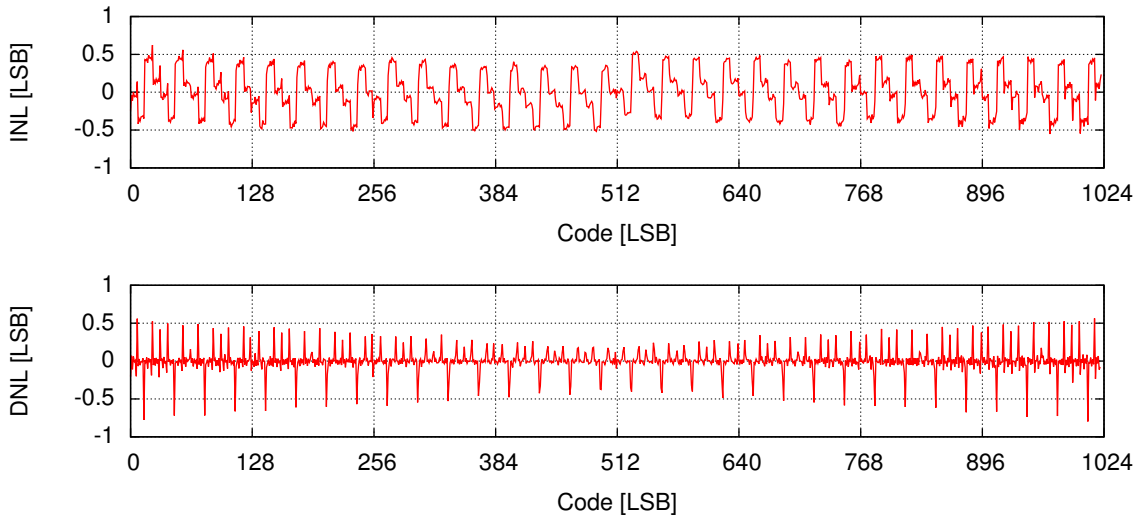


Figure 3.44: Static measurement result of the ADC_A_V2 prototype at 10 MHz sampling frequency.

To ensure a proper working conditions, the settling delay was extended in the ADC_A_V2 prototype, even at the cost of reduced maximum sampling frequency. The settling delay equal 4 was found as optimal for overall ADC prototype and was used during all measurements performed for ADC_A_V2. The detailed results, presenting the influence of settling error on the static parameters, are presented in Appendix B.

The maximum sampling frequency of the ADC_A_V2 is around 45 MHz, as can be seen from the measurements results shown in Figure 3.45. However, above 30 MHz sampling frequency the INL and DNL slightly exceeds the boundary value of 1 LSB. Despite this, the static ENOB above 9.4 LSB was obtained in the entire sampling frequency range up to 45 MHz. The static parameters obtained at 40 MHz sampling frequency are shown in Figure 3.46. Since the settling delay was extended, the whole conversion length also increased. It can be seen from Figure 3.34b, that the duration of sampling phase decreases with increasing sampling frequency at constant conversion length, leading to degradation of the ADC performance above 30 MHz.

The dynamic parameters versus sampling frequency at 0.2 Nyquist input sine frequency are shown in Figure 3.47. Up to 30 MHz sampling frequency the ENOB above 9.3 LSB was obtained,

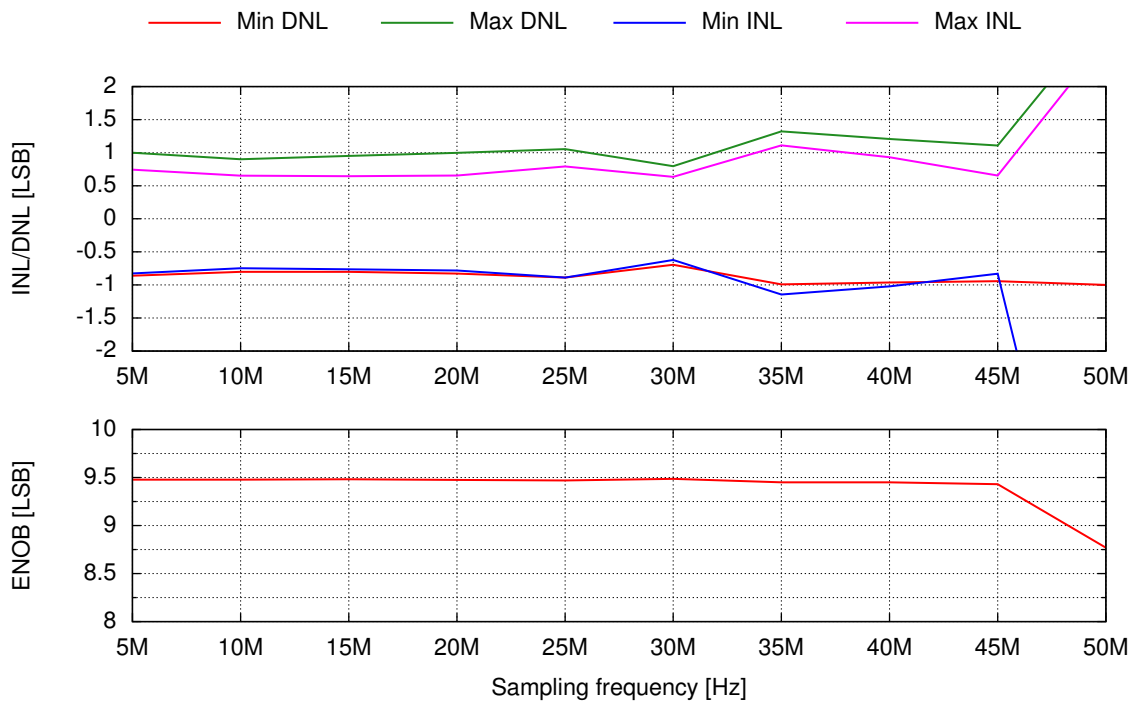


Figure 3.45: Static measurement result of the ADC_A_V2 prototype versus sampling frequency.

only 0.1 LSB lower than the one achieved from the static measurements (Figure 3.45). For higher sampling frequencies the ENOB degrades significantly, reaching below 7 LSB at the 40 MHz sampling frequency. This degradation results from the insufficient sampling phase length, as it was already described.

The dynamic parameters of the ADC_A_V2 were measured also for various input sine frequencies at fixed 30 MHz sampling frequency. The results are presented in Figure 3.48. The ENOB above 9.2 LSB was obtained up to the Nyquist frequency. A minor ENOB dependence on the input frequency

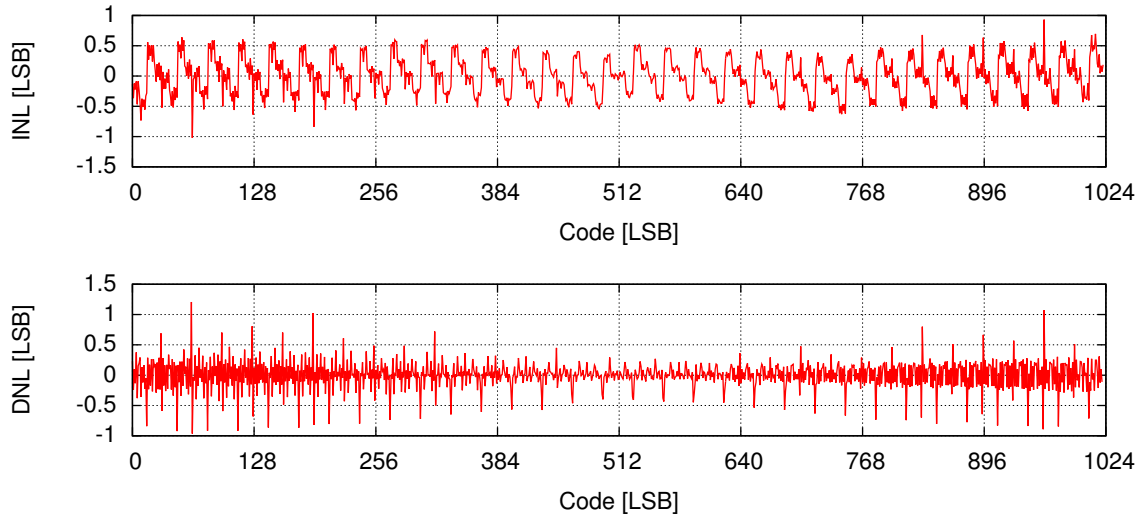


Figure 3.46: Static measurement result of the ADC_A_V2 prototype at 40 MHz sampling frequency.

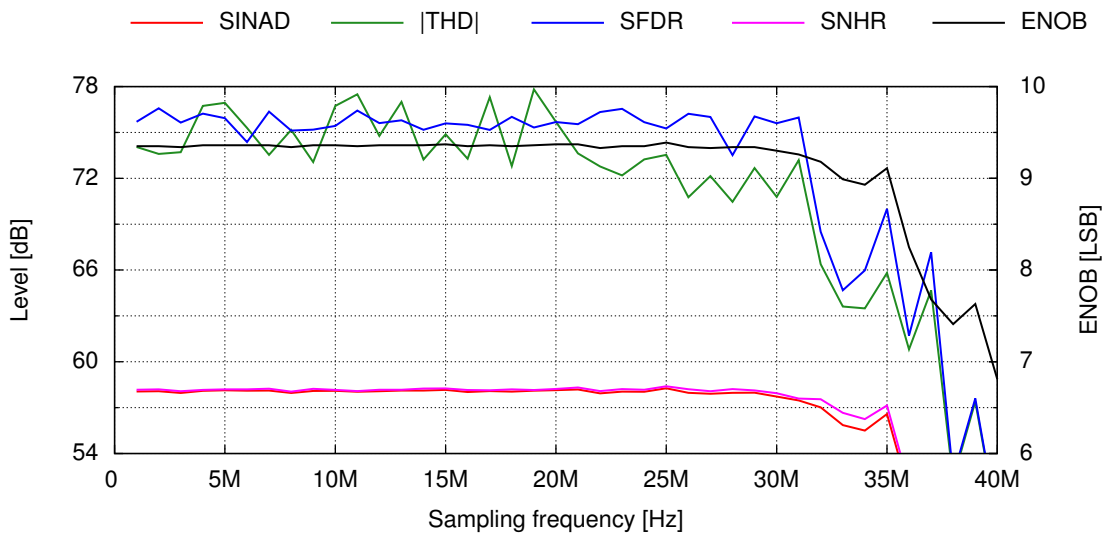


Figure 3.47: Dynamic measurement result of the ADC_A_V2 prototype versus sampling frequency at 0.2 Nyquist input sine frequency.

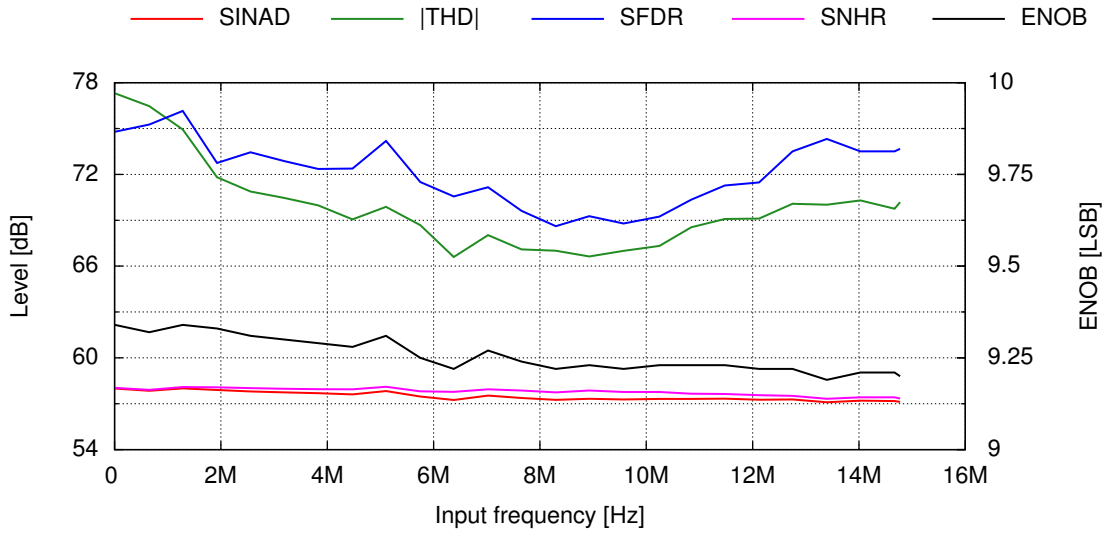


Figure 3.48: Dynamic measurement result of the ADC_A_V2 prototype versus input frequency at 30 MHz sampling frequency.

can be found for ADC_A_V2, since the ENOB decreases very little from 9.3 LSB to 9.2 LSB with increasing input frequency.

The ADC_A_V2 power power consumption is presented in Figure 3.49. Above 1 MHz of sampling frequency power consumption scales linearly with sampling frequency. At 40 MHz the ADC consumes around 0.85 mW while at 20 MHz power consumption drops to 0.45 mW, the same value as for the ADC_A_V1 prototype.

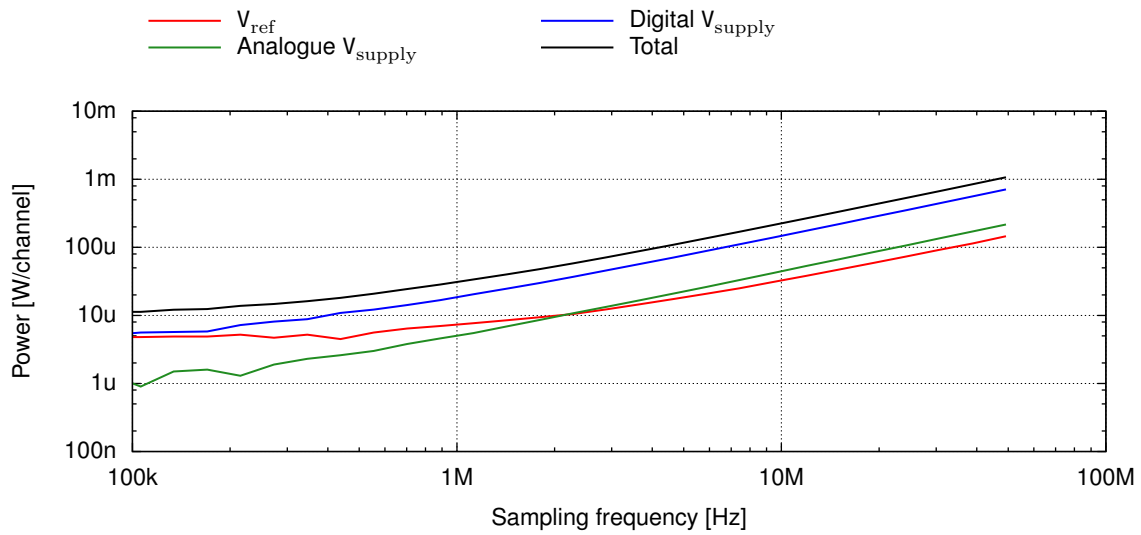


Figure 3.49: ADC_A_V2 prototype power consumption versus sampling frequency.

First ADC prototype in CMOS 130 nm process B technology

The same set of measurements was performed for the first ADC prototype fabricated in CMOS 130 nm process B technology, called hereinafter ADC_B_V1. The exemplary results of static measurements at 10 MHz sampling frequency, with the longest settling delay, are presented in Figure 3.50. The performance of ADC_B_V1 is excellent with static ENOB equal to 9.92 LSB and the DNL and INL within (-0.206,0.192) LSB and (-0.267,0.284) LSB respectively. The achieved results indicate a very good capacitance matching in the CMOS 130 nm process B technology, since the minimum available value of 26.2 fF was used as the unit capacitance (see Section 3.3.2).

Analogously to the previous prototypes, the settling delay circuit was implemented in the control logic. However, to ensure the proper operation of control logic, a simplified implementation was

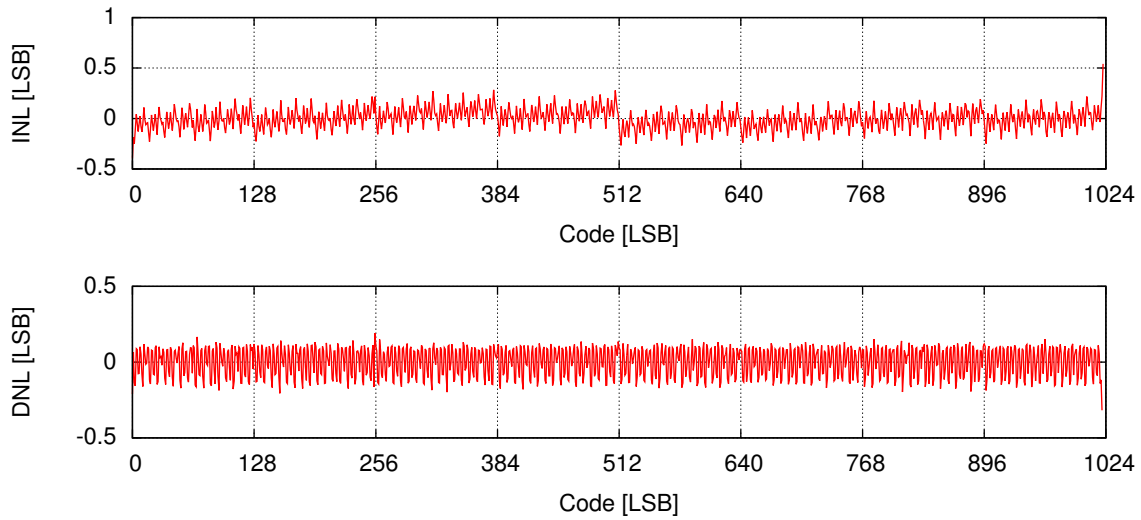


Figure 3.50: Static measurement result of the ADC_B_V1 prototype at 10 MHz sampling frequency for the longest settling delay.

chosen for the ADC_B_V1 prototype. As it was described in Section 3.3.3, the same settling delay is utilized for all processed bits in this prototype. Since the MSB capacitance is the largest one in the whole DAC, its settling time is the longest. Therefore, to obtain the performance presented in Figure 3.50, the longest settling delay, equal 7, has to be set in order to avoid the error during the MSB switching. However, this leads to the unnecessary time waste during the last bits processing, limiting the maximum sampling frequency to around 30 MHz.

In order to increase the maximum sampling frequency, the settling delay can be shorten. Although the settling error cannot be avoided in this case, a trade off between sampling rate and the ADC performance can be found. As an example, the static characteristics, obtained at 10 MHz sampling frequency for settling delay equal 5, are presented in Figure 3.51. As can be seen, the extreme value of DNL, -1 LSB, occurs only for two codes (256 and 768), corresponding to the MSB switching. The characteristics for all remaining codes are quantitatively similar to the one presented in Figure 3.50 obtained for the longest settling delay. This indicates, that the settling error occurs only for the MSB switching, and the settling delay equal 5 is sufficient for all other switchings. Since the static ENOB corresponding to the results presented in Figure 3.51 is still very high (above 9.8 LSB), the influence of two missing codes onto the overall ADC performance, alongside a perfectly linear 1022 other ones, is negligible and a settling delay equal 5 was used in the following measurements in order to achieve 40 MHz sampling frequency. The detailed results of the static parameters for various settling delays are presented in Appendix B.

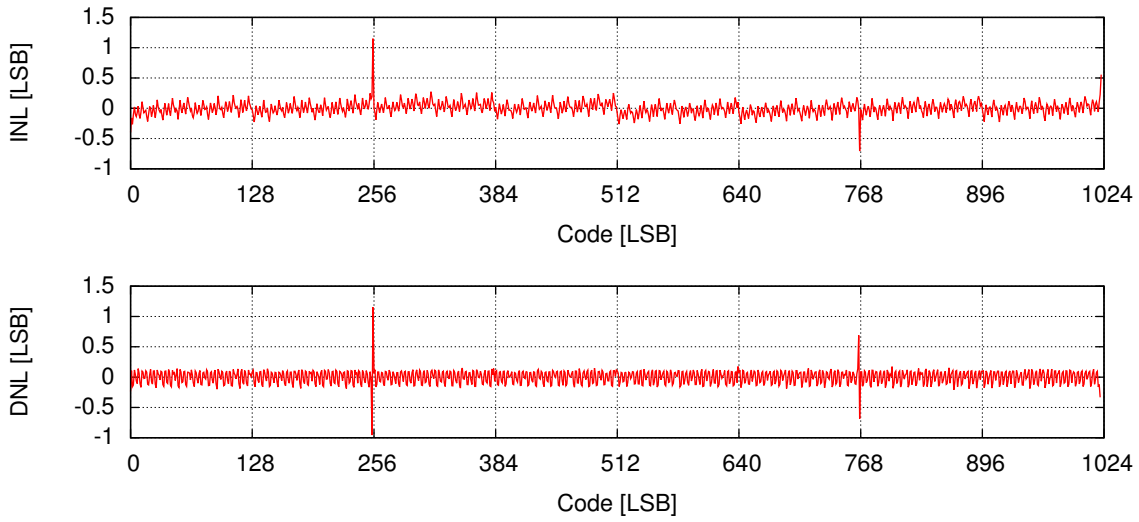


Figure 3.51: Static measurement result of the ADC_B_V1 prototype at 10 MHz sampling frequency for the settling delay equal 5.

The ADC_B_V1 dynamic parameters versus sampling frequency at 0.2 Nyquist input sine frequency are presented in Figure 3.52. The dynamic ENOB remains between 9.4 and 9.5 LSB up to 37 MHz sampling frequency, and slightly decreases to 9.3 LSB with sampling frequency reaching the maximum value of 40 MHz. Analogously to the previous prototypes, this effect is related to the shortening of sampling phase length with the increasing sampling frequency. However, contrary to the previous results (Figures 3.41 and 3.47), the ENOB degradation at 40 MHz sampling frequency is negligible and so the performance of the ADC_B_V1 is the best of all three prototypes.

The results of dynamic parameters measurements for various input sine frequencies at 20 MHz sampling frequency are presented in Figure 3.53. The ENOB varies between 9.4 and 9.5 LSB in the

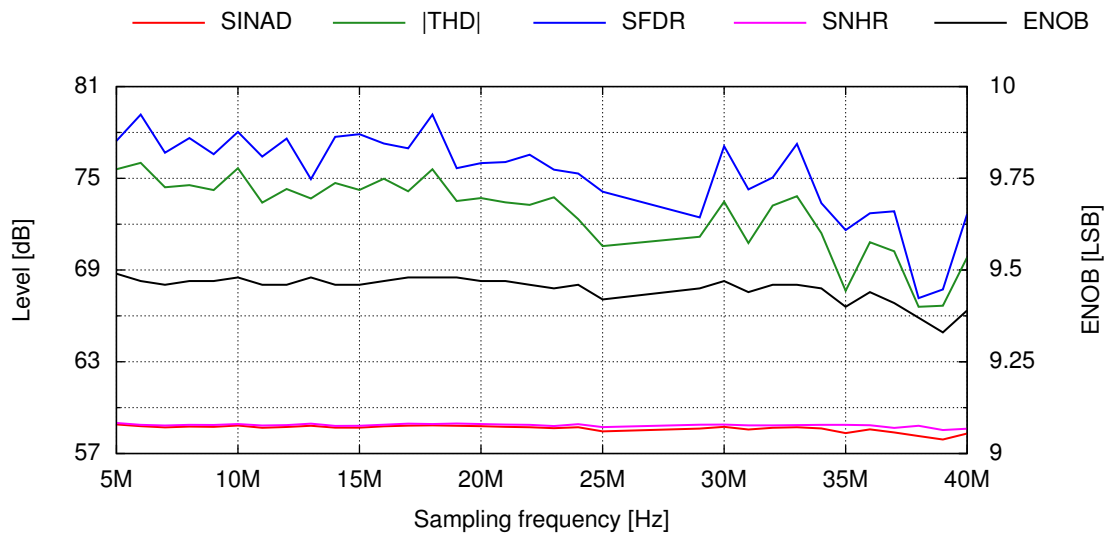


Figure 3.52: Dynamic measurement result of the ADC_B_V1prototype versus sampling frequency at 0.2 Nyquist input sine frequency.

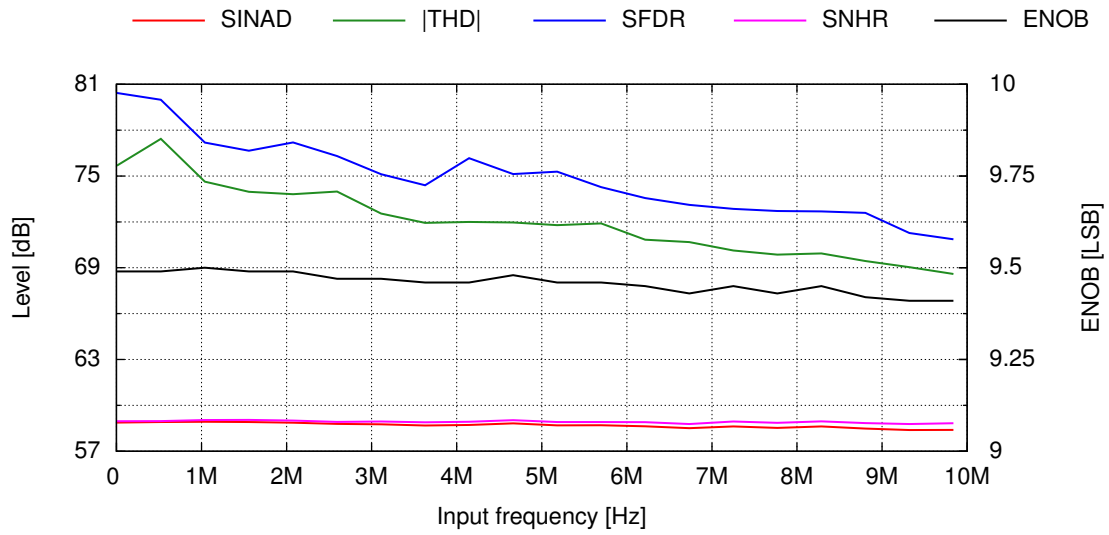


Figure 3.53: Dynamic measurement result of the ADC_B_V1 prototype versus input frequency at 20 MHz sampling frequency.

whole range of input sine frequency, indicating the excellent ADC dynamic performance. A complementary measurements, performed at 40 MHz sampling frequency, reveal however a significant degradation of dynamic parameters near the Nyquist frequency, caused by too short sampling phase. This degradation can be easily recovered by implementation of more sophisticated settling delay circuit, similar to the one used in ADC_A_V1 and ADC_A_V2 prototypes. Such improvement will shorten the overall conversion length (simultaneously without introducing the missing codes at MSB capacitance switching), providing effectively longer sampling phase, which will allow to restore the ENOB near the Nyquist frequency at the fastest sampling. The detailed ADC performance for various input sine frequencies at 40 MHz sampling frequency is presented in Appendix B.

The ADC_B_V1 power power consumption is presented in Figure 3.54. As can be seen, the reference voltage V_{ref} power consumption does not scale linearly with the sampling frequency, remaining

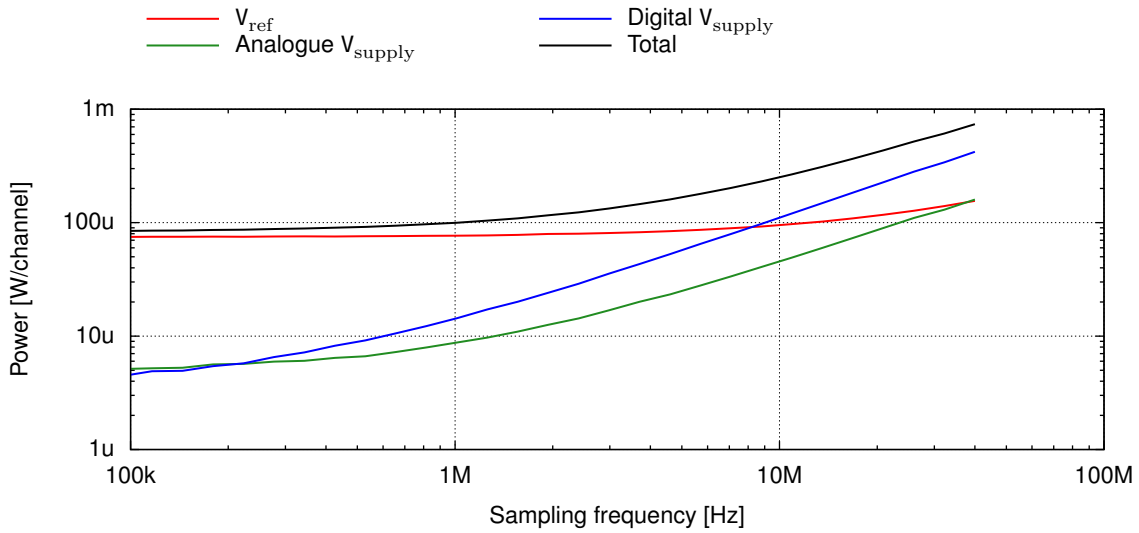


Figure 3.54: ADC_B_V1 prototype power consumption versus sampling frequency.

almost constant up to 10 MHz. This permanent consumption, of around 80 μW per channel, provides a significant contribution to the total power consumption at higher frequencies, and dominates below 10 MHz of sampling frequency. This power consumption is most likely caused by the leakage current of the decoupling structures of reference voltage V_{ref}, provided by the CMOS 130 nm process B technology. This issue can be fixed in the future prototype by designing the decoupling devices with significantly lower leakage current. Despite the constant leakage on the reference voltage, the ADC_B_V1 power consumption at 40 MHz sampling frequency is around 0.74 mW per channel (0.68 mW per channel without the leakage), and is the smallest of all three prototypes.

Summary of ADC measurements

With the goal of developing a SoC readout ASIC for the LumiCal detector, a three prototypes of 10-bit SAR ADC were designed and fabricated. The performance of two CMOS 130 nm technologies was explored by these designs. All three ADC prototypes show a good performance, with the dynamic and static ENOBs above 9 LSB in almost all conditions. The excellent results achieved for the ADC_B_V1 place it within the best currently published designs. Although some minor issues still have to be revised, the ADC_B_V1 prototype is a very good candidate for the SoC readout ASIC with the power consumption of around 0.74 mW per channel at 40 MHz of sampling frequency, and the design ready for multichannel integration. The ADC power consumption, what may be surprising, is in fact smaller than the front-end electronics power consumption, allowing to integrate the 10-bit ADC in each channel without significant increase of the total power consumption. This was impossible in the past for older technologies and less efficient architectures. In addition, due to the asynchronous logic design, all three prototypes provide directly the power pulsing functionality, required by the future linear collider.

Summary

The development of the Luminosity Calorimeter (LumiCal) for future linear collider was the main objective of this dissertation. The two main components of this development can be highlighted:

– the experimental verification of correct operation of multi-plane LumiCal prototype, covering all stages of HEP detector development – starting from construction, assembly and tests, through the execution of the testbeam, finishing with the analysis of the collected data;

– development of the second generation of dedicated readout ASICs, in order to improve the key parameters, like power consumption and radiation hardness.

The main objectives of this dissertation have been fully attained. The performance of the multi-plane LumiCal prototype was verified experimentally during the testbeam. Author has been actively involved in both, the extensive preparation of the multi-plane prototype and the execution of the testbeam. The analysis of the collected data allowed to reconstruct the shower development proving the LumiCal concept. The second generation of the front-end and ADC prototype ASICs were developed, fabricated and tested, with results confirming the correct, complying with the specification, performance. The major conducted activities with the author's contribution are listed below:

- **LumiCal multi-plane prototype preparation**

  In order to perform, for the first time, the testbeam of multi-plane LumiCal prototype, a precise mechanical structure was developed to meet the demanding geometrical requirements (see Section 2.1.1). The existing readout boards, used successfully in single-plane configuration in a number of testbeams [66, 48], were optimized and tuned in order to enable the multi-plane operation. The complete multi-plane prototype was integrated, assembled and extensively tested in the laboratory. The improvements of the mechanical structure and readout boards, requiring few iterative integration and testing steps, allowed to achieve fully functional multi-plane LumiCal prototype.

- **Testbeam of the multi-plane prototype**

  After the initial preparatory work, the LumiCal multi-plane prototype was successfully used, for the first time, in the testbeam performed in October 2014 at T9 east area of PS accelerator at CERN. The complete system (mechanical structure and readout boards) fulfilled the expectations allowing to collect the data in three different geometrical configurations (see Section 2.1.1). The prepared readout boards and DAQ provided sufficient amount of experimental data, enabling the shower development analysis.

- **Testbeam data analysis software**

  In order to analyze the data collected during the testbeam, a dedicated software was developed. The initial processing of the data from two detectors included in the testbeam instrumentation – the LumiCal and the telescope (detector recording particle tracks, supporting the measure-

ments), was implemented as discussed in Section 2.2. The efficiency of telescope alignment and tracking procedures was investigated (see Section 2.2.1), and the obtained results enabled the verification of position reconstruction (see Section 2.3.3). The initial processing of the LumiCal data, the common mode subtraction procedure in particular, was discussed and the proper implementation was chosen based on the investigated performance of various configurations (see Section 2.2.2).

- **Amplitude reconstruction by deconvolution**

  In order to enable a fast and efficient reconstruction of the deposited charge, an innovative method, based on advanced Digital Signal Processing (DSP), was implemented. Aside some other benefits, i.e. pile-up immunity improvement, the deconvolution enable a good reconstruction of the front-end pulse amplitude even at low SNR in a given system. The complete procedure for the LumiCal detector was discussed together with its performance studies (see Section 2.2.2).

- **Shower development**

  Based on the prepared software, the LumiCal capability for the reconstruction of electromagnetic shower development was investigated. Although not all aspects of the detector geometry were included in the MC simulation setup, the currently available MC results are quantitatively in good agreement with the achieved experimental results. The shower development was fully reconstructed, as shown in Section 2.3.4.

- **Front-end prototype**

  In order develop the second generation of dedicated readout ASICs for the LumiCal, two modern deep sub-micron CMOS technologies were investigated (see Section 3.1). Based on these considerations, a new front-end electronics was designed, fabricated and tested (see Section 3.2). The achieved results indicates that the prototype is functional and fulfills the requirements. The major improvement in power consumption, comparing to the existing prototype, was achieved. The results were already published [99].

- **ADC prototype**

  To the author knowledge, up to now no ultra-low power fast sampling ADC was implemented in the readout electronics for particle physics detectors and published. Although a pipeline ADC was developed previously for the existing prototype of LumiCal readout [63], its power consumption was substantially to high. Taking advantage of the potential of modern deep sub-micron CMOS technologies, a 10-bit SAR ADC was designed and three prototypes were fabricated in two different 130 nm CMOS technologies. The selected SAR architecture was presented and its performance was discussed in details (see Section 3.3). The detailed results of the extensive tests were shown (see Section 3.3.4), with particular emphasis on the last prototype, so-called ADC_B_V1 (see Section 3.3.4). Its excellent performance places this design among the best, currently existing designs, what may be verified by comparing it with the State of Art ADCs, with similar technology and specifications, taken from the best engineering journals. The comparison of the key parameters is presented in Table S.1. The well known Walden Figure Of Merit (FOM) [105, 106], showing the power efficiency, for all the compared designs (including the one presented in this dissertation) remains between 29-57 fJ/conversion. Most of designs have the ENOB above 9 bits, however, both the ENOB as the linearity (INL, DNL) of the developed ADC_B_V1 prototype are the best among the presented, moreover, the occupied area is the smallest.

	[100]	[101]	[102]	[103]	[104]	This work (ADC_B_V1)
Architecture	SAR	SAR	SAR	SAR	SAR	SAR
Resolution	10-bit	10-bit	10-bit	10-bit	10-bit	10-bit
Process (nm)	90	130	130	90	130	130
Area (mm^2)	0.1	0.052	0.32	0.18	0.095	0.047
Input range (V)	± 1.2	± 1	± 1.2	± 0.6	± 1.2	± 1.2
f_{sample} (MS/s)	30	50	40	100	20	0.01–40
Power (μW)	980	826	550	3000	620	∼400@20MS/s,
Max INL (LSB)	1.32	1.36	1.55	0.86	0.47	∼0.2@20MS/s
Max DNL (LSB)	0.88	0.91	0.78	0.79	0.34	∼0.3@20MS/s
ENOB (bit)	9.16	9.18	8.35	9.1	9.32	9.47@20MS/s
FOM (fJ/conv.)	57	29	42	55	41	30-40

Table S.1: Comparison with State of Art ADCs.

During the long R&D activities, author gathered a unique experience in the construction and testing of advanced radiation detection systems, particularly involving the design and testing of dedicated readout ASICs. The works performed by author covered all phases of the development of typical particle physics experiment, starting from the conceptual and design works, through the development of core system components and dedicated electronic readout, followed by the preparation and participation in testbeam, and finishing with elaboration and analysis of the collected experimental data.

Future improvements are still foreseen for the LumiCal detector. In order to meet the narrow geometrical requirements, a sophisticated sensor supporting structure, with overall thickness lower than 1 mm, needs to be designed. Simultaneously, a completely new readout system with dedicated DAQ has to be developed to enable experimental verification of the complete, 30-layer prototype of the LumiCal detector. The developed front-end and ADC prototypes enable the possibility to integrate and fabricate a full functionality, multi-channel System-on-Chip (SoC) readout ASIC for the LumiCal detector. This will be the next task taken by author. Such a system will be one of the first, if not the first in the world, multi-channel readout SoC ASIC, with a fast ultra-low power ADC implemented in each channel.

Acronyms

ADC Analog-to-Digital Converter . . . 40
ALICE A Large Ion Collider Experiment . . . 16
AMCS Asymmetric MCS . . . 116
APV Analog Pipeline Voltage . . . 79
ASIC Application Specific Integrated Circuit . . . 31
ATLAS A Toroidal LHC Apparatus . . . 16
BDS Beam Delivery System . . . 21
BSM Beyond Standard Model . . . 16
BeamCal Beam Calorimeter . . . 25
CCD Charge-Coupled Device . . . 27
CERN Conseil Européen pour la Recherche Nucléaire . . . 16
CLIC Compact Linear Collider at CERN . . . 17
CMOS Complementary Metal-Oxide Semiconductor . . . 27
CMS Compact Muon Solenoid . . . 16
CMS Common Mode Subtraction . . . 41
CP Charge Parity . . . 18
CPS CMOS Pixel Sensors . . . 27
CVD Chemical Vapor Deposition . . . 37
CW Continuous–Wave . . . 20
DAC Digital-to-Analog Converter . . . 51
DAQ Data Acquisition System . . . 40
DC Direct Current . . . 19
DEPFET DEPleted Field Effect Transistor . . . 27
DESY Deutsches Elektronen-Synchrotron . . . 48
DFT Discrete Fourier Transform . . . 131
DNL Differential Nonlinearity . . . 121
DSP Digital Signal Processing . . . 40
DUT Device Under Test . . . 64
ECAL Electromagnetic Calorimeter . . . 25
EMCS Early Reset MCS . . . 116
ENC Equivalent Noise Charge . . . 110
ENOB Effective Number Of Bits . . . 132
ETD End-cap of TPC Detector . . . 28
FC Folded Cascode . . . 106
FCAL Forward CALorimetry . . . 33
FE Frond-end electronics . . . 126
FIR Finite Impulse Response . . . 79

FPGA Field-Programmable Gate Array . . . 40
FPCCD Fine Pixel CCD . . . 27
FTD Forward Tracker Detector . . . 28
FOM Figure Of Merit . . . 144
FSM Finite State Machine . . . 127
GBW Gain–Bandwidth Product . . . 106
GEM Gas Electron Multiplier . . . 28
GPIB General Purpose Interface Bus . . . 108
GUT Grand Unified Theory . . . 19
HCAL Hadronic Calorimeter . . . 25
HEP High Energy Physics . . . 16
HERA Hadron-Electron Ring Accelerator . . . 16
HV High Voltage . . . 53
IDN IDentification Number . . . 87
IIR Infinite Impulse Response . . . 79
ILC International Linear Collider . . . 17
ILD International Large Detector . . . 25
INL Integral Nonlinearity . . . 130
IP Interaction Point . . . 20
LAN Local Area Network . . . 108
LDO Low Drop-Out . . . 129
LEP Large Electron Positron Collider . . . 16
LHC Large Hadron Collider . . . 16
LHCAL Luminosity Hadronic CALorimeter . . . 32
LHCb Large Hadron Collider beauty . . . 16
LSB Least Significant Bit . . . 75
LVDS Low-Voltage Differential Signaling . . . 51
LumiCal Luminosity Calorimeter . . . 25
MAPS Monolithic Active Pixel Sensors . . . 62
MBK Multi-Beam Klystrons . . . 20
MC Monte Carlo . . . 32
MCS Merge Capacitor Switching . . . 116
MDAC Multiplying DAC . . . 51
MIP Minimum Ionizing Particle . . . 39
MOS Metal-Oxide Semiconductor . . . 50
MPV Most Probable Value . . . 42
MSB Most Significant Bit . . . 115
PC Personal Computer . . . 49
PCB Printed Circuit Board . . . 40
PFA Particle Flow reconstruction Algorithm . . . 24
PS Proton Synchrotron . . . 55
PXI PCI eXtensions for Instrumentation . . . 62
PZC Pole-Zero Cancellation . . . 50
QCD Quantum Chromodynamics . . . 17
QED Quantum ElectroDynamics . . . 35
RF Radio Frequency . . . 20
RFC Recycled Folded Cascode . . . 106

Bibliography

[1] O. S. Brüning, P. Collier, P. Lebrun, S. Myers, R. Ostojic, J. Poole, and P. Proudlock, *LHC Design Report*. Geneva: CERN, 2004. [Online]. Available: http://ab-div.web.cern.ch/ab-div/publications/LHC-DesignReport.html [Accessed: 15 May 2015]

[2] J. Brau, Y. Okada, N. Walker, and et al, Eds., *International Linear Collider Reference Design Report*. ILC Global Design Effort and World Wide Study, Aug. 2007, vol. 2: Executive Summary. [Online]. Available: http://ilcdoc.linearcollider.org/record/6321/files/ILC_RDR_Volume_1-Executive_Summary.pdf [Accessed: 15 May 2015]

[3] A. Djouadi, J. Lykken, K. Mönig, Y. Okada, M. Oreglia, and S. Yamashita, Eds., *International Linear Collider Reference Design Report*. ILC Global Design Effort and World Wide Study, Aug. 2007, vol. 2: Physics at the ILC. [Online]. Available: http://ilcdoc.linearcollider.org/record/6321/files/ILC_RDR_Volume_2-Physics_at_the_ILC.pdf [Accessed: 15 May 2015]

[4] T. Behnke, C. Damerell, J. Jaros, and A. Miyamoto, Eds., *International Linear Collider Reference Design Report*. ILC Global Design Effort and World Wide Study, Aug. 2007, vol. 4: Detectors. [Online]. Available: http://ilcdoc.linearcollider.org/record/6321/files/ILC_RDR_Volume_4-Detectors.pdf [Accessed: 16 May 2015]

[5] N. Phinney, N. Toge, and N. Walker, Eds., *International Linear Collider Reference Design Report*. ILC Global Design Effort and World Wide Study, Aug. 2007, vol. 3: Accelerator. [Online]. Available: http://ilcdoc.linearcollider.org/record/6321/files/ILC_RDR_Volume_3-Accelerator.pdf [Accessed: 15 May 2015]

[6] M. Battaglia, A. de Roeck, J. R. Ellis, and D. Schulte, *Physics at the CLIC Multi-TeV Linear Collider : report of the CLIC Physics Working Group*. Geneva: CERN, 2004.

[7] L. Linssen and et al., *Physics and Detectors at CLIC: CLIC Conceptual Design Report*. CERN, 2012. [Online]. Available: http://arxiv.org/pdf/1202.5940v1 [Accessed: 17 May 2015]

[8] E. John and W. Ian, "New physics with the compact linear collider," *Nature*, vol. 409, 2001. [Online]. Available: http://dx.doi.org/10.1038/35053224 [Accessed: 17 May 2015]

[9] T. Behnke, J. E. Brau, B. Foster, J. Fuster, M. Harrison, J. M. Paterson, M. Peskin, M. Stanitzki, N. Walker, and H. Yamamoto, Eds., *International Linear Collider Technical Design Report*. ILC Global Design Effort and World Wide Study, Jun. 2013, vol. 1: Executive Summary. [Online]. Available: https://www.linearcollider.org/ILC/Publications/Technical-Design-Report [Accessed: 13 May 2015]

[10] J. Wess and B. Zumino, "A lagrangian model invariant under supergauge transformations," *Phys. Lett. B*, vol. 49, no. 1, pp. 52–54, 1974.

[11] A. Salam and J. A. Strathdee, "Superfields and fermi-bose symmetry," *Phys. Rev. D*, vol. 11, p.

1521, 1975.

[12] S. Stapnes and et al., *CLIC Conceptual Design Report*. CERN, 2012. [Online]. Available: http://project-clic-cdr.web.cern.ch/project-CLIC-CDR/ [Accessed: 17 May 2015]

[13] T. Behnke, J. E. Brau, P. Burrows, J. Fuster, M. Peskin, M. Stanitzki, Y. Sugimoto, S. Yamada, and H. Yamamoto, Eds., *International Linear Collider Technical Design Report*. ILC Global Design Effort and World Wide Study, Jun. 2013, vol. 4: Detectors. [Online]. Available: https://www.linearcollider.org/ILC/Publications/Technical-Design-Report [Accessed: 19 May 2015]

[14] T. Abe and et al., "The International Large Detector: Letter of Intent," ILD Concept Group - Linear Collider Collaboration, Tech. Rep., 2010, FERMILAB-LOI-2010-03, FERMILAB-PUB-09-682-E, DESY-2009-87, KEK-REPORT-2009-6. [Online]. Available: http://arxiv.org/pdf/1006.3396v1 [Accessed: 19 May 2015]

[15] H. Aihara and et al., "Sid letter of intent," SiD Collaboration, Tech. Rep., 2009, SLAC-R-944. [Online]. Available: http://arxiv.org/pdf/0911.0006v1 [Accessed: 19 May 2015]

[16] C. Hu-Guo, J. Baudot, G. Bertolone, A. Besson, A. Brogna, and et al., "First reticule size maps with digital output and integrated zero suppression for the eudet-jra1 beam telescope," *Nucl.Instrum.Meth.*, vol. A623, pp. 480–482, 2010.

[17] I. Valin, C. Hu-Guo, J. Baudot, G. Bertolone, A. Besson, and et al., "A reticle size cmos pixel sensor dedicated to the star hft," *JINST*, vol. 7, 2012.

[18] L. Greiner, E. Anderssen, H. Matis, H. Ritter, J. Schambach, and et al., "A maps based vertex detector for the star experiment at rhic," *Nucl.Instrum.Meth*, vol. A650, pp. 68–72, 2011.

[19] Y. Sugimoto, H. Ikeda, D. Kamai, E. Kato, A. Miyamoto, and et al., "R&d status of fpccd vertex detector for ild," Tech. Rep., 2012. [Online]. Available: http://arxiv.org/abs/1202.5832 [Accessed: 19 May 2015]

[20] Y. Sugimoto, H. Ikeda, A. Miyamoto, T. Nagamine, Y. Takubo, and et al., "R and d status of fpccd vtx," Tech. Rep., 2009, LCWS2008 Proceedings. [Online]. Available: http://arxiv.org/abs/0902.2067 [Accessed: 19 May 2015]

[21] D. Collaboration, O. Alonso, and et al., "Depfet active pixel detectors for a future linear e+e- collider," *Nuclear Science, IEEE Transactions on*, vol. 60, pp. 1457–1465, 2013.

[22] J. Velthuis, R. Kohrs, M. Mathes, A. Raspereza, L. Reuen, and et al., "Depfet, a monolithic active pixel sensor for the ilc," *Nucl.Instrum.Meth.*, vol. A579, pp. 685–689, 2007.

[23] K. A. Olive and et al. (Particle Data Group), "Review of Particle Physics," *Chin. Phys. C*, vol. 88, pp. 010 009+, 2014. [Online]. Available: http://pdg.lbl.gov [Accessed: 20 May 2015]

[24] S. Eidelman and et. al., "Review of Particle Physics," *Physics Letters B*, vol. 592, pp. 1+, 2004. [Online]. Available: http://pdg.lbl.gov [Accessed: 27 April 2015]

[25] D. Green, *The Physics of Particle Detectors*. Cambridge University Press, 2005.

[26] H. Abramowicz and et al., "Instrumentation of the very forward region of a linear collider detector," *Nuclear Science, IEEE Transactions on*, vol. 51, no. 6, pp. 2983 – 2989, dec. 2004. [Online]. Available: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=1369422 [Accessed: 21 May 2015]

[27] K. Nakamura and et al. (Particle Data Group), "Review of particle physics," *J. Phys. G: Nucl. Part. Phys.*, vol. 37, no. 7A, p. 075021, 2010.

[28] K. Yokoya and P. Chen., "Beam-beam phenomena in linear colliders," KEK, Tech. Rep., April 1995, KEK Preprint 91-2. [Online]. Available: http://citeseerx.ist.psu.edu/viewdoc/summary?doi=10.1.1.44.2209 [Accessed: 10 May 2015]

[29] M. A. Pons, P. Bambade, and A. Faus-Golfe, "Luminosity, beamstrahlung energy loss and beam-beam deflection for e^+e^- and e^-e^- collisions at the ilc with 500 gev and varying transverse beam sizes," LAL, Tech. Rep., Jan 2006, LAL/RT 06-01. [Online]. Available: http://www.iaea.org/inis/collection/NCLCollectionStore/_Public/38/097/38097077.pdf [Accessed: 8 May 2015]

[30] K. Yokoya and P. Chen, "Beam-beam phenomena in linear colliders," in *Frontiers of Particle Beams: Intensity Limitations*, ser. Lecture Notes in Physics. Springer Berlin Heidelberg, 1992, vol. 400, pp. 415–445. [Online]. Available: http://dx.doi.org/10.1007/3-540-55250-2_37 [Accessed: 10 May 2015]

[31] M. Ohlerich, "Investigations of the physics potential and detector development for the ilc," Ph.D. dissertation, Brandenburgischen Technischen Universität Cottbus, 2010. [Online]. Available: http://www-library.desy.de/preparch/desy/thesis/desy-thesis-10-008.pdf [Accessed: 17 May 2015]

[32] E. Caffo, M ; Remiddi, "Bhabha scattering," *Workshop on Z Physics at LEP1*, vol. 1, pp. 171–202, Sep 1989.

[33] R. Bonciani and A. Ferroglia, "Bhabha scattering at nnlo," *Nuclear Physics B - Proceedings Supplements*, vol. 181–182, no. 0, pp. 259 – 263, 2008, Proceedings of the International Workshop on e+e- Collisions. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0920563208001655 [Accessed: 8 May 2015]

[34] S. Actis, M. Czakon, J. Gluza, and T. Riemann, "Fermionic NNLO contributions to Bhabha scattering," *Acta Phys.Polon.*, vol. B38, pp. 3517–3528, 2007.

[35] A. Penin, "Two-loop photonic corrections to massive bhabha scattering," *Nuclear Physics B*, vol. 734, no. 1–2, pp. 185 – 202, 2006. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S055032130501000X [Accessed: 14 May 2015]

[36] "Superconducting darmstadt linear accelerator." [Online]. Available: http://www.ikp.tu-darmstadt.de/sdalinac_ikp/ [Accessed: 18 May 2015]

[37] C. Grah and et al., "Polycrystalline cvd diamonds for the beam calorimeter of the ilc," *Nuclear Science, IEEE Transactions on*, vol. 56, no. 2, pp. 462 –467, april 2009. [Online]. Available: http://dx.doi.org/10.1109/TNS.2009.2013853 [Accessed: 22 May 2015]

[38] C. Grah, K. Afanaciev, P. Bernitt, G. Chelkov, J. Gajewski, R. Heller, H. Henschel, A. Ignatenko, Z. Krumshteyn, S. Kulis, W. Lange, W. Lohmann, M. Ohlerich, A. Rosco, A. Sapronov, R. Schmidt, and S. Schuwalow, "Radiation hard sensors for the beam calorimeter of the ilc," in *Nuclear Science Symposium Conference Record, 2007. NSS '07. IEEE*, vol. 3, 26 2007-nov. 3 2007, pp. 2281 –2284. [Online]. Available: http://dx.doi.org/10.1109/NSSMIC.2007.4436601 [Accessed: 28 May 2015]

[39] K. Afanaciev and et al., "Investigation of the radiation hardness of gaas sensors in an electron beam," *JINST*, vol. 7, p. 11022, 2012.

[40] A. Abusleme, "The bean: a pulse processor for a particle physics experiment," Ph.D.

dissertation, Stanford University., 2011. [Online]. Available: http://purl.stanford.edu/pj537bm6926 [Accessed: 2 July 2015]

[41] J. Blocki and et al., "Lumical new mechanical structure," *EUDET-Memo*, no. 10, 2009. [Online]. Available: http://www.eudet.org/e26/e28/e42441/e68452/EUDET-Memo-2009-10.doc [Accessed: 1 July 2015]

[42] J. Blocki, W. Daniluk, E. Kielar, J. Kotula, A. Moszczynski, K. Oliwa, B. Pawlik, W. Wierba, L. Zawiejski, and J. Aguilar, "Redesign of lumical mechanical structure," *EUDET-Memo*, no. 06, 2010. [Online]. Available: http://www.eudet.org/e26/e28/e86887/e98740/EUDET-MEMO-2010-06.doc [Accessed: 02 June 2015]

[43] H.Abramowicz, R.Ingbir, S.Kananov, A.Levy, and I.Sadeh, "Revised requirements on the readout of the luminosity calorimeter," *EUDET-Memo*, no. 8, 2008. [Online]. Available: http://www.eudet.org/e26/e28/e615/e783/eudet_memo_2008_08.pdf [Accessed: 1 June 2015]

[44] J. Blocki and et al., "Silicon sensors prototype for lumical calorimeter," *EUDET-Memo*, no. 7, 2009. [Online]. Available: http://www.eudet.org/e26/e28/e42441/e68451/EUDET-MEMO-2009-07.doc [Accessed: 22 May 2015]

[45] T. Awes, F. Obenshain, F. Plasil, S. Saini, S. Sorensen, and G. Young, "A simple method of shower localization and identification in laterally segmented calorimeters," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 311, no. 1–2, pp. 130 – 138, 1992. [Online]. Available: http://www.sciencedirect.com/science/article/pii/0168900292908582 [Accessed: 2 June 2015]

[46] H. Abramowicz, R. Ingbir, S. Kananov, A. Levy, and I. Sadeh, "Geant4 simulation of the electronic readout.constraints for the luminosity detector of the ilc." *EUDET-Memo*, no. 17, 2007. [Online]. Available: http://www.eudet.org/e26/e28/e182/e308/eudet-memo-2007-17.pdf [Accessed: 11 July 2015]

[47] I. Sadeh, "Luminosity measurement at the international linear collider," Master's thesis, Tel Aviv University, 2008. [Online]. Available: http://alzt.tau.ac.il/~sadeh/mscThesis.html [Accessed: 26 May 2015]

[48] H. Abramowicz and et al., "Performance of fully instrumented detector planes of the forward calorimeter of a linear collider detector," *JINST*, vol. 10, may 2015.

[49] M. Idzik, S. Kulis, and D. Przyborowski, "Development of front-end electronics for the luminosity detector at ilc," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 608, no. 1, pp. 169 – 174, 2009. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0168900209013151 [Accessed: 24 May 2015]

[50] M. Idzik, K. Świentek, T. Fiutowski, S. Kulis, and P. Ambalathankandy, "A power scalable 10-bit pipeline adc for luminosity detector at ilc," *JINST*, vol. 6 P01004, 2011.

[51] D. Groom and S. Klein, "Passage of particles through matter," *The European Physical Journal C - Particles and Fields*, vol. 15, pp. 163–173, 2000, 10.1007/BF02683419. [Online]. Available: http://dx.doi.org/10.1007/BF02683419 [Accessed: 4 May 2015]

[52] M. Berger, J. Coursey, M. Zucker, and J. Chang, "Stopping-power and range tables for electrons, protons, and helium ions," Tech. Rep., 2005. [Online]. Available:

http://www.nist.gov/pml/data/star/index.cfm [Accessed: 27 May 2015]

[53] H. Bichsel, "Straggling in thin silicon detectors," *Rev. Mod. Phys.*, vol. 60, pp. 663–699, Jul 1988. [Online]. Available: http://link.aps.org/doi/10.1103/RevModPhys.60.663 [Accessed: 16 May 2015]

[54] L. Landau, "On the energy loss of fast particles by ionization," *Journal of physics*, 1944.

[55] P. Vavilov, "Ionization losses of high-energy heavy particles," *Soviet Phys. JETP*, vol. 5, pp. 749–51, Nov 1957.

[56] H. Spieler, *Semiconductor Detector Systems*. Oxford University Press, Oct. 2005. [Online]. Available: http://www.oup.com/us/catalog/general/subject/EngineeringTechnology/ElectricalComputerEngineering/?view=usa&ci=9780198527848 [Accessed: 13 June 2015]

[57] S. Ramo, "Currents induced by electron motion," *Proceedings of the IRE*, vol. 27, no. 9, pp. 584 – 585, sept. 1939.

[58] G. Cavalleri, E. Gatti, G. Fabri, and V. Svelto, "Extension of ramo's theorem as applied to induced charge in semiconductor detectors," *Nuclear Instruments and Methods*, vol. 92, no. 1, pp. 137 – 140, 1971. [Online]. Available: http://www.sciencedirect.com/science/article/pii/0029554X71902357 [Accessed: 7 May 2015]

[59] W. Sansen and Z. Chang, "Limits of low noise performance of detector readout front ends in cmos technology," *Circuits and Systems, IEEE Transactions on*, vol. 37, no. 11, pp. 1375 –1382, nov 1990.

[60] O. Milgrome, S. Kleinfelder, and M. Levi, "A 12 bit analog to digital converter for vlsi applications in nuclear science," *Nuclear Science, IEEE Transactions on*, vol. 39, no. 4, pp. 771–775, aug 1992.

[61] E. Beuville and et al., "Amplex, a low-noise, low-power analog cmos signal processor for multi-element silicon particle detectors," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 288, no. 1, pp. 157 – 167, 1990, Proceedings of the Fifth European Symposium on Semiconductors Detectors. [Online]. Available: http://www.sciencedirect.com/science/article/pii/016890029090481K [Accessed: 18 June 2015]

[62] G. Gramegna, P. O'Connor, P. Rehak, and S. Hart, "Cmos preamplifier for low-capacitance detectors," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 390, no. 1–2, pp. 241 – 250, 1997. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0168900297003902 [Accessed: 13 June 2015]

[63] M. Idzik, K. Swientek, T. Fiutowski, S. Kulis, and D. Przyborowski, "A 10-bit multichannel digitizer asic for detectors in particle physics experiments," *IEEE Trans. Nucl. Sci.*, 2012.

[64] M. Idzik, K. Świentek, and S. Kulis, "Development of pipeline adc for the luminosity detector at ilc," *Proceedings of the 15th International Conference Mixed Design of Integrated Circuits and Systems MIXDES 2008, Poznan, Poland, 19-21 June*, 2008.

[65] M. Idzik, K. Swientek, and S. Kulis, "Design and measurements of 10 bit pipeline adc for the luminosity detector at ilc," *Proceedings of Topical Workshop on Electronics for Particle Physics, TWEPP-09, Paris, France*, Sep. 2009.

[66] S. Kulis, "Development of prototype luminosity detector modules for future experiments

on linear colliders," Ph.D. dissertation, AGH University of Science and Technology, 2013. [Online]. Available: https://cds.cern.ch/record/1613815/files/CERN-THESIS-2012-358.pdf [Accessed: 15 May 2015]

[67] "Eudaq web page." [Online]. Available: http://eudaq.hepforge.org/ [Accessed: 28 May 2015]

[68] F. X. Nuiry, "Aida infrastructure for very forward calorimeters." Discussion on AIDA mechanics for FCAL, Geneva, Switzerland, 2011. [Online]. Available: http://indico.cern.ch/event/147954/contribution/3/material/slides/1.pdf [Accessed: 11 June 2015]

[69] ——, "Aida infrastructure for very forward calorimeters." 22nd FCAL Workshop, Krakow, Poland, 2013. [Online]. Available: https://indico.cern.ch/event/225688/session/7/contribution/11/material/slides/1.pdf [Accessed: 11 June 2015]

[70] A. Himmi and et al., "Mimosa26 User Manual," Institut de Recherches Subatomiques IN2P3-CNRS / ULP Strasbourg – France, Tech. Rep., 2008. [Online]. Available: https://twiki.cern.ch/twiki/pub/MimosaTelescope/MIMOSA26/M26_UserManual_LQ.pdf [Accessed: 23 June 2015]

[71] M. J. D. Powell, "An efficient method for finding the minimum of a function of several variables without calculating derivatives," *Computer Journal*, vol. 7, no. 2, 1964.

[72] K. Pearson, "Notes on regression and inheritance in the case of two parents," *Proceedings of the Royal Society of London*, vol. 58, pp. 240–242, 1985.

[73] F. Galtion, "Regression towards mediocrity in hereditary stature," *Journal of the Anthropological Institute of Great Britain and Ireland*, vol. 15, pp. 246–263, 1886.

[74] T. Bienz, "Strangeonium Spectroscopy at 11 Gev/c and Cherenkov Ring Imaging at the SLD." Ph.D. dissertation, Stanford University., 1990.

[75] S. Gadomski, G. Hall, T. Høgh, P. Jalocha, E. Nygård, and P. Weilhammer, "The deconvolution method of fast pulse shaping at hadron colliders," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 320, no. 1–2, pp. 217 – 227, 1992. [Online]. Available: http://www.sciencedirect.com/science/article/pii/0168900292907794 [Accessed: 16 Feb 2015]

[76] R. G. Lyons, *Understanding Digital Signal Processing*. Prentice Hall, Nov. 2010.

[77] S. Lukić. FCAL Hardware Meeting, 2015. [Online]. Available: https://agenda.linearcollider.org/category/230/ [Accessed: 17 July 2015]

[78] A. Neagu and T. Preda. FCAL clustering meeting, 2015. [Online]. Available: https://agenda.linearcollider.org/category/217/ [Accessed: 17 July 2015]

[79] R. Assaad and J. Silva-Martinez, "The recycling folded cascode: A general enhancement of the folded cascode amplifier," *IEEE J Solid-St. Circ.*, vol. 44, no. 9, 2009.

[80] B. Ginsburg and A. P. Chandrakasan, "An energy-efficient charge recycling approach for a sar converter with capacitive dac," *IEEE ISCAS*, vol. 1, 2005.

[81] C.-C. Liu, S.-J. Chang, G.-Y. Huang, and Y.-Z. Lin, "A 10-bit 50-ms/s sar adc with a monotonic capacitor switching procedure," *IEEE Journal of Solid State Circuits*, vol. 45, no. 4, 2010.

[82] Y.-K. Chang, C.-S. Wang, and C.-K. Wang, "A 8-bit 500-ks/s low power sar adc for bio-medical

application," *IEEE Asian Solid-State Circuits Conferance*, 2007.

[83] Y. Zhu, C. and H Chan, U.-F. Chio, S.-W. Sin, S.-P. U, R.-P. Martins, and F. Maloberti, "A 10-bit 100-ms/s reference-free sar adc in 90 nm cmos," *IEEE Journal of Solid State Circuits*, vol. 45, no. 6, 2010.

[84] V. Hariprasath, J. Guerber, S.-H. Lee, and U.-K. Moon, "Merged capacitor switching based sar adc with highest switching energy-efficiency," *Electronics Letters*, vol. 46, no. 9, 2010.

[85] J. Guerber, H. Venkatram, T. Oh, and U.-K. Moon, "Enhanced sar adc energy efficiency from the early reset merged capacitor switching algorithm," *IEEE International Symposium on Circuits and Systems*, 2012.

[86] Y.-K. Cho., Y.-D. Jeon, J.-W. Nam, and J. Kwon, "A 9-bit 80 ms/s successive approximation register analog-to-digital converter with a capacitor reduction technique," *IEEE Transactions on Circuits and Sytems*, vol. 57, no. 10, 2010.

[87] B. Sedighi, A. Huynh, and E. Skafidas, "Design of the internal dac in sar adcs," *IEEE International Midwest Symposium on Circuits and Systems*, 2015.

[88] C. Yuan and Y. Lam, "Low-energy and area-efficient tri-level switching scheme for sar adc," *Electronics Letters*, vol. 48, no. 9, 2012.

[89] G.-Y. Huang, S.-J. Chang, C.-C. Liu, and Y.-Z. Lin, "10-bit 30ms/s sar adc using a switchback switching method," *IEEE Transactions on VLSI Systems*, vol. 21, no. 3, 2013.

[90] A. Sanyal and N.Sun, "Sar adc architecture with 98% recution in switching energy over conventional scheme," *Electronics Letters*, vol. 49, no. 4, 2013.

[91] Z. Zhu, Y. Xiao, and X. Song, "Vcm-based monotonic capacitor switching scheme for sar adc," *Electronics Letters*, vol. 49, no. 5, 2013.

[92] D. Zhang, *Design of Ultra-Low-Power Analog-to-Digital Converters*. Linköping University, 2012.

[93] M. Dessouky and A. Kaiser, "Input switch configuration for rail-to-rail operation of switched opamp circuits," *Electronics Letters*, vol. 35, no. 1, pp. 8–10, 1999.

[94] H. Jeon and Y.-B. Kim, "Offset voltage analysis of dynamic latched comparator," *IEEE International SOC Conference*, 2010.

[95] M. Chen and R. Brodersen, "A 6b 600 ms/s 5.3 mw asynchronous adc in 0.13 μm cmos," *IEEE Journal of Solid State Circuits*, vol. 41, no. 12, 2006.

[96] G. Kim, M. Kim, and W. K. B.S. Chang, "A low-voltage, low-power cmos delay element," *IEEE Journal of Solid State Circuits*, vol. 31, no. 7, 1996.

[97] S. Tilden and et al., "Ieee standard for terminology and test methods for analog-to-digital converters," *IEEE Std 1241-2010 (Revision of IEEE Std 1241-2000)*, pp. 1–139, 14 2011. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=929859 [Accessed: 26 March 2015]

[98] R. J. Baker, *CMOS mixed-signal circuit design*. Wiley-Interscience, 2002.

[99] J. Moroń, M. Firlej, T. Fiutowski, M. Idzik, K. Świentek, and P. Terlecki, "Development of front-end electronics for lumical detector in cmos 130 nm technology," *JINST*, vol. 10, 2015.

[100] G. Y. Huang, S. J. Chang, C. C. Liu, and Y. Z. Lin, "10-bit 30-ms/s sar adc using a switchback switching method," *IEEE Transactions On Very Large Scale Integration (VLSI) Systems*, vol. 21,

pp. 584–588, 2013.

[101] C. C. Liu, S. J. Chang, G. Y. Huang, and Y. Z. Lin, "A 10-bit 50ms/s sar adc with a monotonic capacitor switching procedure," *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 731–740, 2010.

[102] S. H. Cho, C. K. Lee, J. K. Kwon, and S. T. Ryu, "A 550-uw 10-b 40-ms/s sar adc with multistep addition-only digital error correction," *IEEE Journal of Solid-State Circuits*, vol. 46, pp. 1881–1892, 2011.

[103] Y. Zhu, C. H. Chan, U. F. Chio, S. W. Sin, S. P. U, R. P. Martins, and F. Maloberti, "A 10-bit 100-ms/s reference-free sar adc in 90 nm cmos," *IEEE Journal of Solid State Circuits*, vol. 45, no. 6, 2010.

[104] S. M. Park, Y. H. Jeong, D. G. Jeong, S. W. Baek, Y. J. Hwang, P. H. Lee, and Y. C. Jang, "A 10-bit 20-ms/s asynchronous sar adc with controllable analog input voltage range and meta-stability detection circuit," *International SoC Design Conference (ISOCC)*, pp. 201–203, 2014.

[105] R. Walden, "Analog-to-digital converter technology comparison," *Proc. of GaAs IC Symp.*, pp. 228–231, 1994.

[106] ——, "Analog-to-digital converter survey and analysis," *IEEE J. Selected Areas in Comminications*, no. 4, pp. 539–550, 1999.

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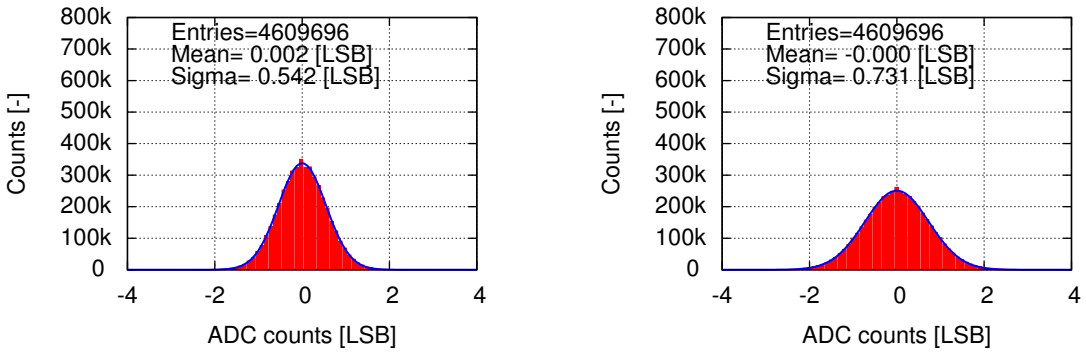
Appendix A

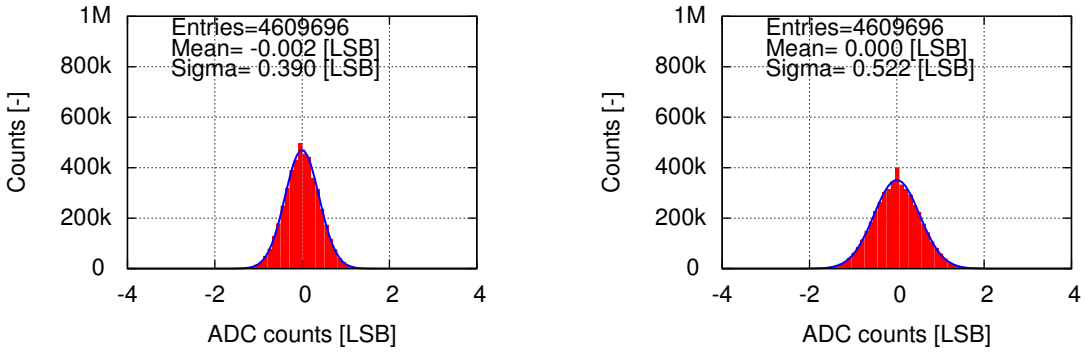
Detail testbeam analysis results

A.1 System noise performance



a) MOS feedback, noise after initial processing

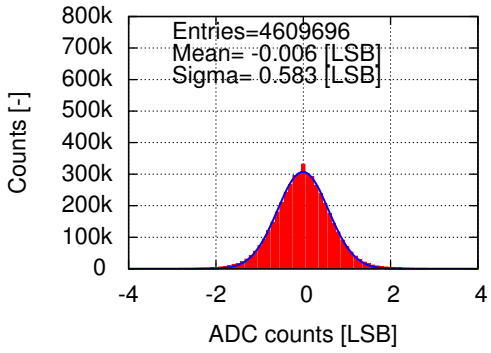
b) MOS feedback, noise after deconvolution



c) R feedback, noise after initial processing

d) R feedback, noise after deconvolution

Figure A.1: Board IDN63 noise performance in the first configuration.



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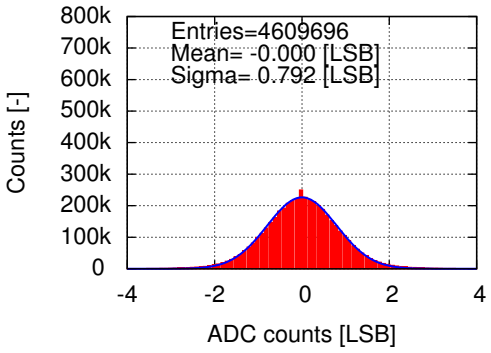
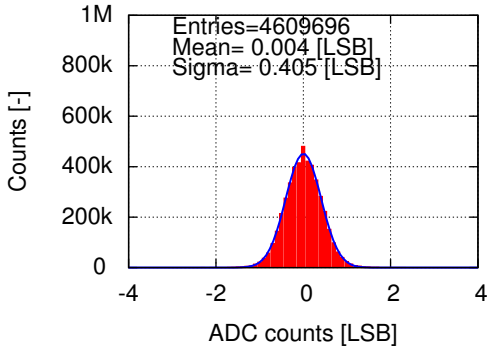
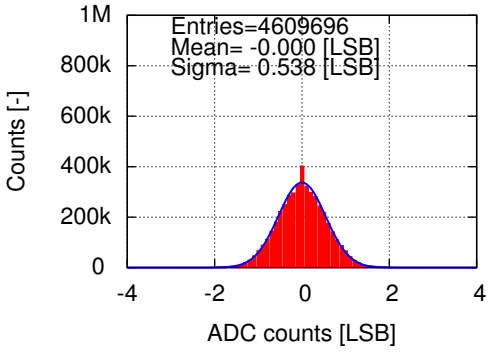


b) MOS feedback, noise after deconvolution

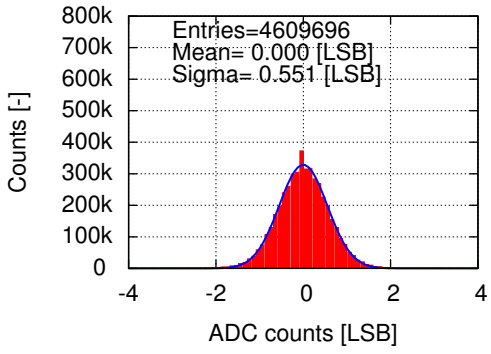


c) R feedback, noise after initial processing



d) R feedback, noise after deconvolution

Figure A.2: Board IDN64 noise performance in the first configuration.



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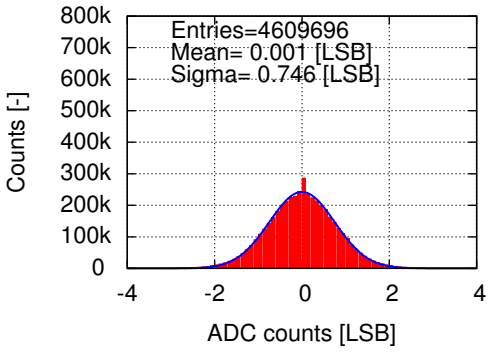
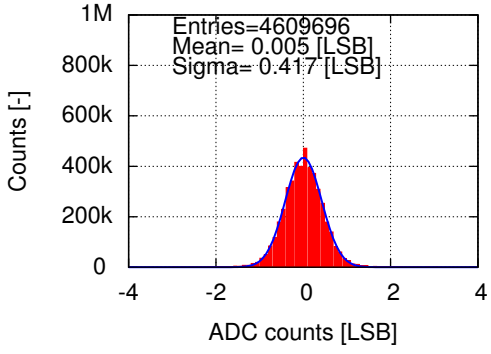


b) MOS feedback, noise after deconvolution



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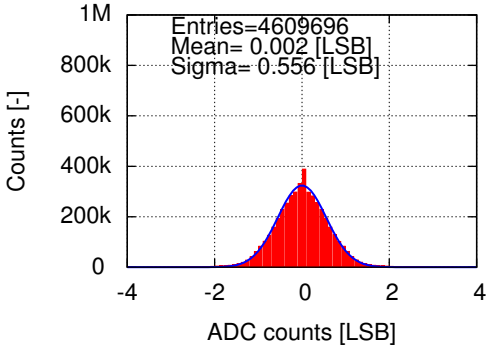

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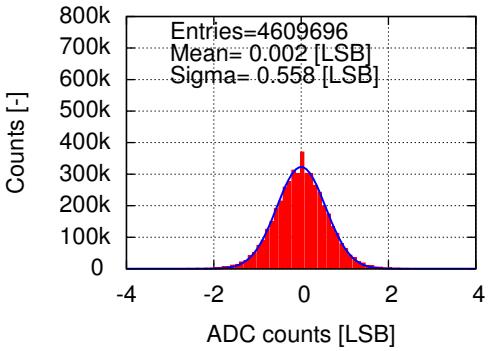
Figure A.3: Board IDN67 noise performance in the first configuration.



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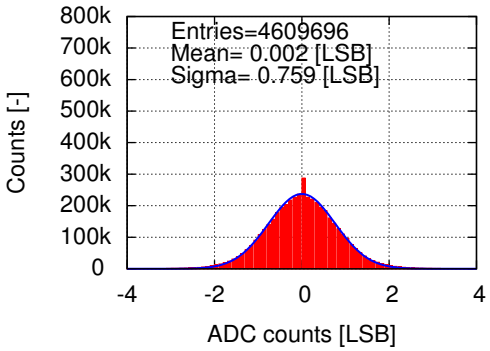
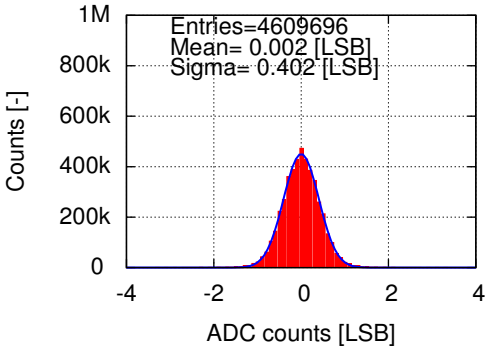


b) MOS feedback, noise after deconvolution



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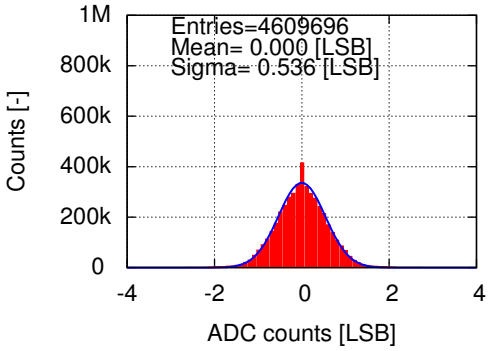
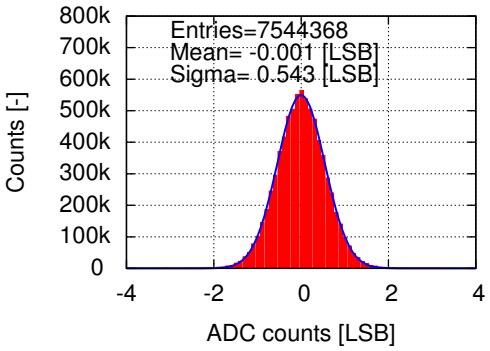


d) R feedback, noise after deconvolution

Figure A.4: Board IDN76 noise performance in the first configuration.



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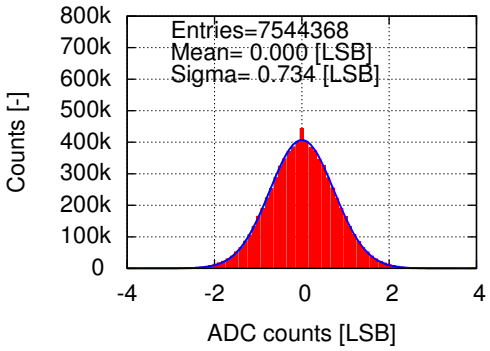
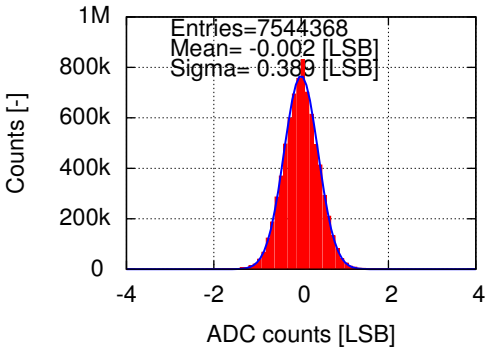


b) MOS feedback, noise after deconvolution



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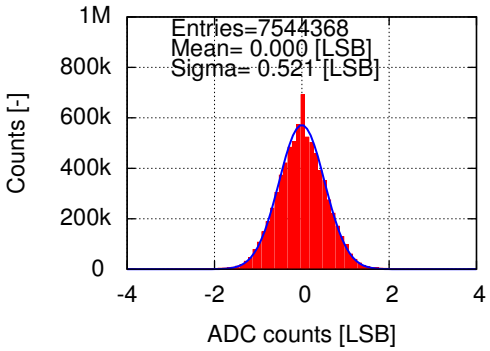
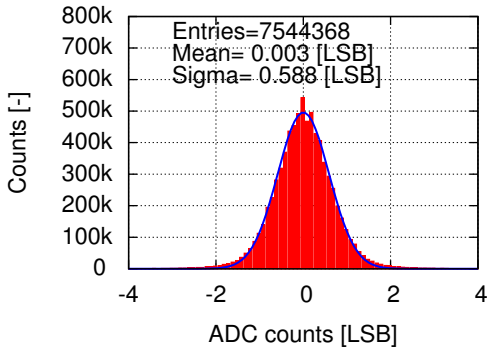


d) R feedback, noise after deconvolution

Figure A.5: Board IDN63 noise performance in the second configuration.



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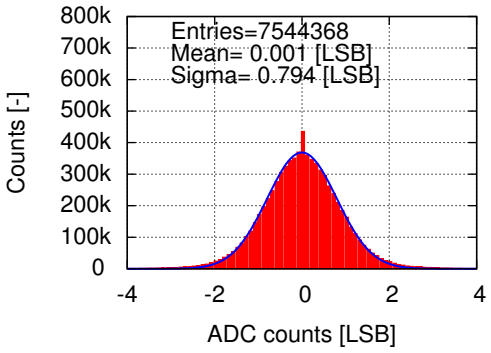
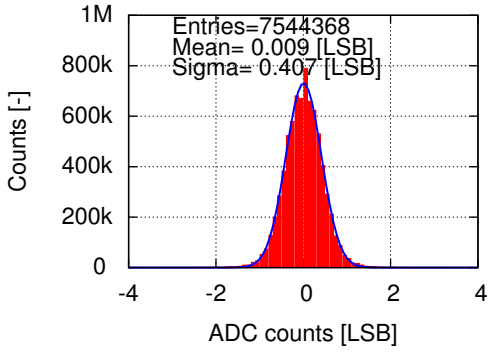


b) MOS feedback, noise after deconvolution



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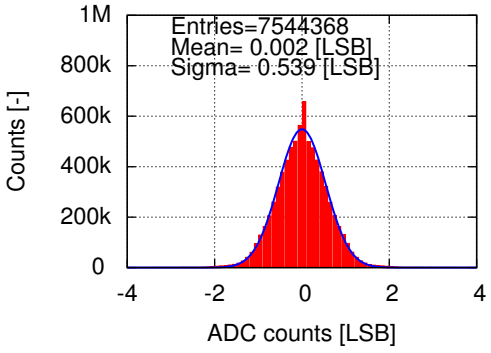
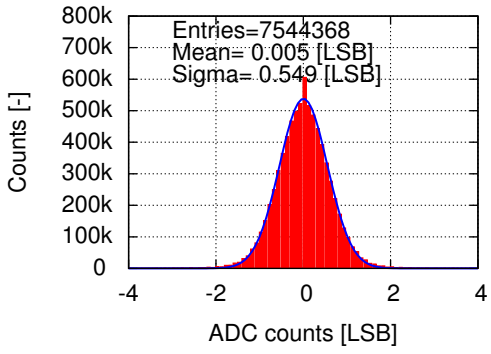


d) R feedback, noise after deconvolution

Figure A.6: Board IDN64 noise performance in the second configuration.



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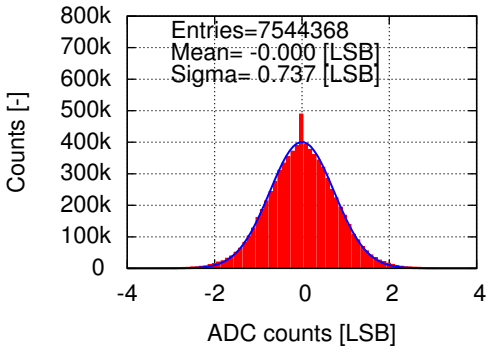

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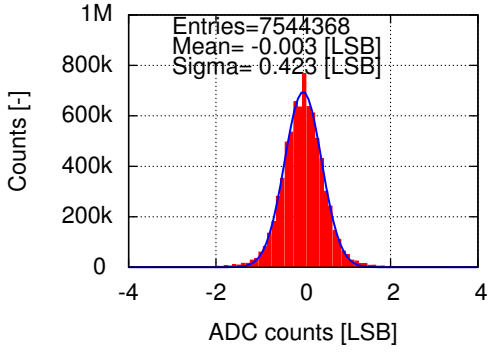

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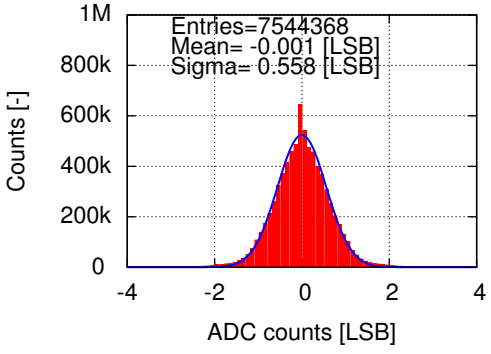

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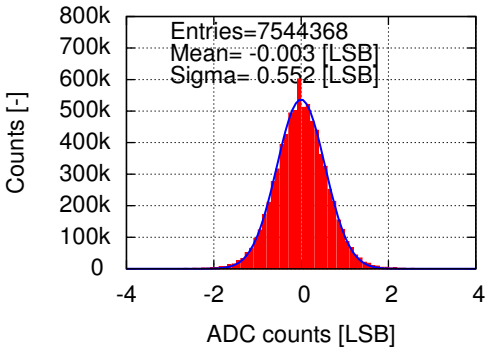
Figure A.7: Board IDN67 noise performance in the second configuration.



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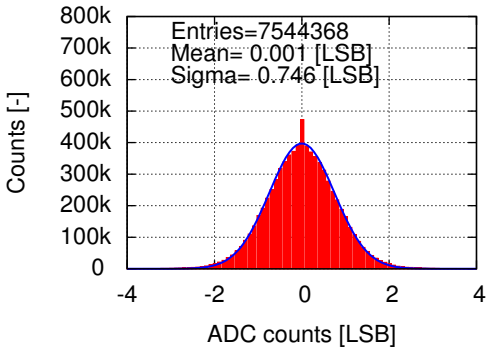

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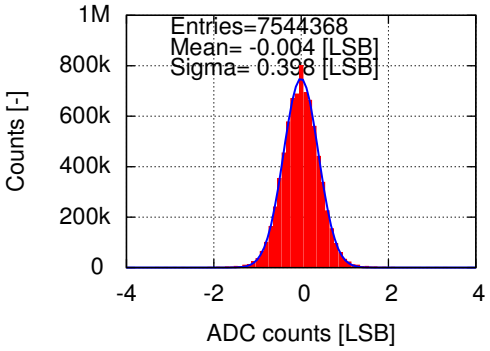
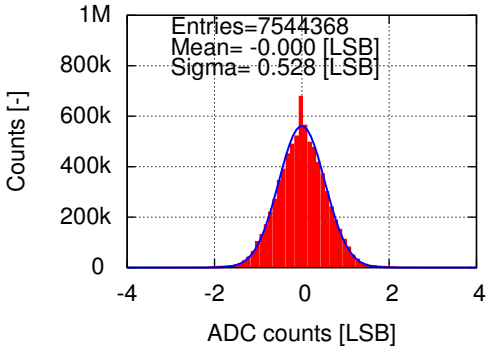
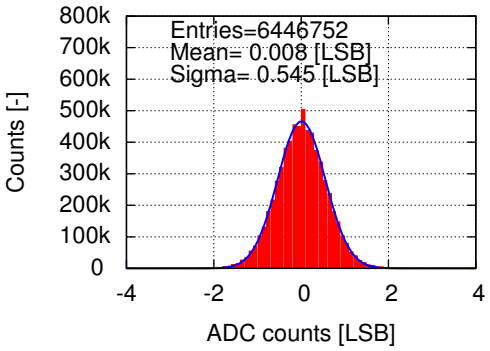


c) R feedback, noise after initial processing

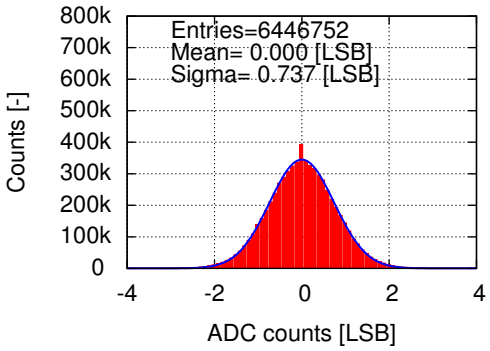


d) R feedback, noise after deconvolution

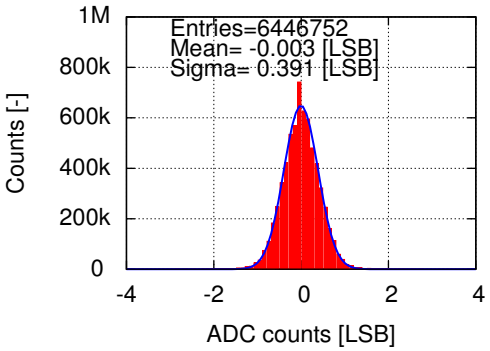
Figure A.8: Board IDN76 noise performance in the second configuration.



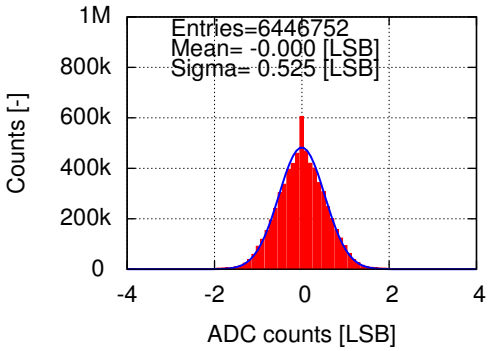
a) MOS feedback, noise after initial processing



b) MOS feedback, noise after deconvolution

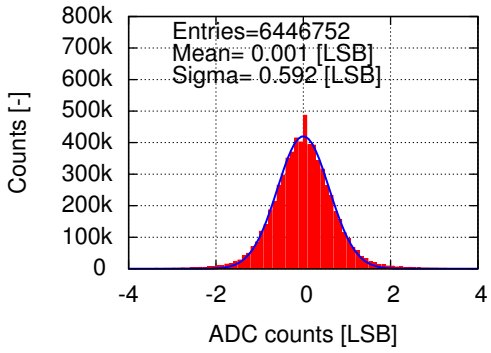


c) R feedback, noise after initial processing

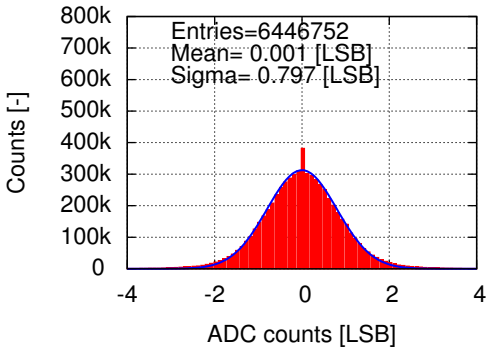


d) R feedback, noise after deconvolution

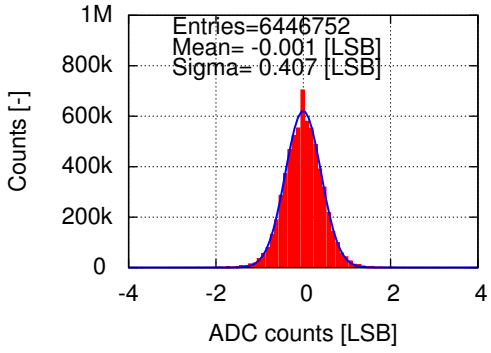
Figure A.9: Board IDN63 noise performance in the third configuration.



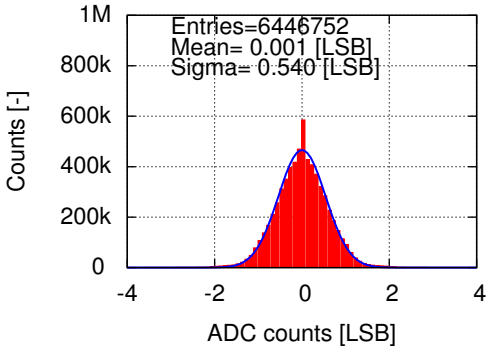
a) MOS feedback, noise after initial processing



b) MOS feedback, noise after deconvolution

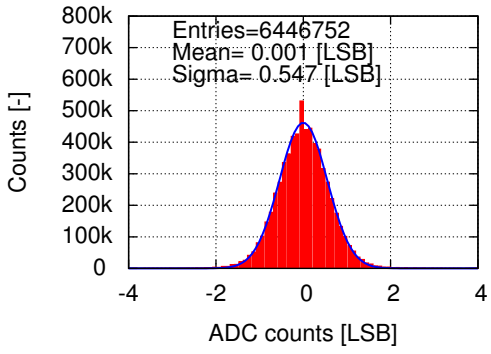


c) R feedback, noise after initial processing

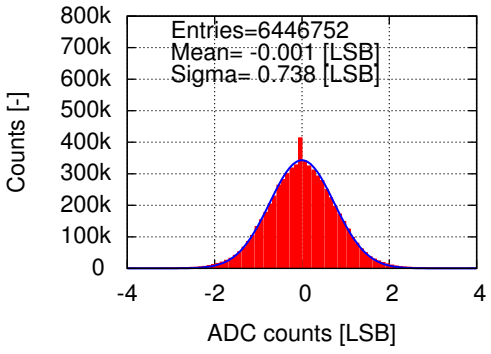


d) R feedback, noise after deconvolution

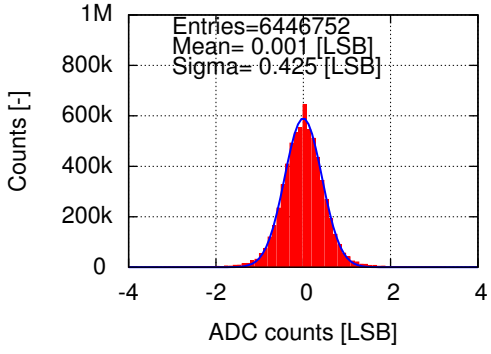
Figure A.10: Board IDN64 noise performance in the third configuration.



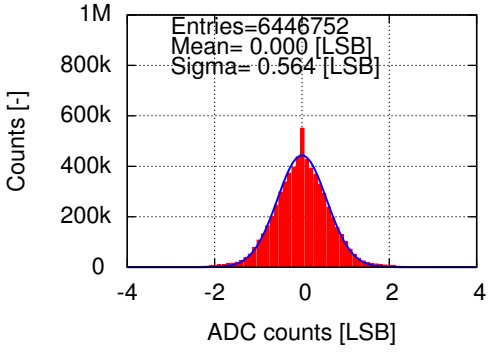
a) MOS feedback, noise after initial processing



b) MOS feedback, noise after deconvolution



c) R feedback, noise after initial processing



d) R feedback, noise after deconvolution

Figure A.11: Board IDN67 noise performance in the third configuration.

A.2 Board gain calibration by the muon peak Most Probable Value (MPV)

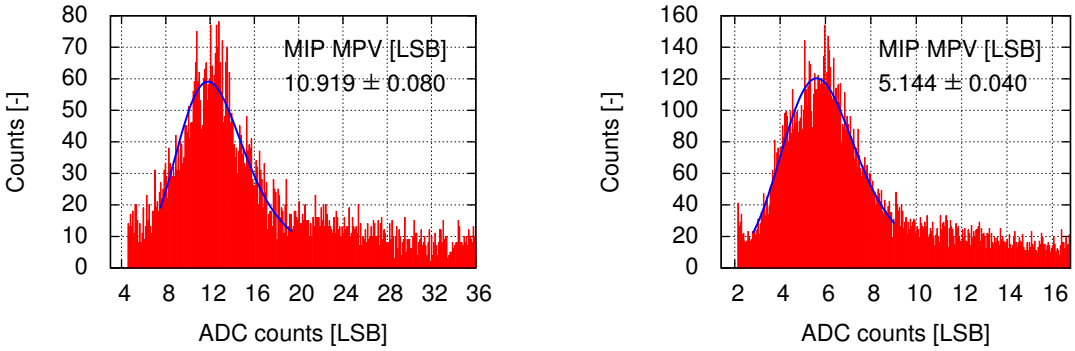


Figure A.12: Channels energy distribution with convolution of Landau and Gauss distributions fitted to the muon peak for board IDN63 in the first configuration.

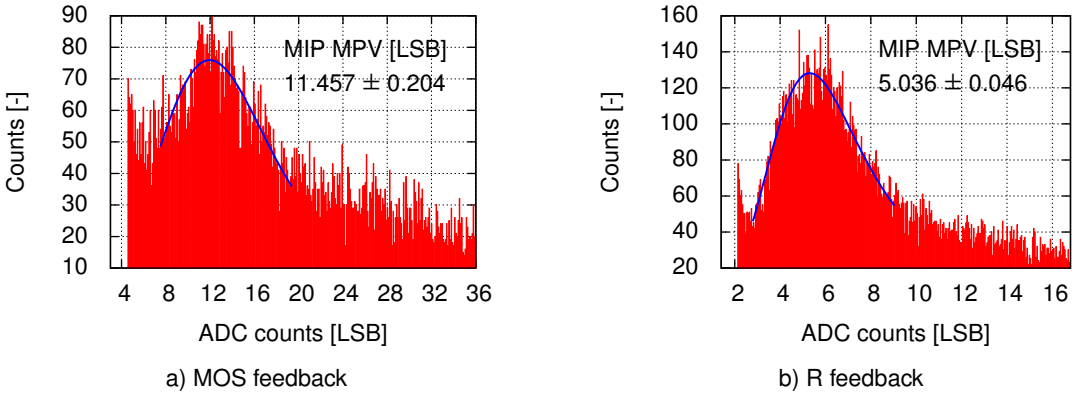


Figure A.13: Channels energy distribution with convolution of Landau and Gauss distributions fitted to the muon peak for board IDN64 in the first configuration.

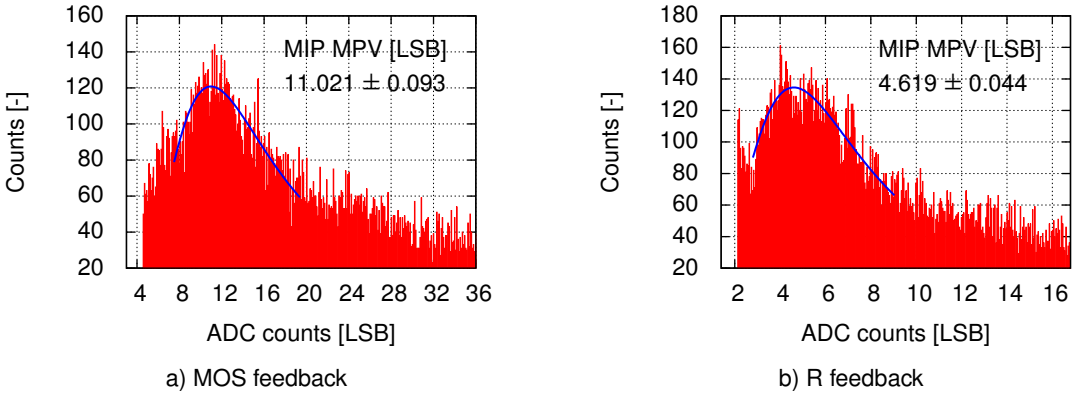
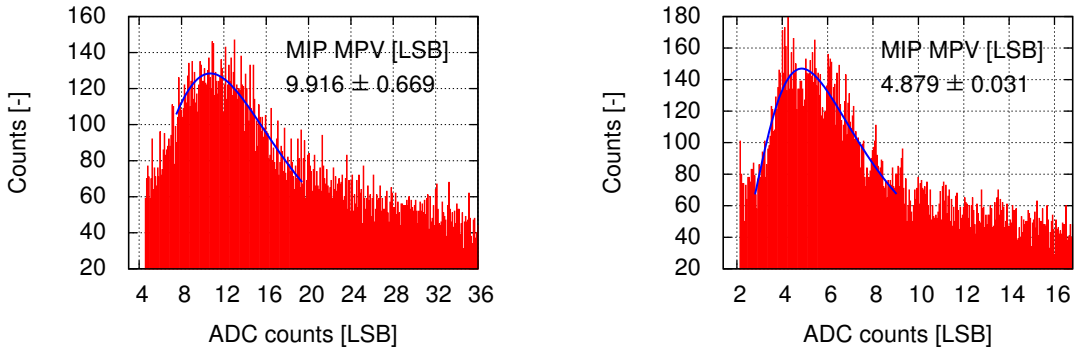
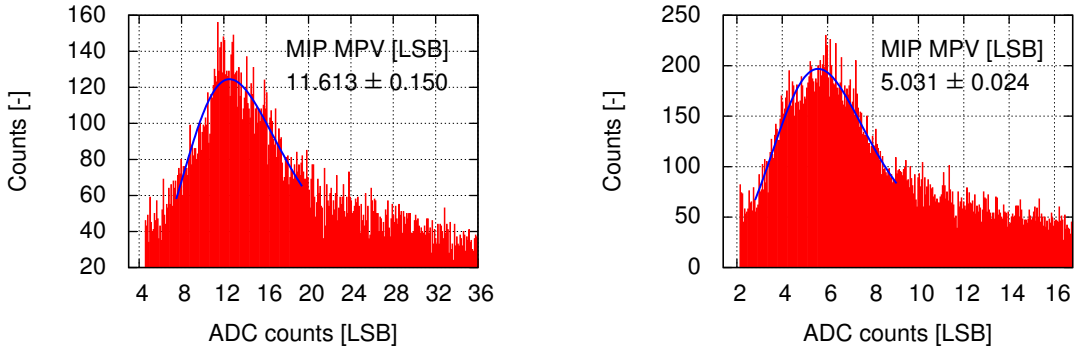


Figure A.14: Channels energy distribution with convolution of Landau and Gauss distributions fitted to the muon peak for board IDN67 in the first configuration.



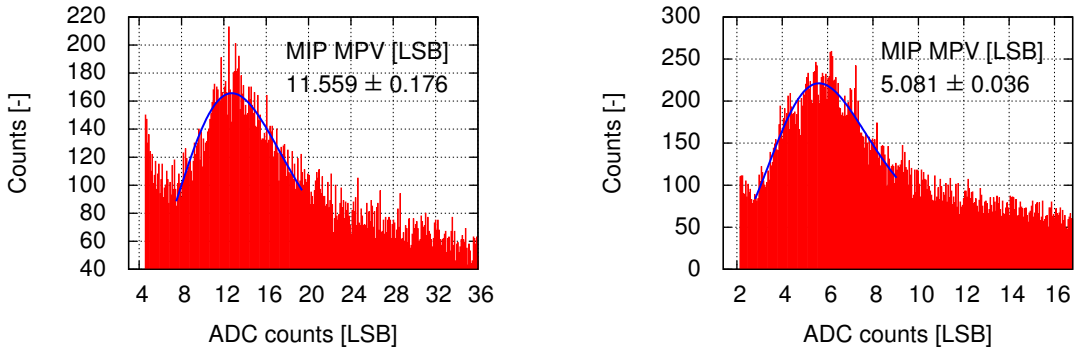
a) MOS feedback b) R feedback

Figure A.15: Channels energy distribution with convolution of Landau and Gauss distributions fitted to the muon peak for board IDN76 in the first configuration.



a) MOS feedback b) R feedback

Figure A.16: Channels energy distribution with convolution of Landau and Gauss distributions fitted to the muon peak for board IDN63 in the second configuration.



a) MOS feedback b) R feedback

Figure A.17: Channels energy distribution with convolution of Landau and Gauss distributions fitted to the muon peak for board IDN64 in the second configuration.

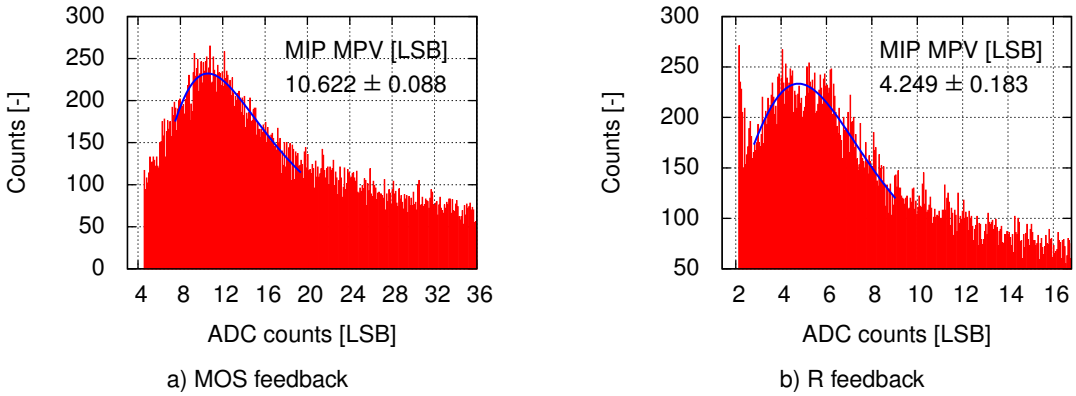


Figure A.18: Channels energy distribution with convolution of Landau and Gauss distributions fitted to the muon peak for board IDN67 in the second configuration.

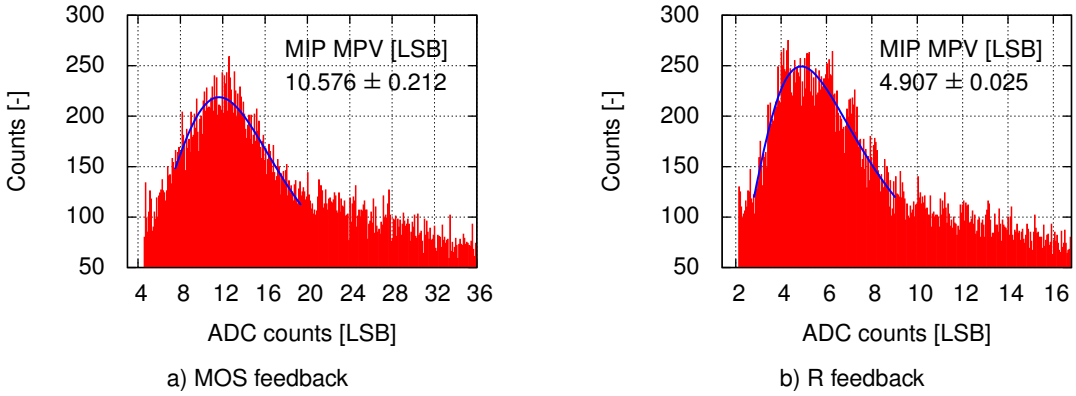


Figure A.19: Channels energy distribution with convolution of Landau and Gauss distributions fitted to the muon peak for board IDN76 in the second configuration.

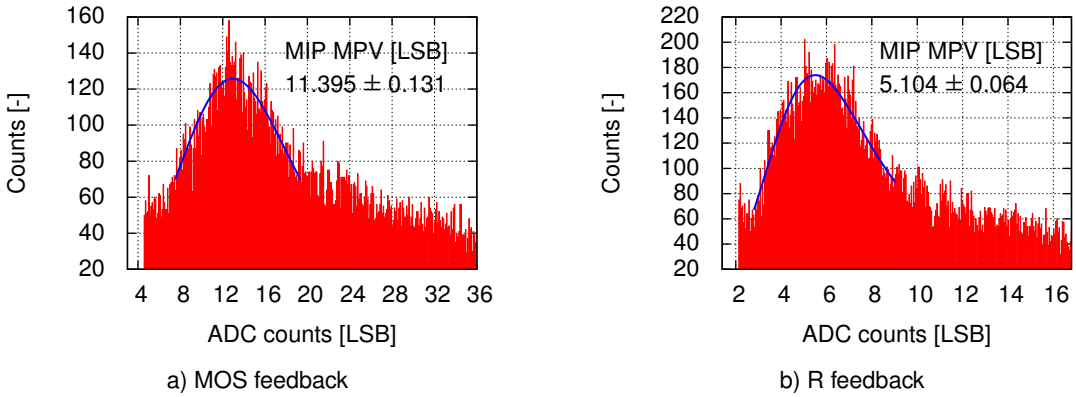
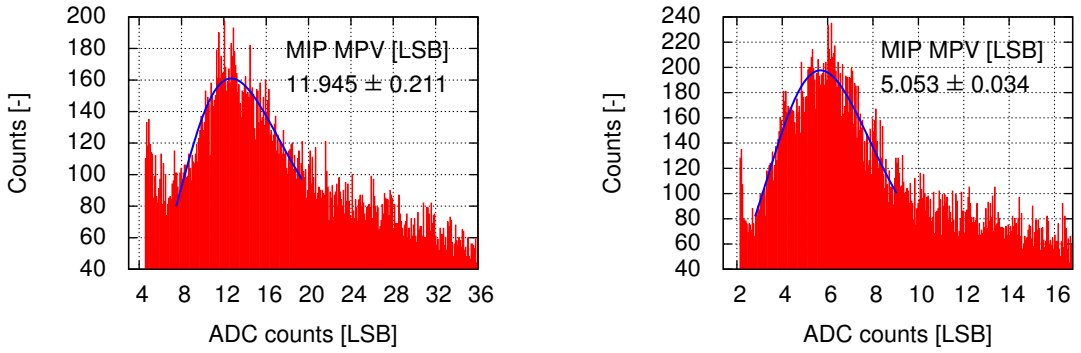
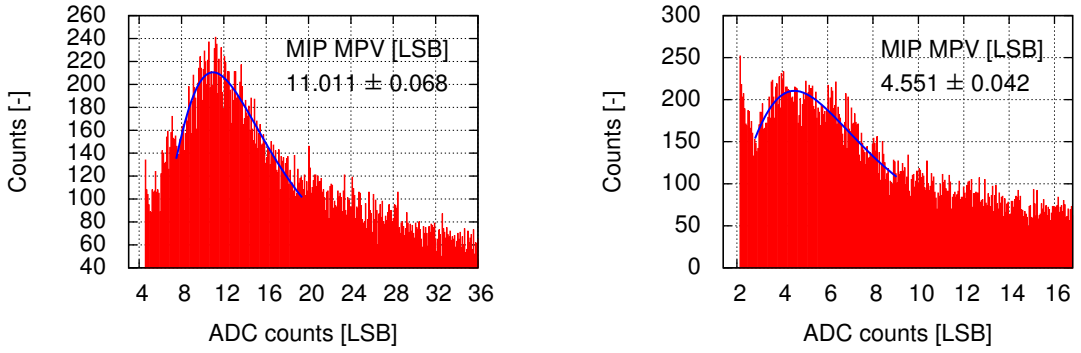


Figure A.20: Channels energy distribution with convolution of Landau and Gauss distributions fitted to the muon peak for board IDN63 in the third configuration.



a) MOS feedback b) R feedback

Figure A.21: Channels energy distribution with convolution of Landau and Gauss distributions fitted to the muon peak for board IDN64 in the third configuration.



a) MOS feedback b) R feedback

Figure A.22: Channels energy distribution with convolution of Landau and Gauss distributions fitted to the muon peak for board IDN67 in the third configuration.

A.3 Energy spectra

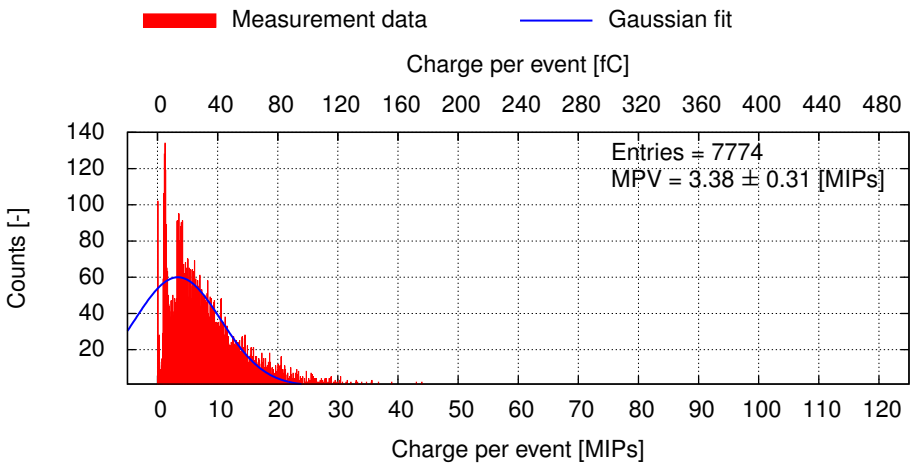


Figure A.23: Spectrum of energy deposited in the whole instrumented area of board IDN63 (sensor S0) in the first configuration after the muons cut procedure.

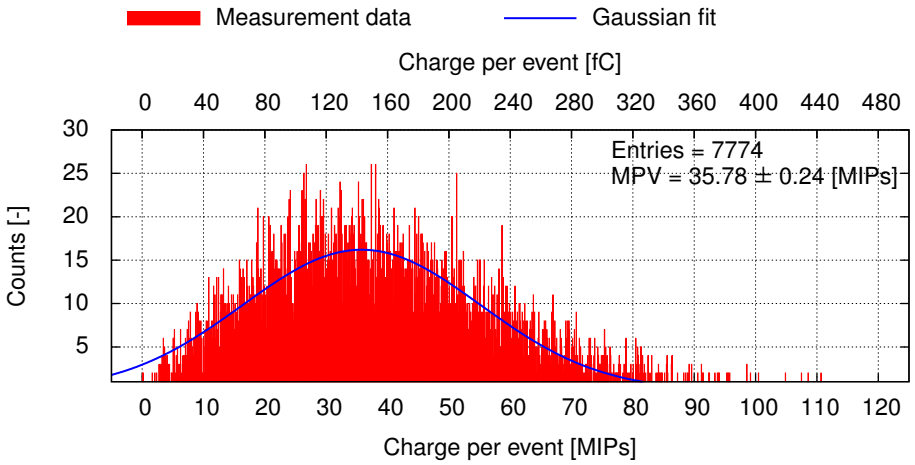


Figure A.24: Spectrum of energy deposited in the whole instrumented area of board IDN64 (sensor S1) in the first configuration after the muons cut procedure.

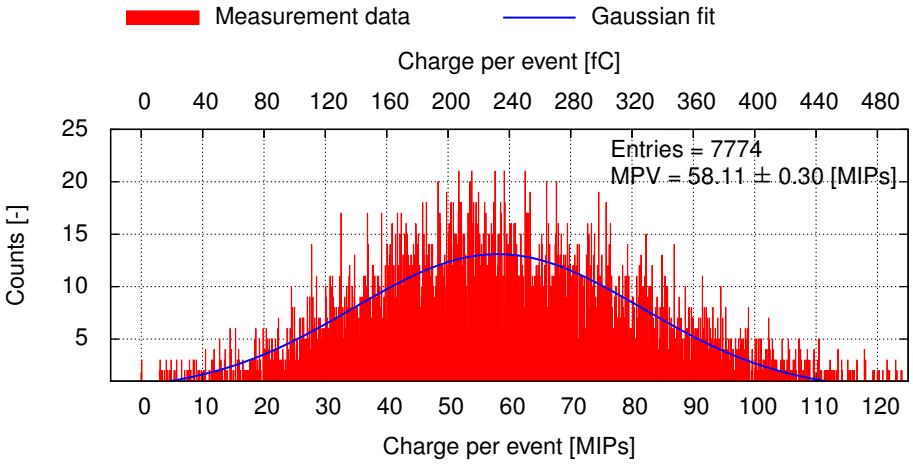


Figure A.25: Spectrum of energy deposited in the whole instrumented area of board IDN67 (sensor S2) in the first configuration after the muons cut procedure.

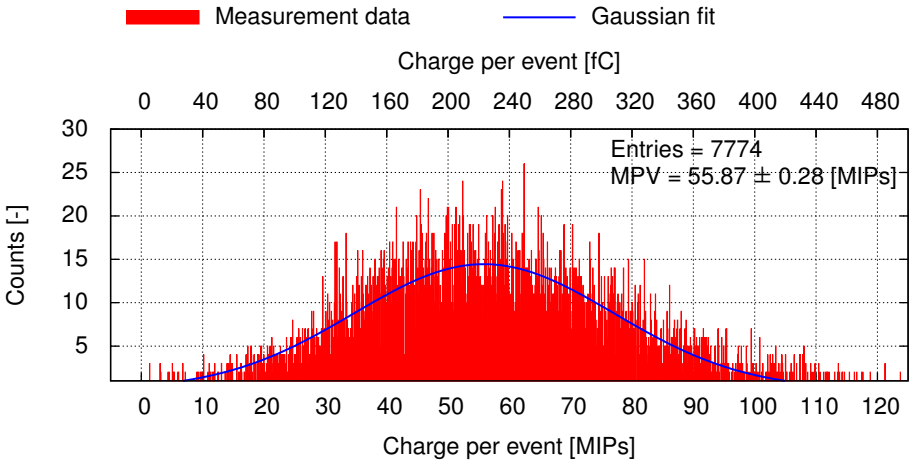


Figure A.26: Spectrum of energy deposited in the whole instrumented area of board IDN76 (sensor S3) in the first configuration after the muons cut procedure.

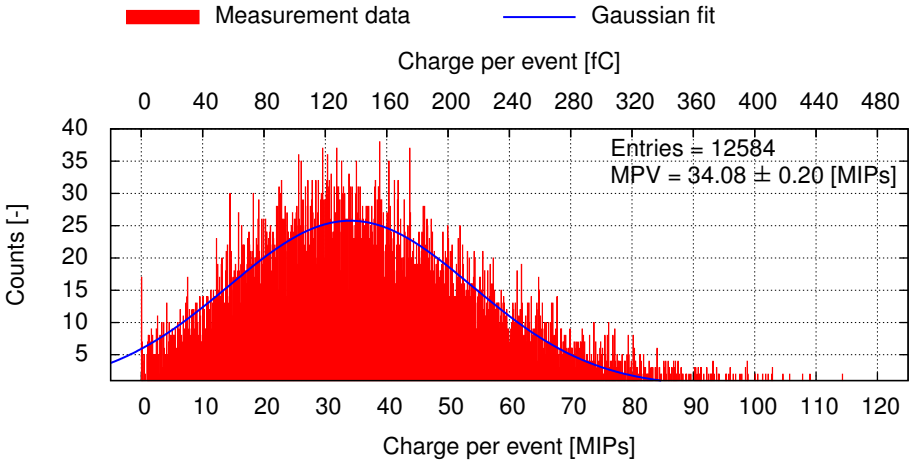


Figure A.27: Spectrum of energy deposited in the whole instrumented area of board IDN63 (sensor S0) in the second configuration after the muons cut procedure.

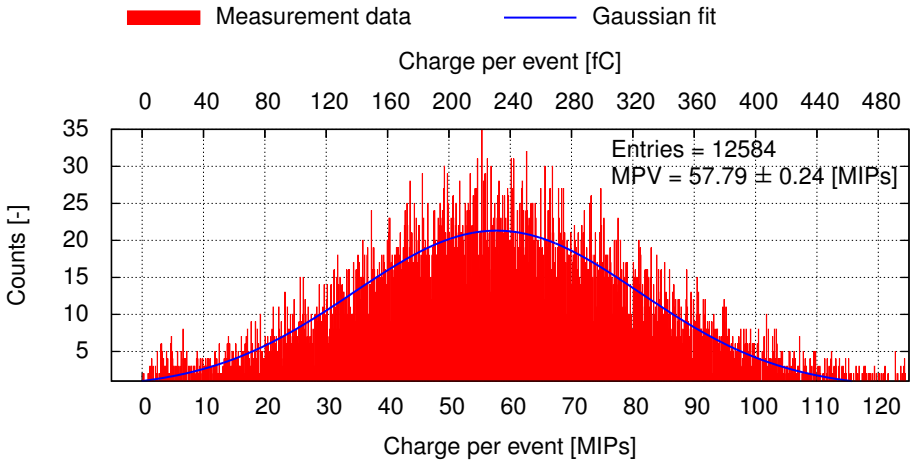


Figure A.28: Spectrum of energy deposited in the whole instrumented area of board IDN64 (sensor S1) in the second configuration after the muons cut procedure.

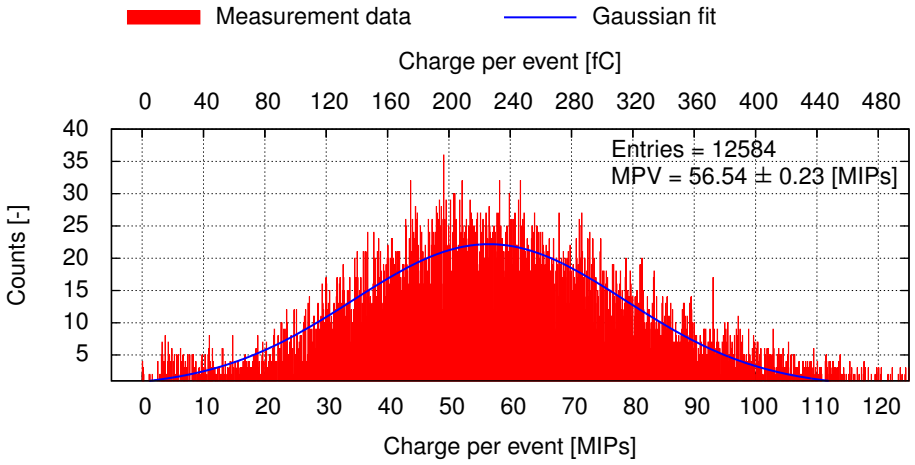


Figure A.29: Spectrum of energy deposited in the whole instrumented area of board IDN67 (sensor S2) in the second configuration after the muons cut procedure.

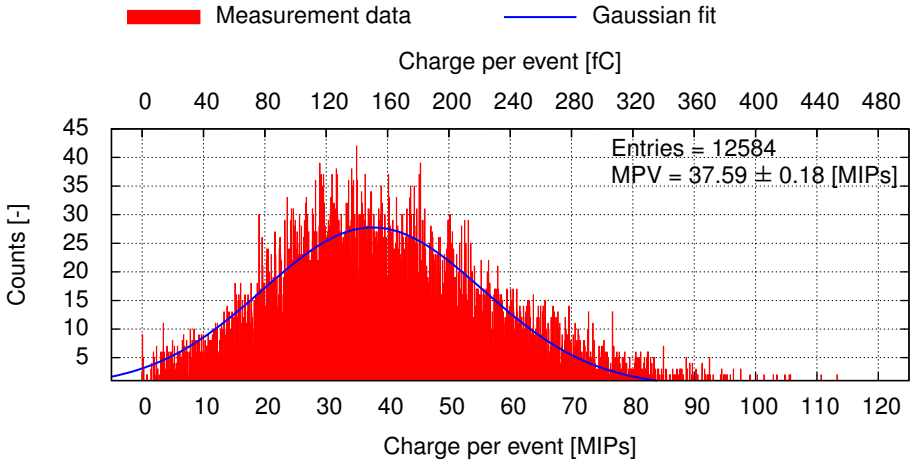


Figure A.30: Spectrum of energy deposited in the whole instrumented area of board IDN76 (sensor S3) in the second configuration after the muons cut procedure.

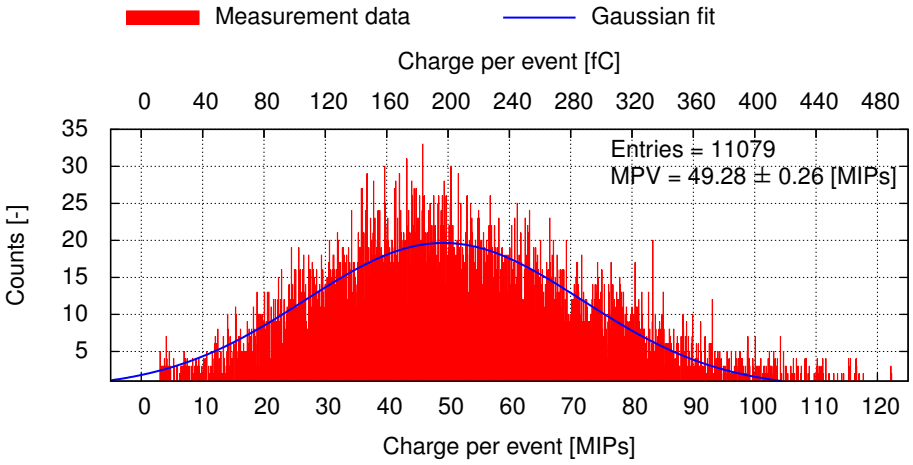


Figure A.31: Spectrum of energy deposited in the whole instrumented area of board IDN63 (sensor S0) in the third configuration after the muons cut procedure.

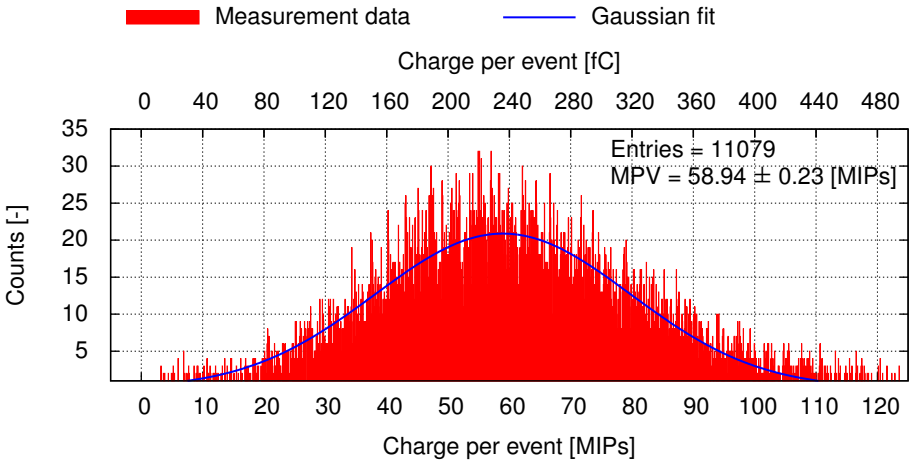


Figure A.32: Spectrum of energy deposited in the whole instrumented area of board IDN64 (sensor S1) in the third configuration after the muons cut procedure.

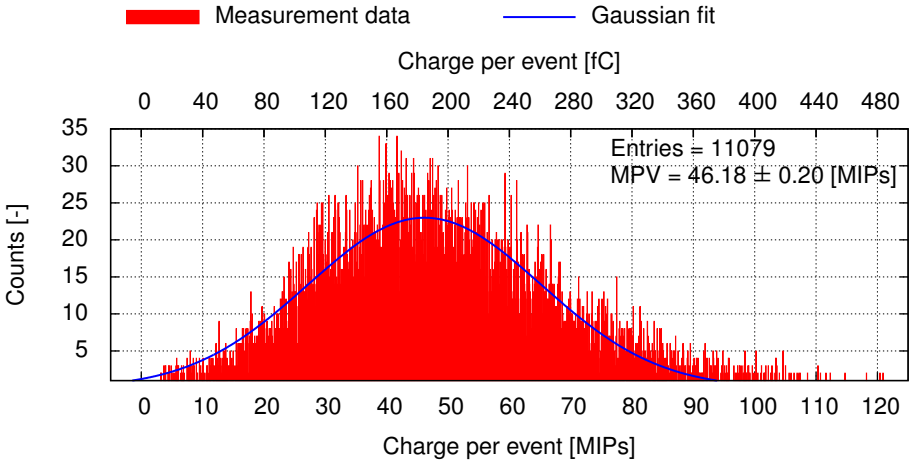


Figure A.33: Spectrum of energy deposited in the whole instrumented area of board IDN67 (sensor S2) in the third configuration after the muons cut procedure.

Appendix B

Detailed ADC prototypes measurement results

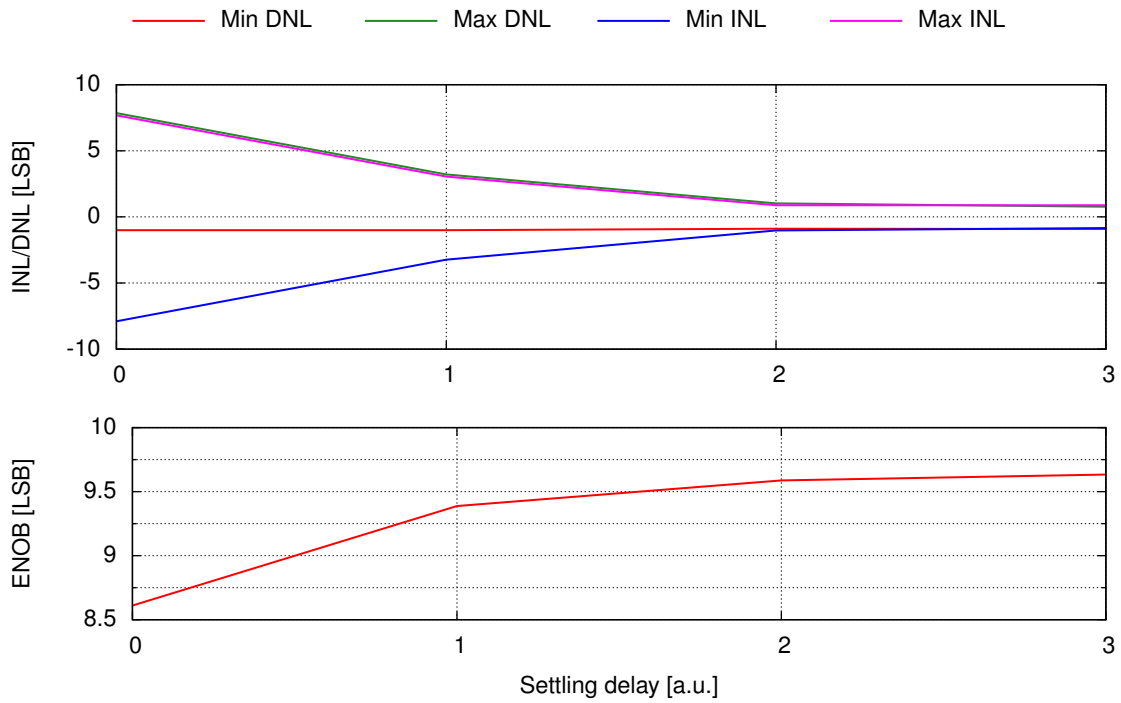


Figure B.1: Static measurement result of the ADC_A_V1 prototype versus settling delay at 10 MHz sampling frequency.

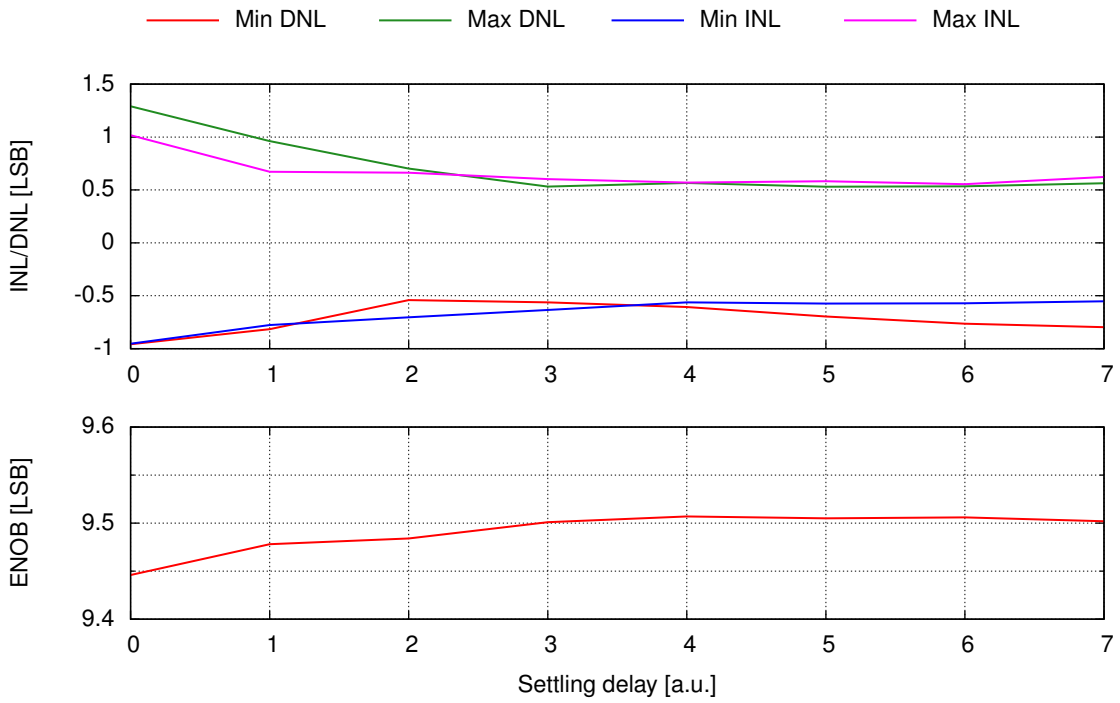


Figure B.2: Static measurement result of the ADC_A_V2 prototype versus settling delay at 10 MHz sampling frequency.

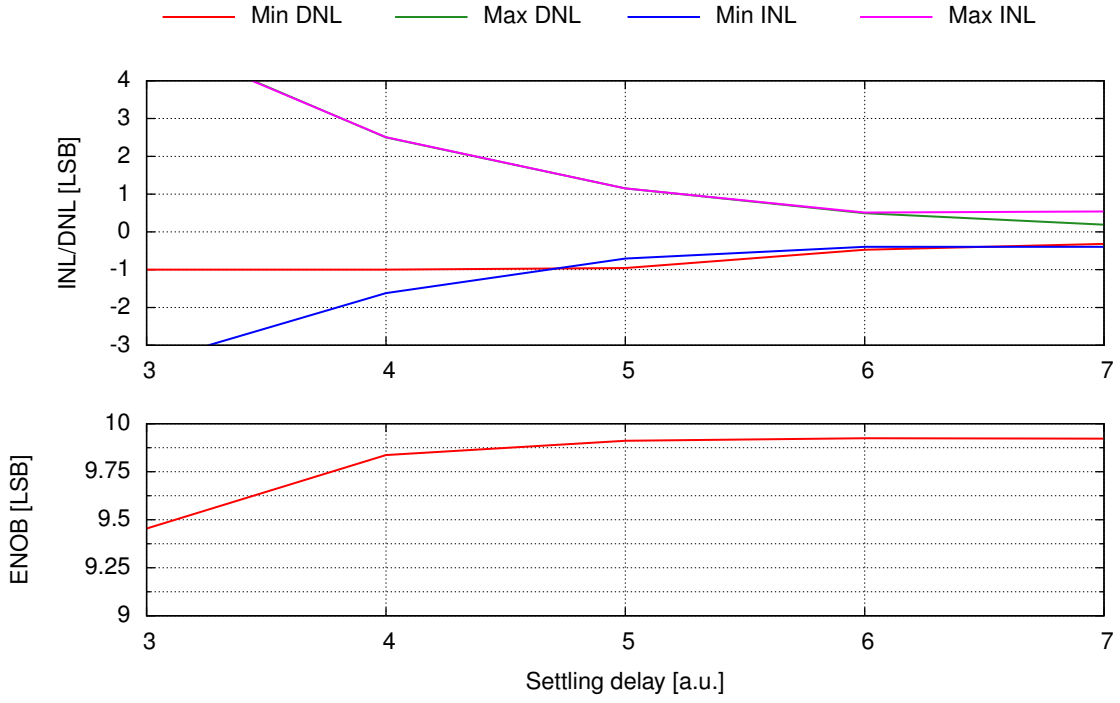


Figure B.3: Static measurement result of the ADC_B_V1 prototype versus settling delay at 10 MHz sampling frequency.

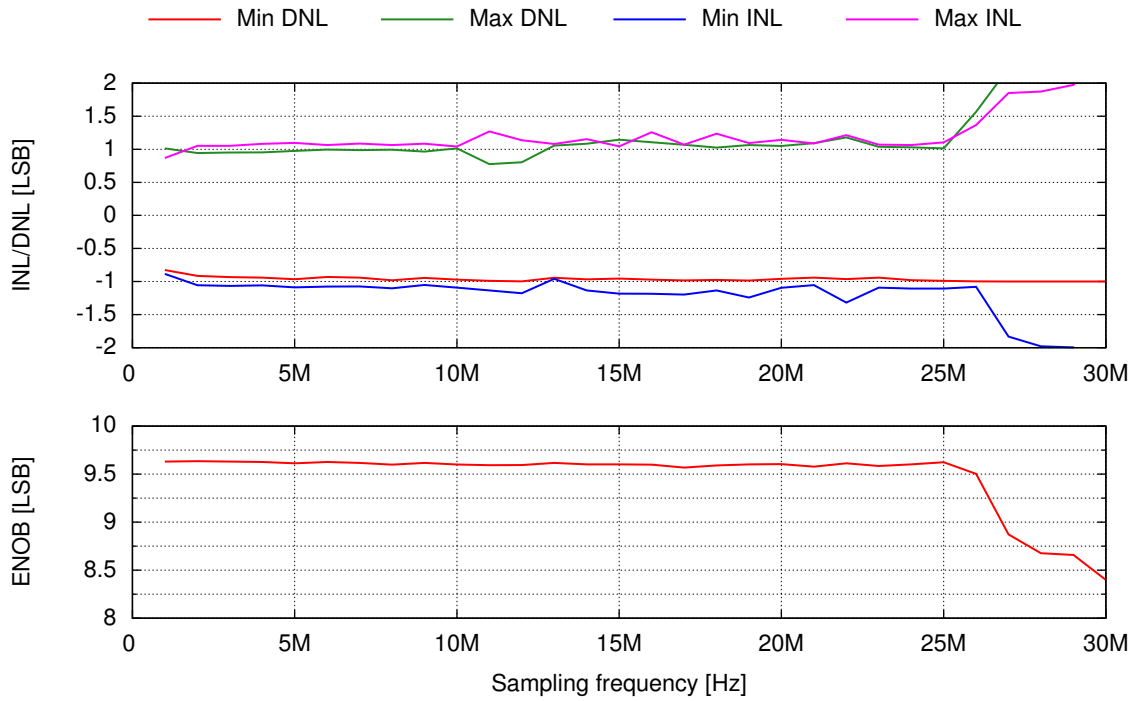


Figure B.4: Static measurement result of the ADC_A_V1 prototype versus sampling frequency with disabled delay thyristor circuit.

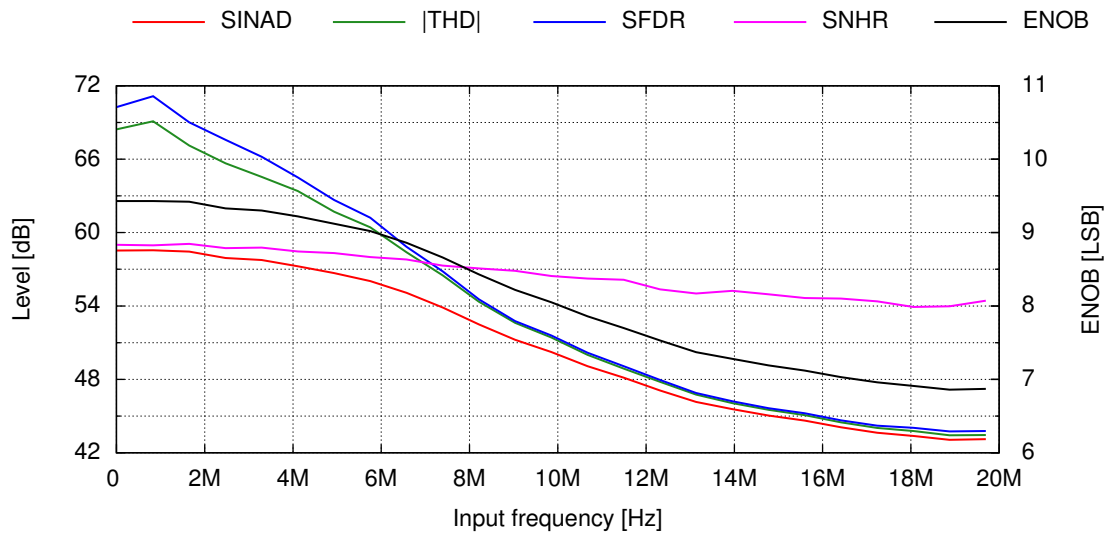


Figure B.5: Dynamic measurement result of the ADC_A_V1 prototype versus input frequency at 40 MHz sampling frequency with enabled delay thyristor circuit.

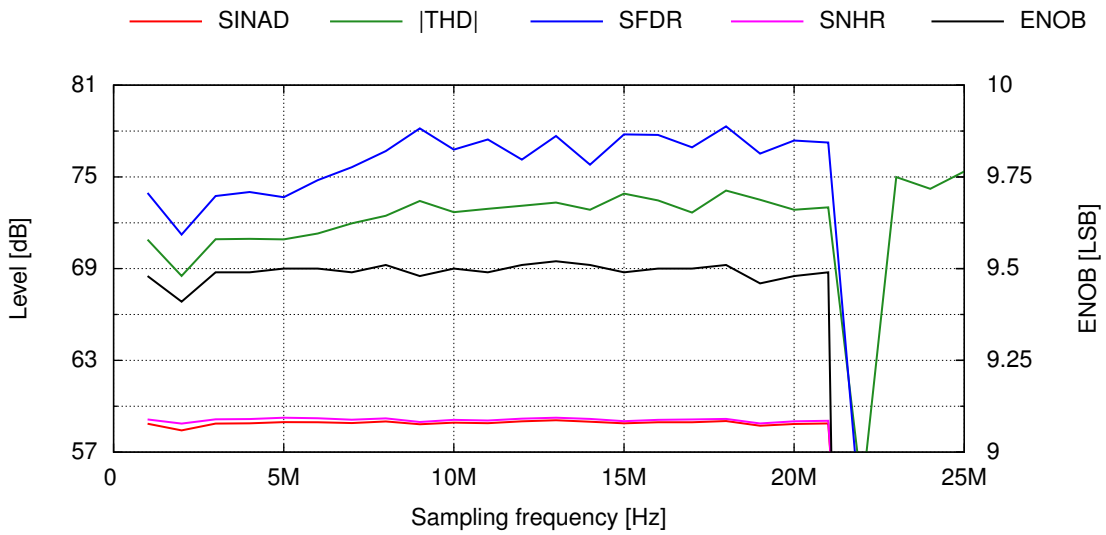


Figure B.6: Dynamic measurement result of the ADC_A_V1 prototype versus sampling frequency at 0.1 Nyquist input sine frequency with disabled delay thyristor circuit.

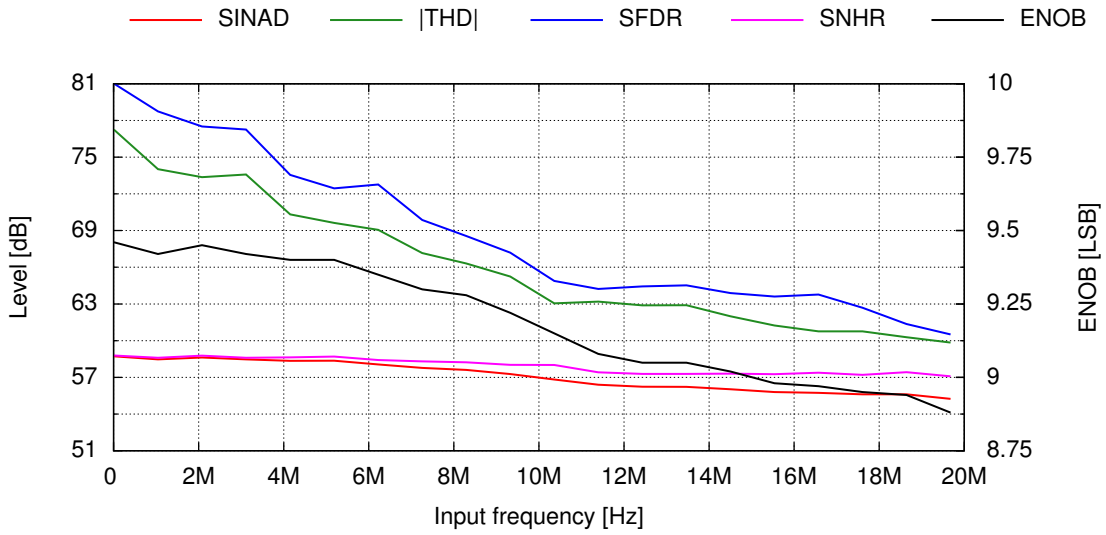


Figure B.7: Dynamic measurement result of the ADC_B_V1 prototype versus input frequency at 40 MHz sampling frequency.