

1. Clocking Errata When Using the TEMAC with Bus Clock Not Set to 125MHz

When generating a design in BSB that uses the V5FXT hard TEMAC core, the Place & Route tool cannot route the 100MHz input clock signal to the PLL to generate various clock signals for the design, if the **Bus Clock** is set to any frequency other than 125MHz (the 125MHz happens to be the frequency of the TEMAC clock input).

So, if the Bus Clock and the TEMAC clock input match (125MHz clock input), then there are no Place & Route issues; however, if the Bus Clock is not set to 125MHz, you must do the following to resolve the Place & Route issue (you are simply adding a BUFG to the 100MHz clock input prior to routing it to the PLL).

- 1) Copy the **edk_bufg_v1_00_a** folder from the Avnet XBD zip file to the **/pcores** folder of your BSB design.
- 2) Edit the **system.mhs** file of the BSB design and add the **edk_bufg_v1_00_a** IP core to the design as shown in the following figure (the line numbers may not match your design).

```
239
240 BEGIN edk_bufg
241     PARAMETER INSTANCE = clk_in_bufg
242     PARAMETER HW_VER = 1.00.a
243     PORT in_clk = dcm_clk_s
244     PORT out_clk = dcm_clk_s_bufg
245 END
246
```

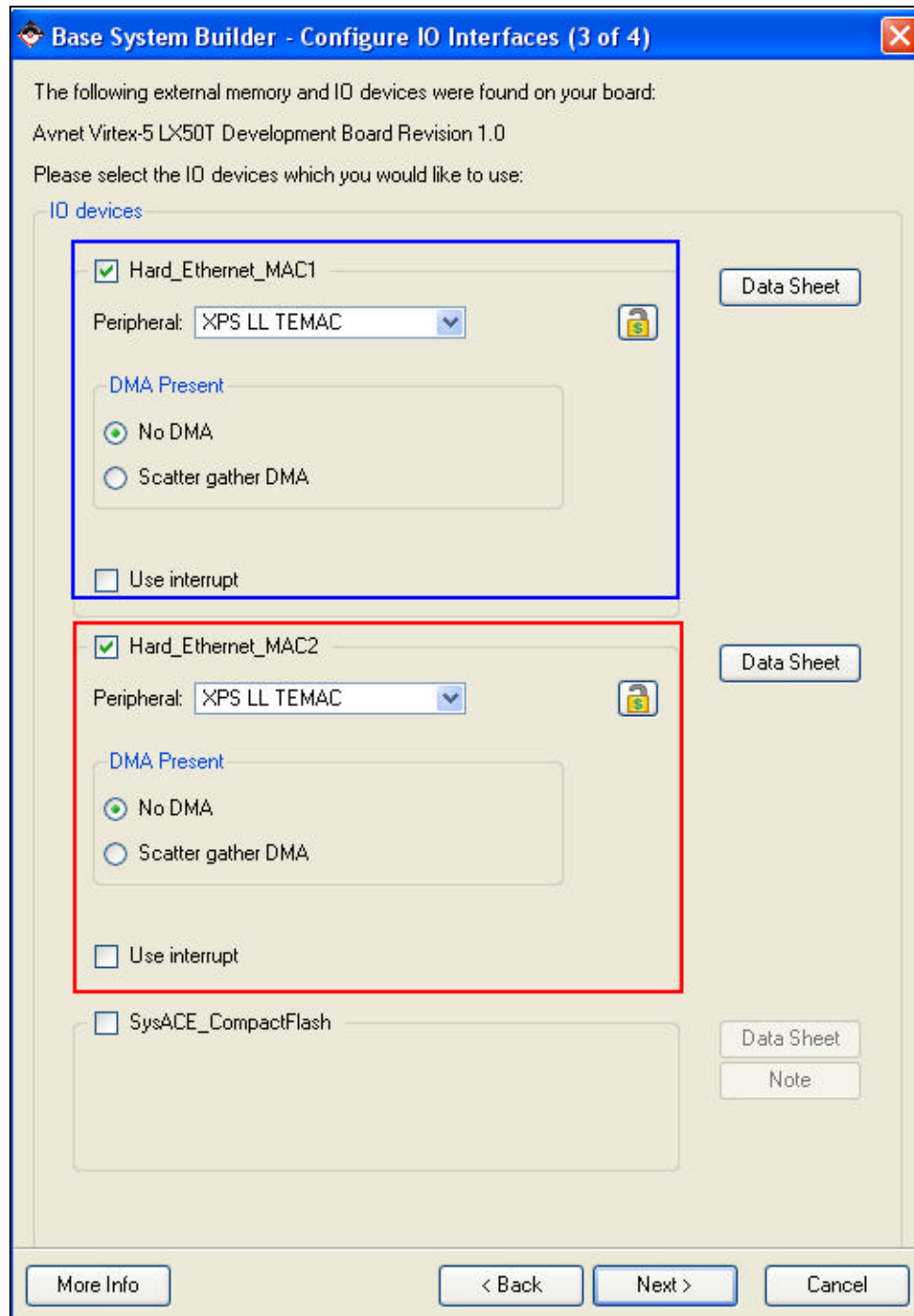
- 3) Edit the **clock_generator** IP section of the **system.mhs** file and set the **CLKIN** port to the **dcm_clk_s_bufg** signal as shown in the following figure (the line numbers may not match your design).

```
280 PORT CLKOUT0 = proc_clk_s
281 PORT CLKOUT1 = ppc440_0_CPMINTERCONNECTCLK
282 PORT CLKOUT2 = sys_clk_s
283 PORT CLKOUT3 = sys_clk_s90
284 PORT CLKOUT4 = clk_200mhz_s
285 PORT CLKOUT5 = temac_clk_s
286 PORT CLKOUT6 = DDR2_SDRAM_16Mx32_mi_mccclkdiv2
287 PORT CLKIN = dcm_clk_s_bufg
288 PORT LOCKED = dcm_all_locked
289 PORT RST = net_gnd
290 END
```

- 4) Save and close the **system.mhs** file. You can now implement the design.

Avnet V5LXT/SXT PCIe Development Board BSB Errata

The Avnet V5LXT/SXT PCIe development board (V5LX50T, V5LX110T, V5SX50T, and V5SX95T versions) provides two on-board 10/100/1000 PHY devices. In the EDK 10.1.02 BSB, user has the option of using a soft Ethernet MAC (default option) or the Virtex-5 integrated hard TEMAC core to connect to the on-board 10/100/1000 PHY devices as shown in the following BSB screen shot for the Avnet V5LX50T development board.



The screenshot shows the 'Base System Builder - Configure IO Interfaces (3 of 4)' window. It displays the configuration for two Ethernet MACs, Hard_Ethernet_MAC1 and Hard_Ethernet_MAC2. Both are checked and configured with 'XPS LL TEMAC' as the peripheral. The 'DMA Present' section for both has 'No DMA' selected. The 'Use interrupt' checkbox is unchecked for both. A 'SysACE_CompactFlash' option is also visible but unchecked. The window includes 'Data Sheet' and 'Note' buttons for each device, and navigation buttons at the bottom.

Base System Builder - Configure IO Interfaces (3 of 4)

The following external memory and IO devices were found on your board:
Avnet Virtex-5 LX50T Development Board Revision 1.0

Please select the IO devices which you would like to use:

IO devices

☒ Hard_Ethernet_MAC1

Peripheral: XPS LL TEMAC

DMA Present

☒ No DMA

☐ Scatter gather DMA

☐ Use interrupt

Hard_Ethernet_MAC2

Peripheral: XPS LL TEMAC

DMA Present

☒ No DMA

☐ Scatter gather DMA

☐ Use interrupt

☐ SysACE_CompactFlash

More Info < Back Next > Cancel

If both hard TEMAC cores are used in a design (as shown in the above BSB screen shot), BSB fails to include the following TEMAC ports (shown in the box in the following figure) for the second TEMAC instantiated in the design.

After creating the design using BSB, please open the **system.mhs** file in the XPS GUI, modify the second instance of the TEMAC core to add the missing ports as shown in the following figure, and save the **system.mhs** file prior to implementing your design.

```
303 BEGIN xps_ll_temac
304     PARAMETER INSTANCE = Hard_Ethernet_MAC2
305     PARAMETER HW_VER = 1.01.b
306     PARAMETER C_SPLB_CLK_PERIOD_PS = 7500
307     PARAMETER C_PHY_TYPE = 1
308     PARAMETER C_TEMAC_TYPE = 0
309     PARAMETER C_TEMAC1_ENABLED = 0
310     PARAMETER C_TEMAC0_PHYADDR = 0b00000000000000000000000000000001
311     PARAMETER C_NUM_IDELAYCTRL = 2
312     PARAMETER C_IDELAYCTRL_LOC = IDELAYCTRL_X0Y5-IDELAYCTRL_X1Y1
313     PARAMETER C_BASEADDR = 0x81c20000
314     PARAMETER C_HIGHADDR = 0x81c2ffff
315     BUS_INTERFACE SPLB = mb_plb
316     BUS_INTERFACE LLINK0 = Hard_Ethernet_MAC2llink0
317     PORT TemacPhy_RST_n = fpga_0_Hard_Ethernet_MAC2_TemacPhy_RST_n
318     PORT GMII_TXD_0 = fpga_0_Hard_Ethernet_MAC2_GMII_TXD_0
319     PORT GMII_TX_EN_0 = fpga_0_Hard_Ethernet_MAC2_GMII_TX_EN_0
320     PORT GMII_TX_ER_0 = fpga_0_Hard_Ethernet_MAC2_GMII_TX_ER_0
321     PORT GMII_TX_CLK_0 = fpga_0_Hard_Ethernet_MAC2_GMII_TX_CLK_0
322     PORT GMII_RXD_0 = fpga_0_Hard_Ethernet_MAC2_GMII_RXD_0
323     PORT GMII_RX_DV_0 = fpga_0_Hard_Ethernet_MAC2_GMII_RX_DV_0
324     PORT GMII_RX_ER_0 = fpga_0_Hard_Ethernet_MAC2_GMII_RX_ER_0
325     PORT GMII_RX_CLK_0 = fpga_0_Hard_Ethernet_MAC2_GMII_RX_CLK_0
326     PORT MII_TX_CLK_0 = fpga_0_Hard_Ethernet_MAC2_MII_TX_CLK_0
327     PORT MDC_0 = fpga_0_Hard_Ethernet_MAC2_MDC_0
328     PORT MDIO_0 = fpga_0_Hard_Ethernet_MAC2_MDIO_0
329     PORT GTX_CLK_0 = temac_clk_s
330     PORT REFCLK = clk_200mhz_s
331     PORT LlinkTemac0_CLK = sys_clk_s
332 END
```