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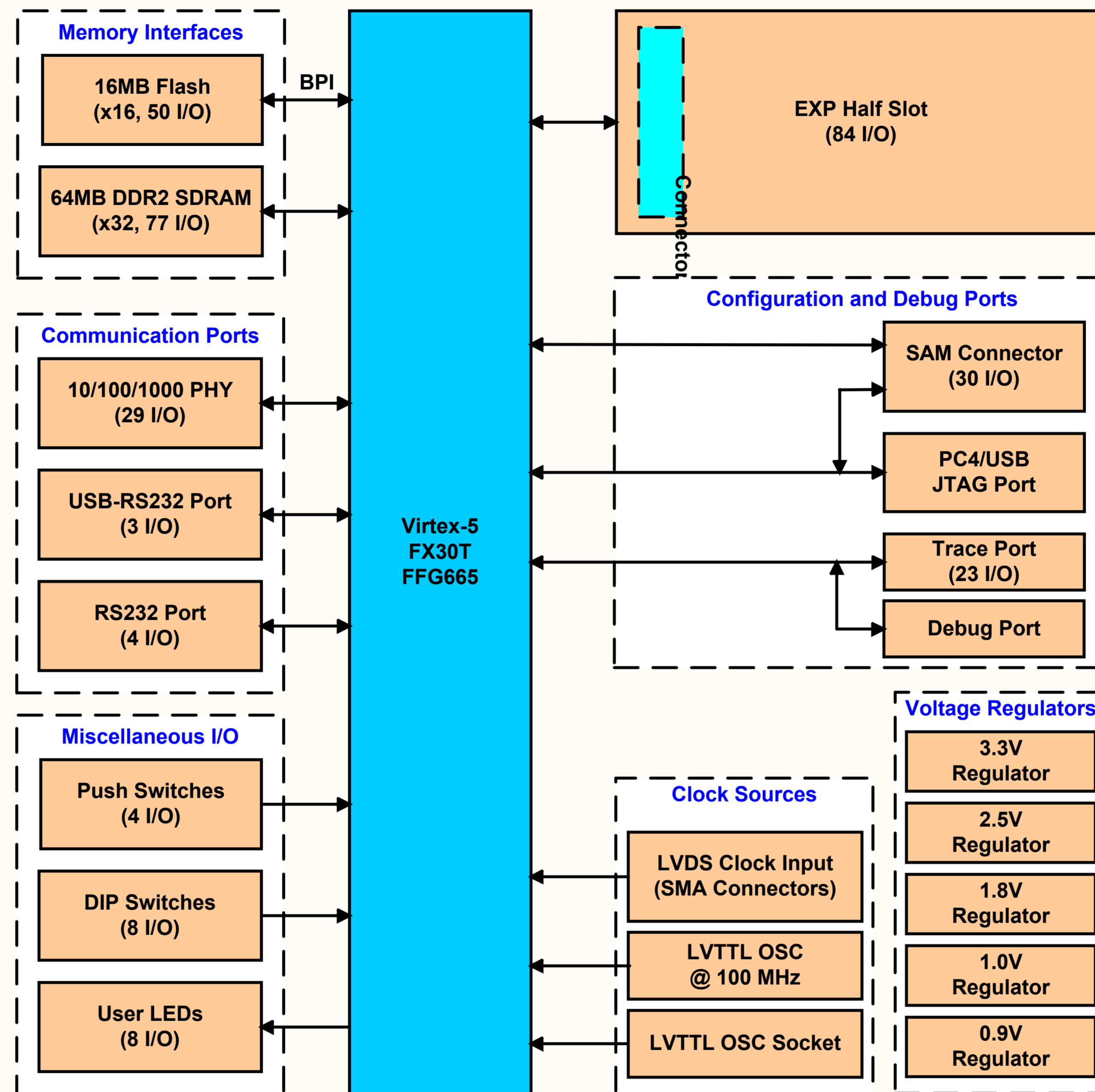


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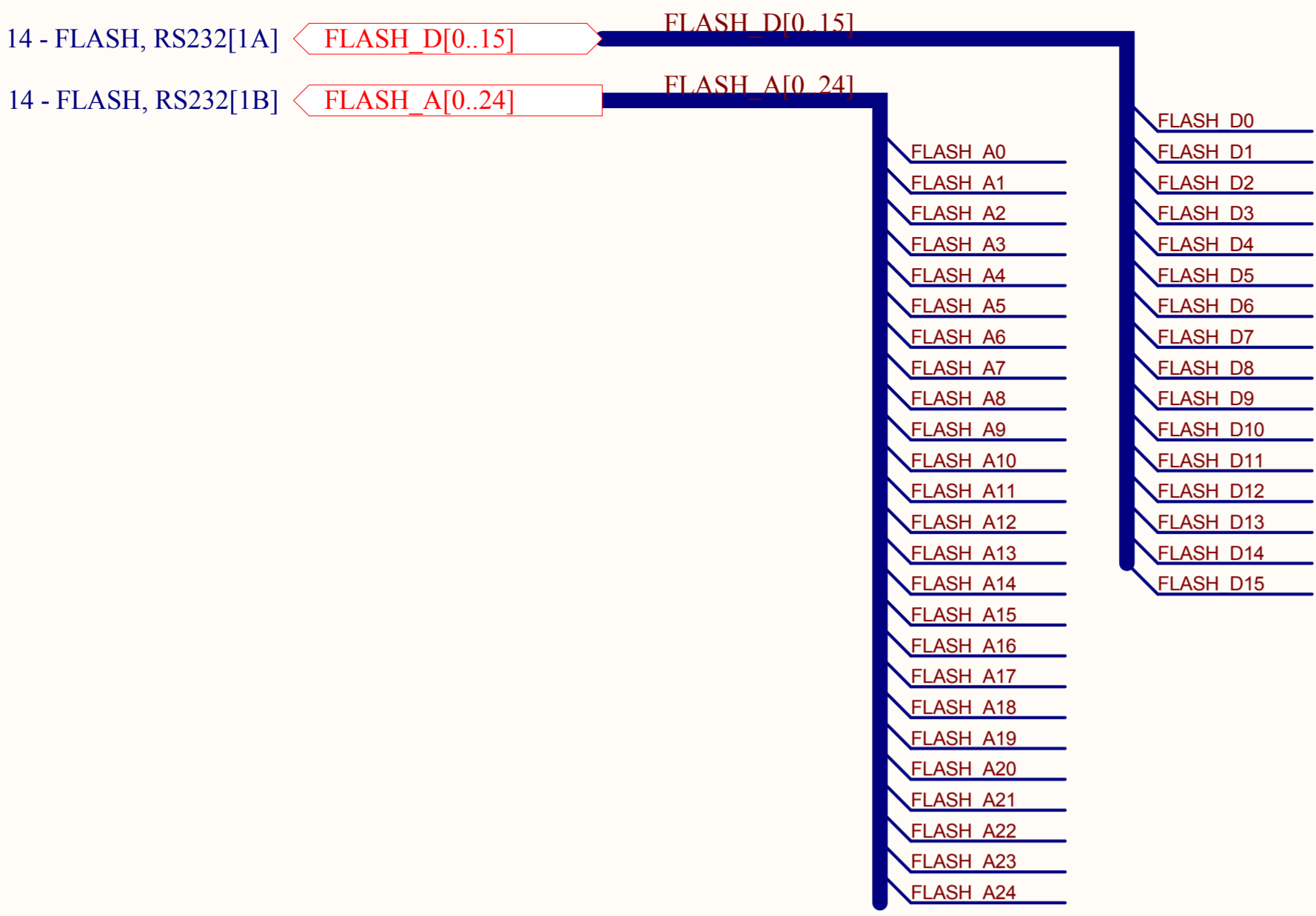
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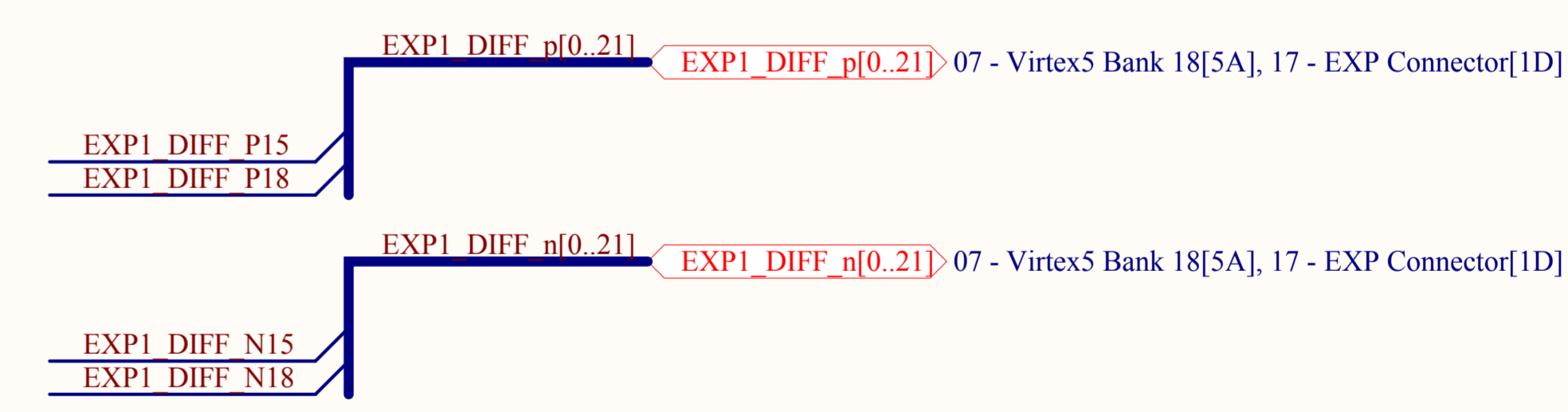
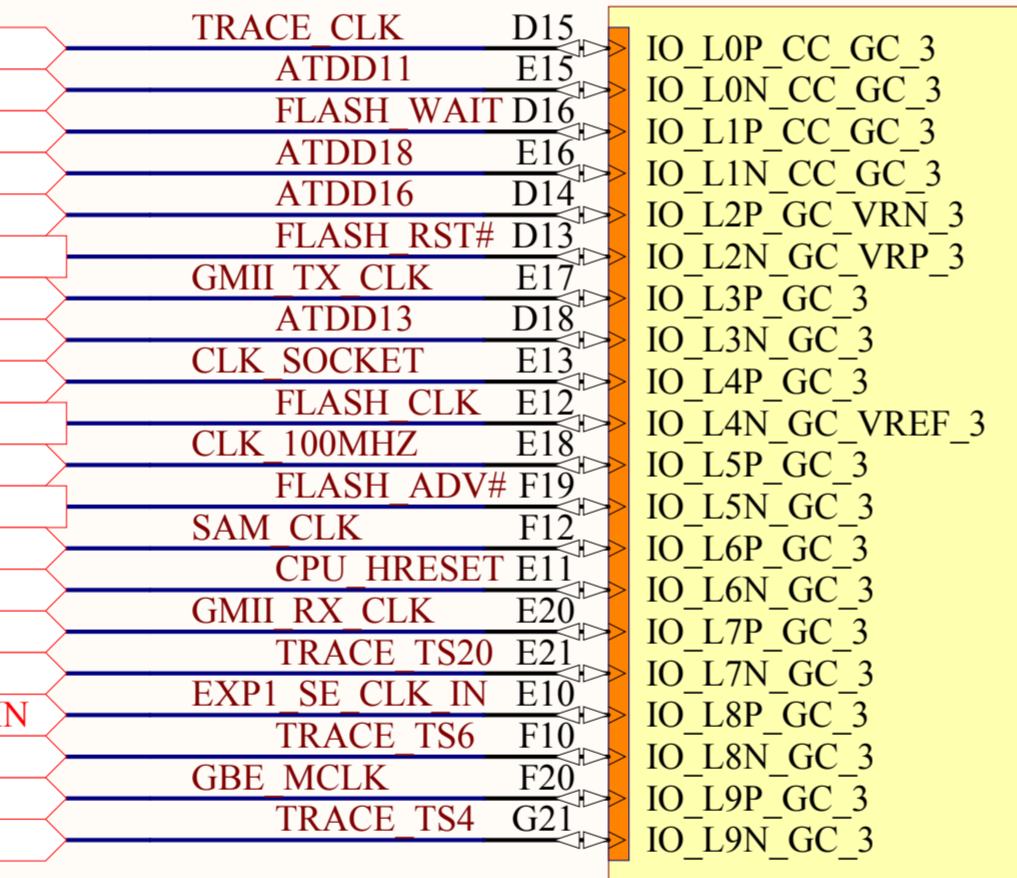
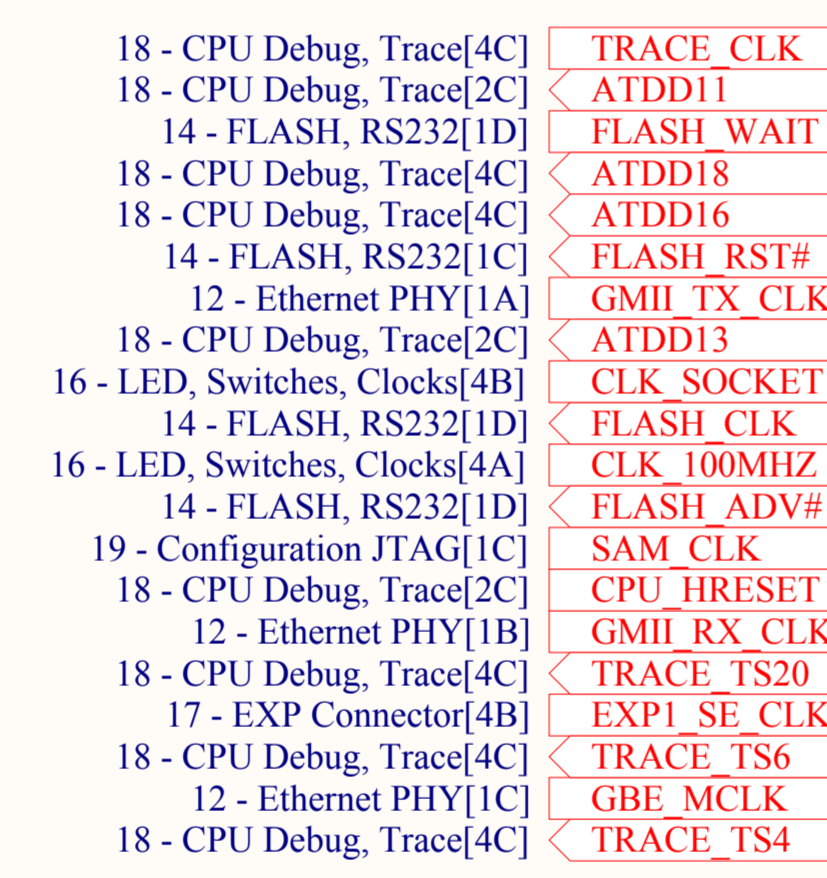
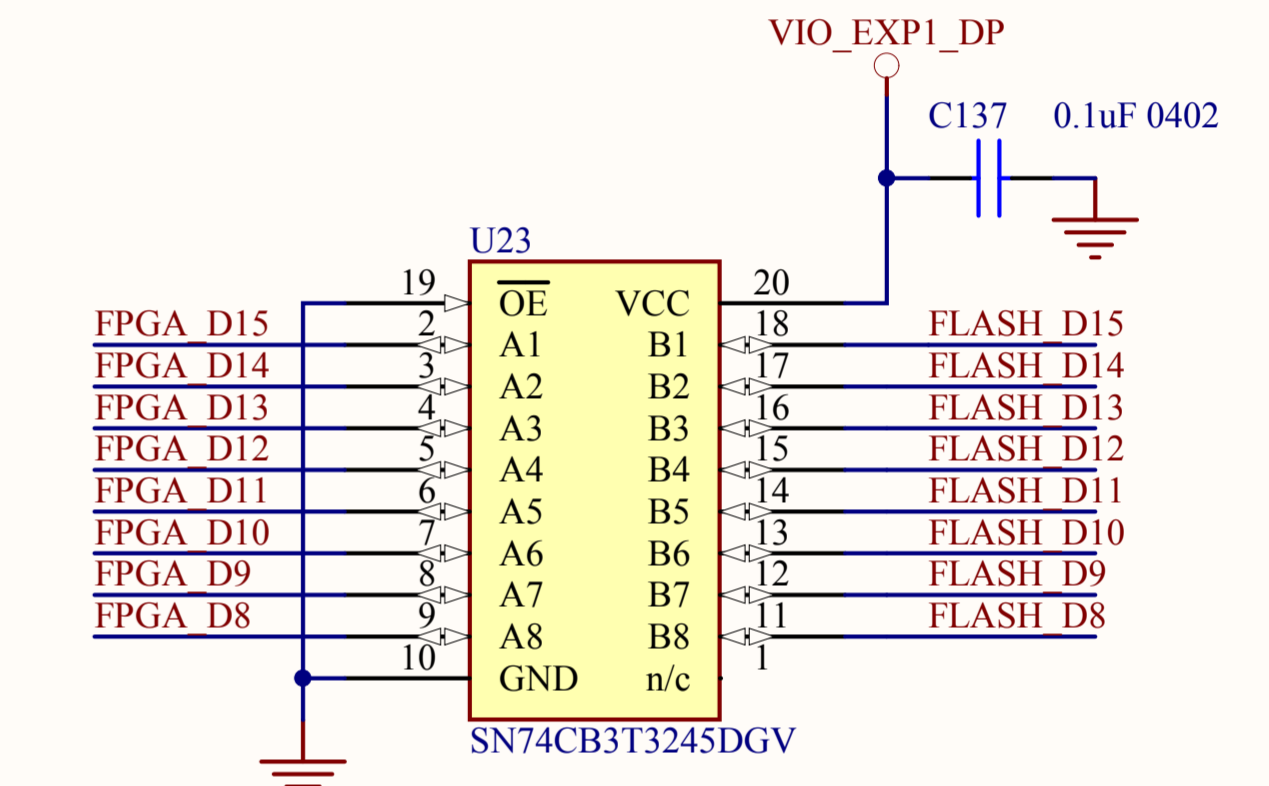
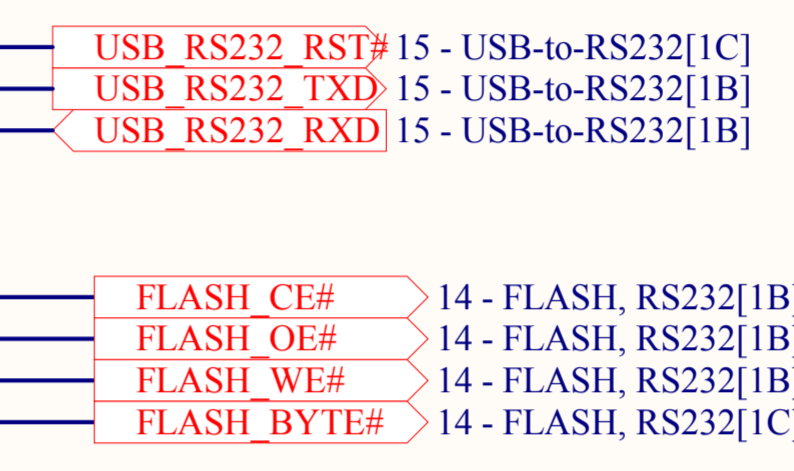
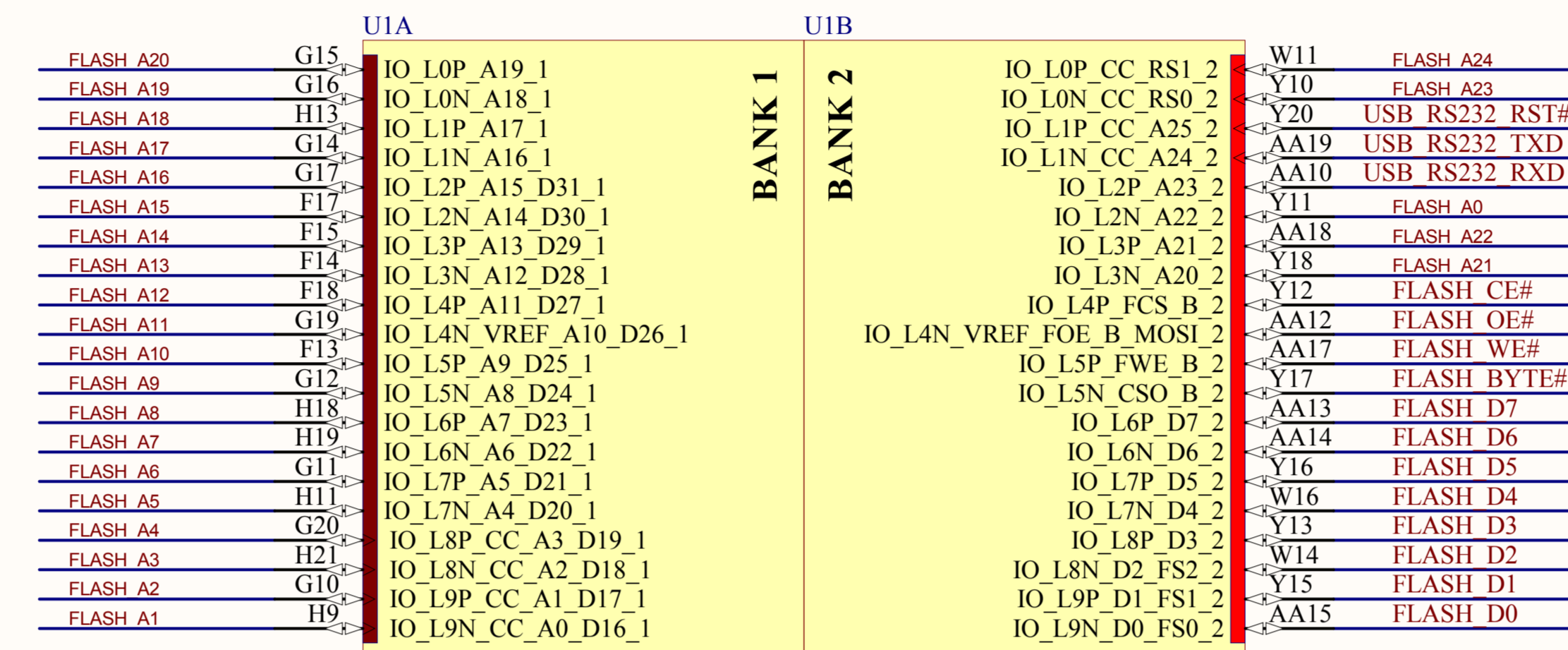
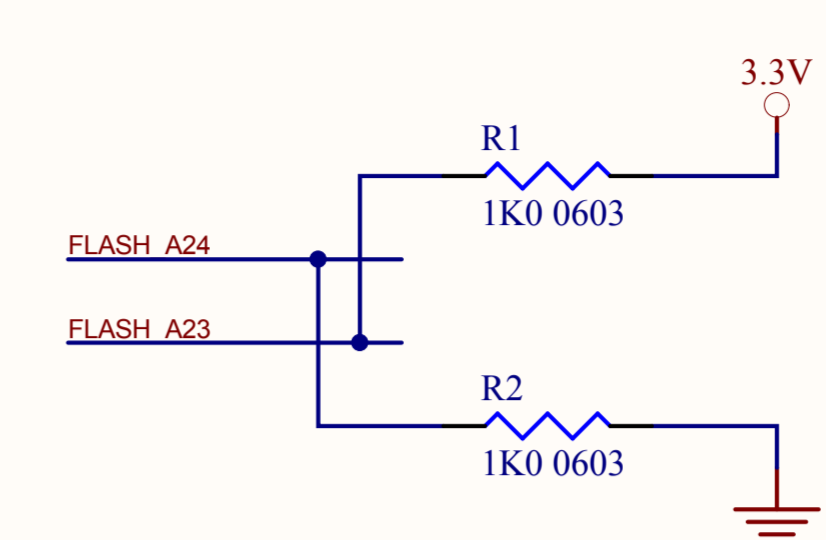
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Title		Rev
Xilinx Virtex-5 FXT Eval Board		Lead Sheet
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Title		Xilinx Virtex-5 FXT Eval Board Block Diagram	
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PU/PD resistors to override initialbitstream selection (BPI mode)



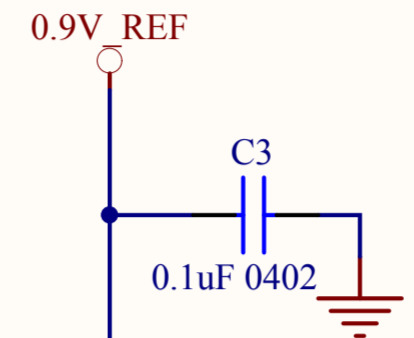
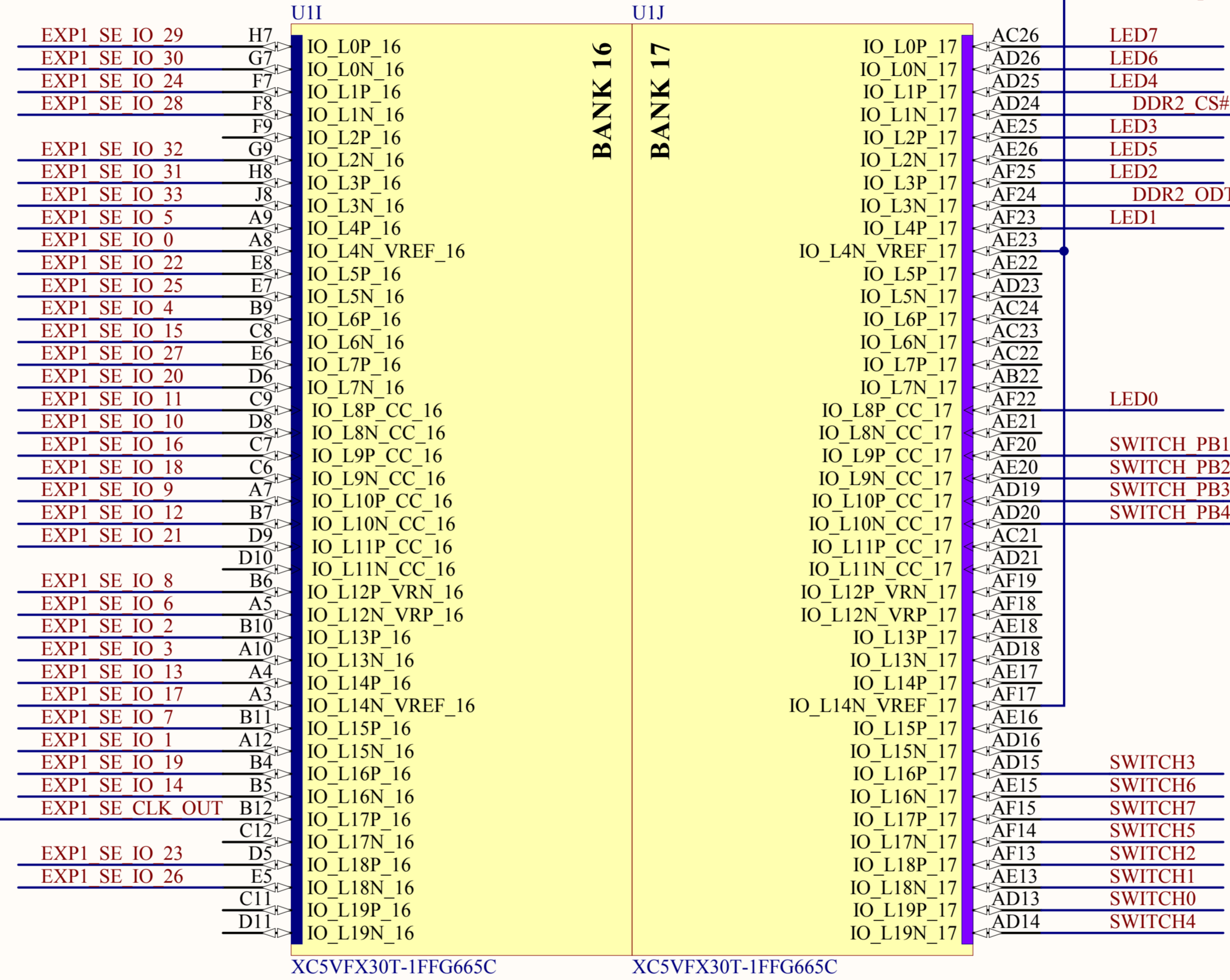
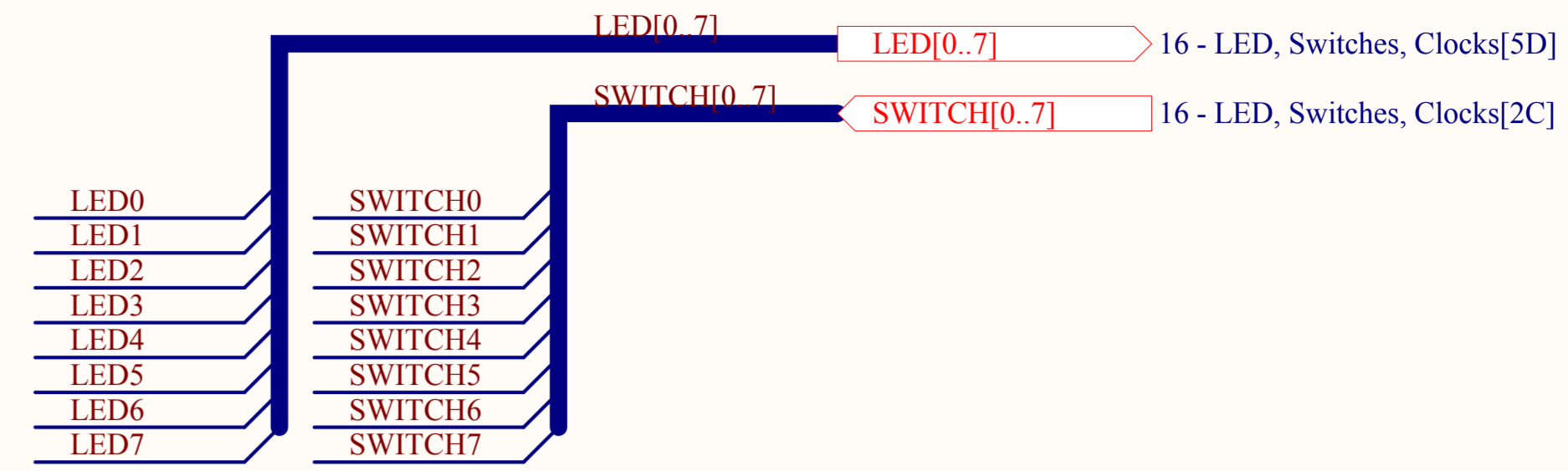
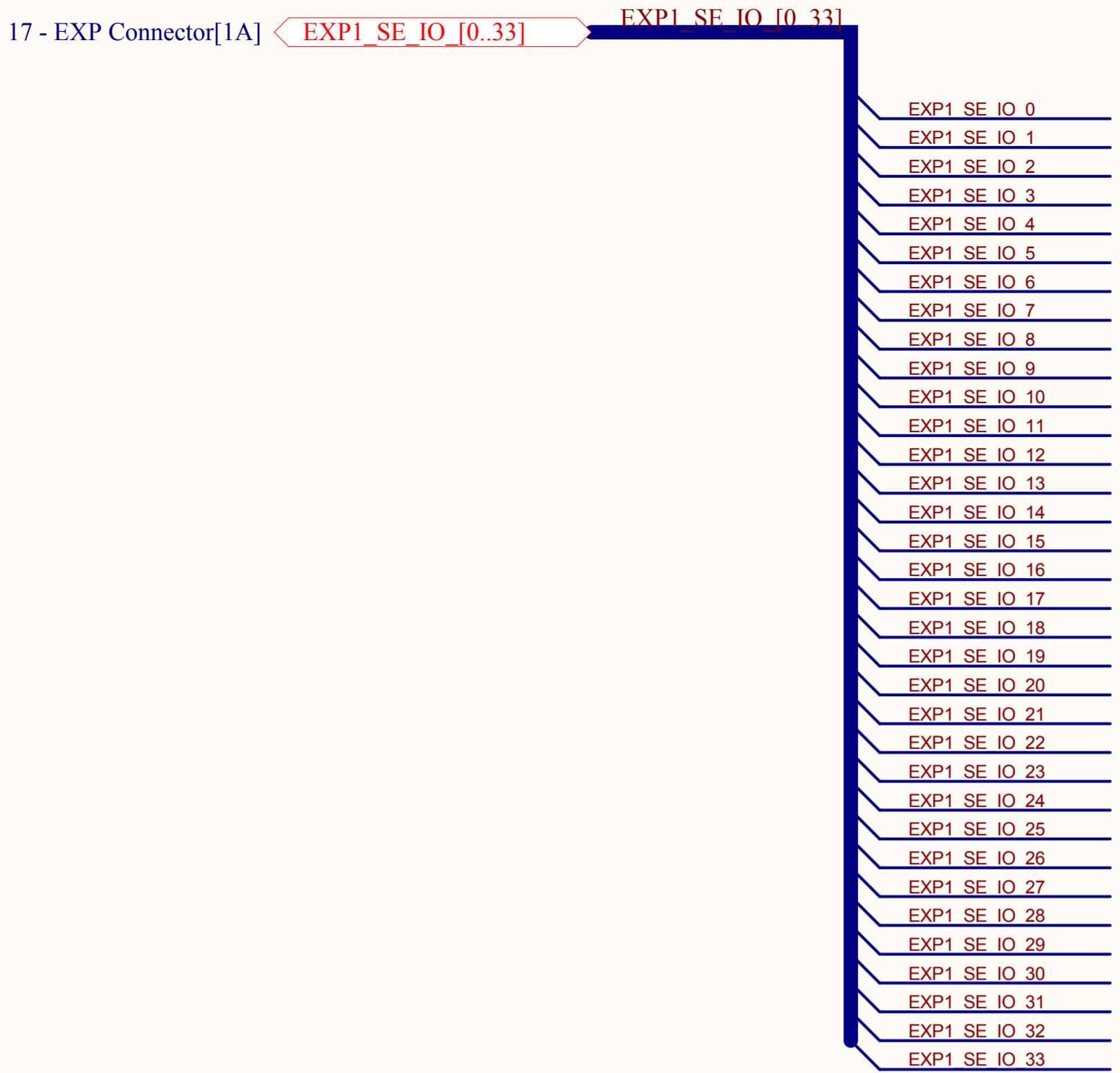
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Title	Xilinx Virtex-5 FXT Eval Board Virtex-5 Banks 1-4
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05 - Virtex5 Banks 13-15[1A], 10 - DDR2 SDRAM[1A] < DDR2_D[0..31] > DDR2_D[0..31]



- CPU HALT# 04 - Virtex5 Banks 11-12[5B], 18 - CPU Debug, Trace[2B]
- CPU TDO 04 - Virtex5 Banks 11-12[5B], 18 - CPU Debug, Trace[2A]
- CPU TCK 04 - Virtex5 Banks 11-12[5B], 18 - CPU Debug, Trace[2B]
- CPU TMS 04 - Virtex5 Banks 11-12[5B], 18 - CPU Debug, Trace[2B]

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Xilinx Virtex-5 FXT Eval Board		
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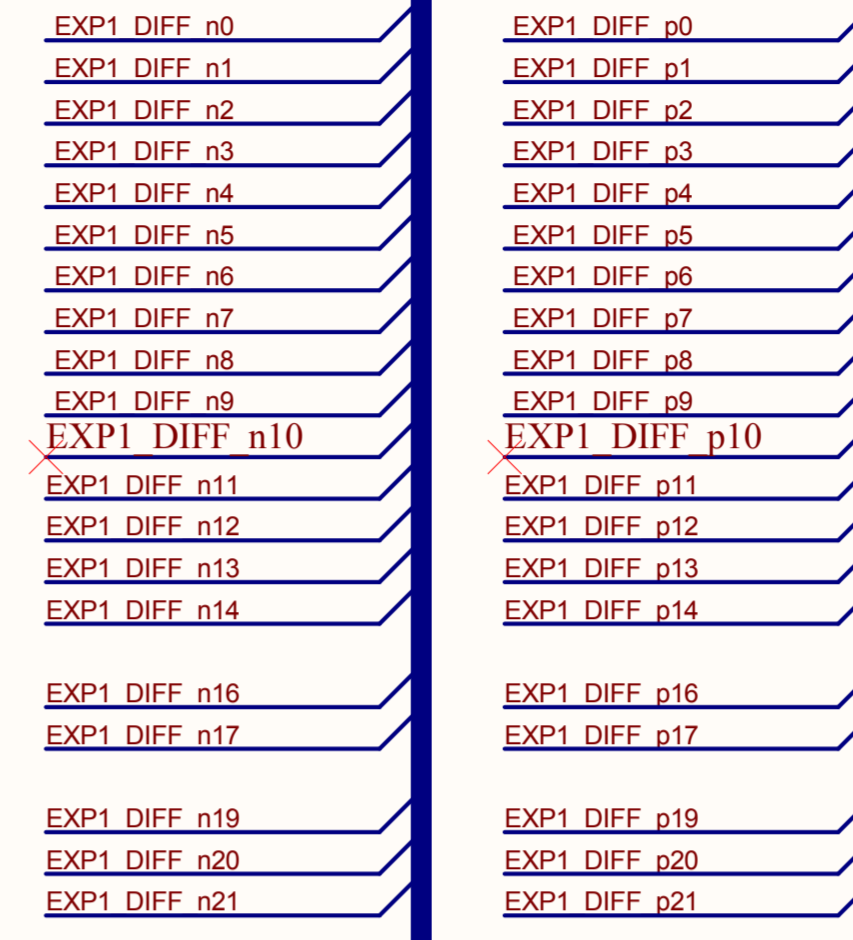
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Size	Document Number Rev
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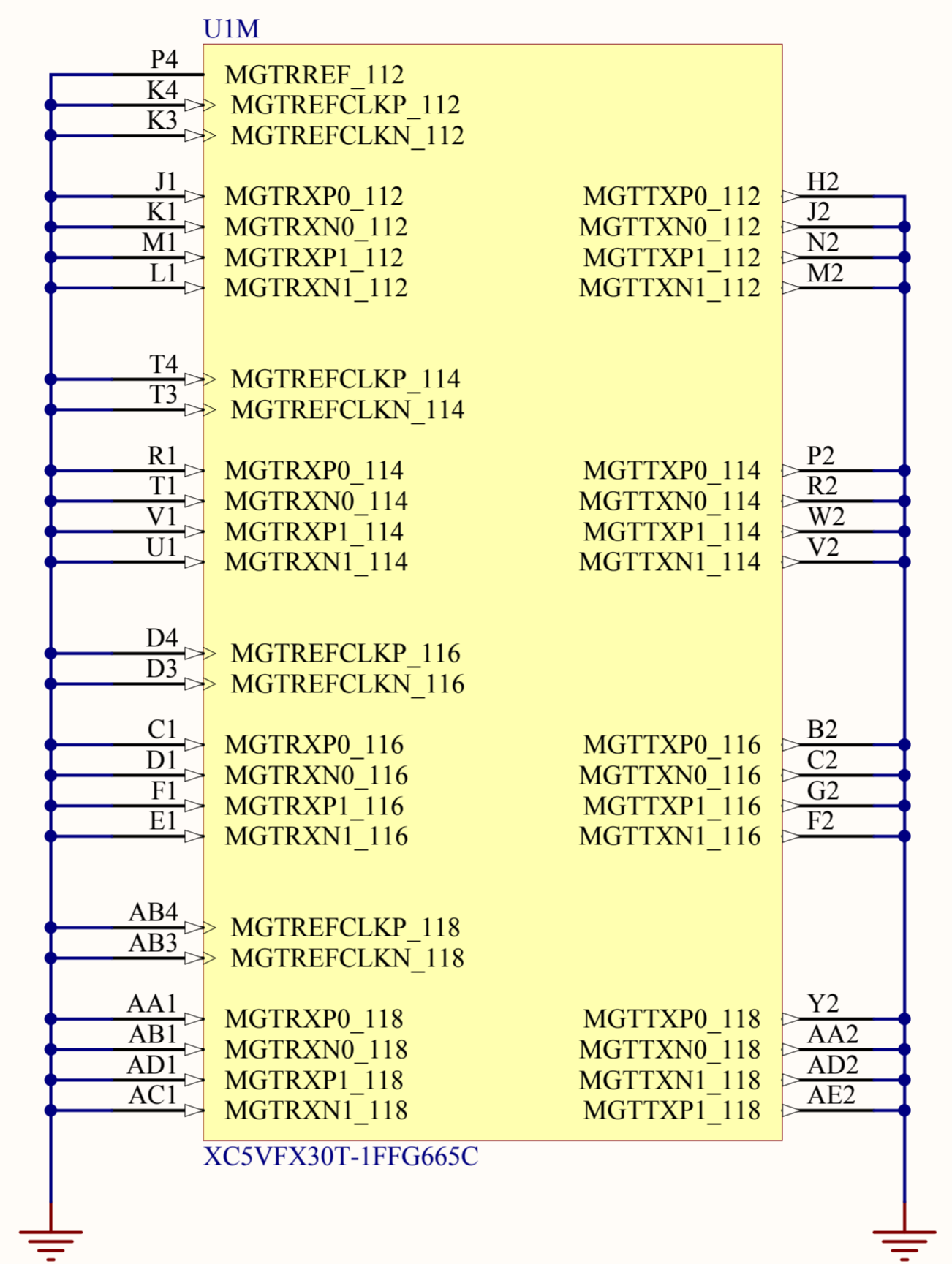
BANK 18

IO_L0P_18	AF12	EXP1 DIFF P1	
IO_L0N_18	AE12	EXP1 DIFF N1	
IO_L1P_18	V8	EXP1 DIFF P21	
IO_L1N_18	V9	EXP1 DIFF N21	
IO_L2P_18	AE11	EXP1 DIFF P3	
IO_L2N_18	AD11	EXP1 DIFF N3	
IO_L3P_18	W9	EXP1 DIFF P20	
IO_L3N_18	W8	EXP1 DIFF N20	
IO_L4P_18	AD10	EXP1 DIFF P5	
IO_L4N_VREF_18	AE10	EXP1 DIFF N5	
IO_L5P_18	V7	EXP1 DIFF P19	
IO_L5N_18	V8	EXP1 DIFF N19	
IO_L6P_18	AF9	EXP1 DIFF P0	
IO_L6N_18	AF10	EXP1 DIFF N0	
IO_L7P_18	AA7	EXP1 DIFF P16	
IO_L7N_18	AA8	EXP1 DIFF N16	
IO_L8P_CC_18	AF8	EXP1 DIFF P2	
IO_L8N_CC_18	AF8	EXP1 DIFF N2	
IO_L9P_CC_18	AA5	EXP1 DIFF P17	
IO_L9N_CC_18	AB5	EXP1 DIFF N17	
IO_L10P_CC_18	AB6	EXP1 RCLK DIFF p	
IO_L10N_CC_18	AB7	EXP1 RCLK DIFF n	
IO_L11P_CC_18	AE8	EXP1 DIFF P6	
IO_L11N_CC_18	AE7	EXP1 DIFF N6	
IO_L12P_VRN_18	AC6	EXP1 DIFF P11	
IO_L12N_VRP_18	AD5	EXP1 DIFF N11	
IO_L13P_18	AE6	EXP1 DIFF P9	
IO_L13N_18	AF5	EXP1 DIFF N9	
IO_L14P_18	AE5	EXP1 DIFF P13	
IO_L14N_VREF_18	AD4	EXP1 DIFF N13	
IO_L15P_18	AF4	EXP1 DIFF P4	
IO_L15N_18	AF3	EXP1 DIFF N4	
IO_L16P_18	AD6	EXP1 DIFF P12	
IO_L16N_18	AC7	EXP1 DIFF N12	
IO_L17P_18	AC8	EXP1 DIFF P7	
IO_L17N_18	AD8	EXP1 DIFF N7	
IO_L18P_18	AD9	EXP1 DIFF P8	
IO_L18N_18	AC9	EXP1 DIFF N8	
IO_L19P_18	AB9	EXP1 DIFF P14	
IO_L19N_18	AA9	EXP1 DIFF N14	

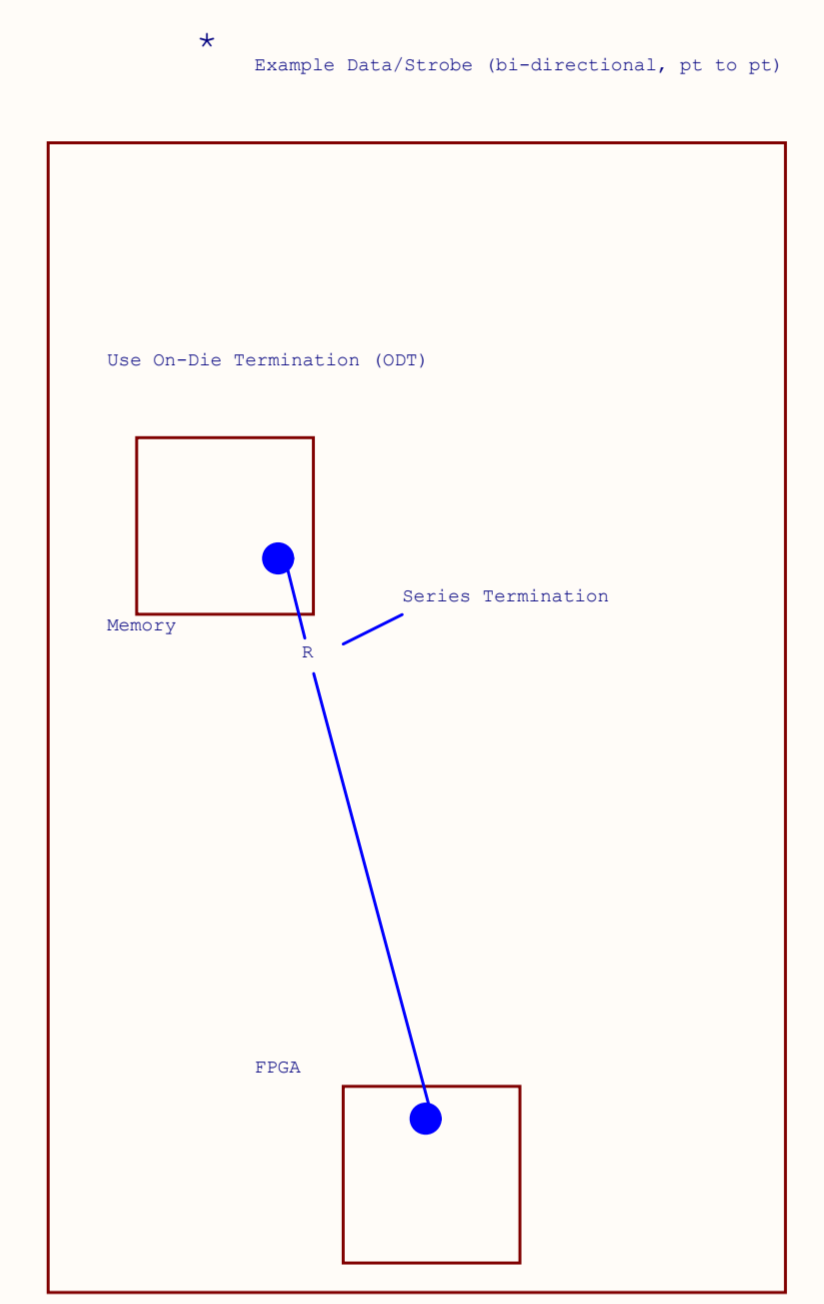
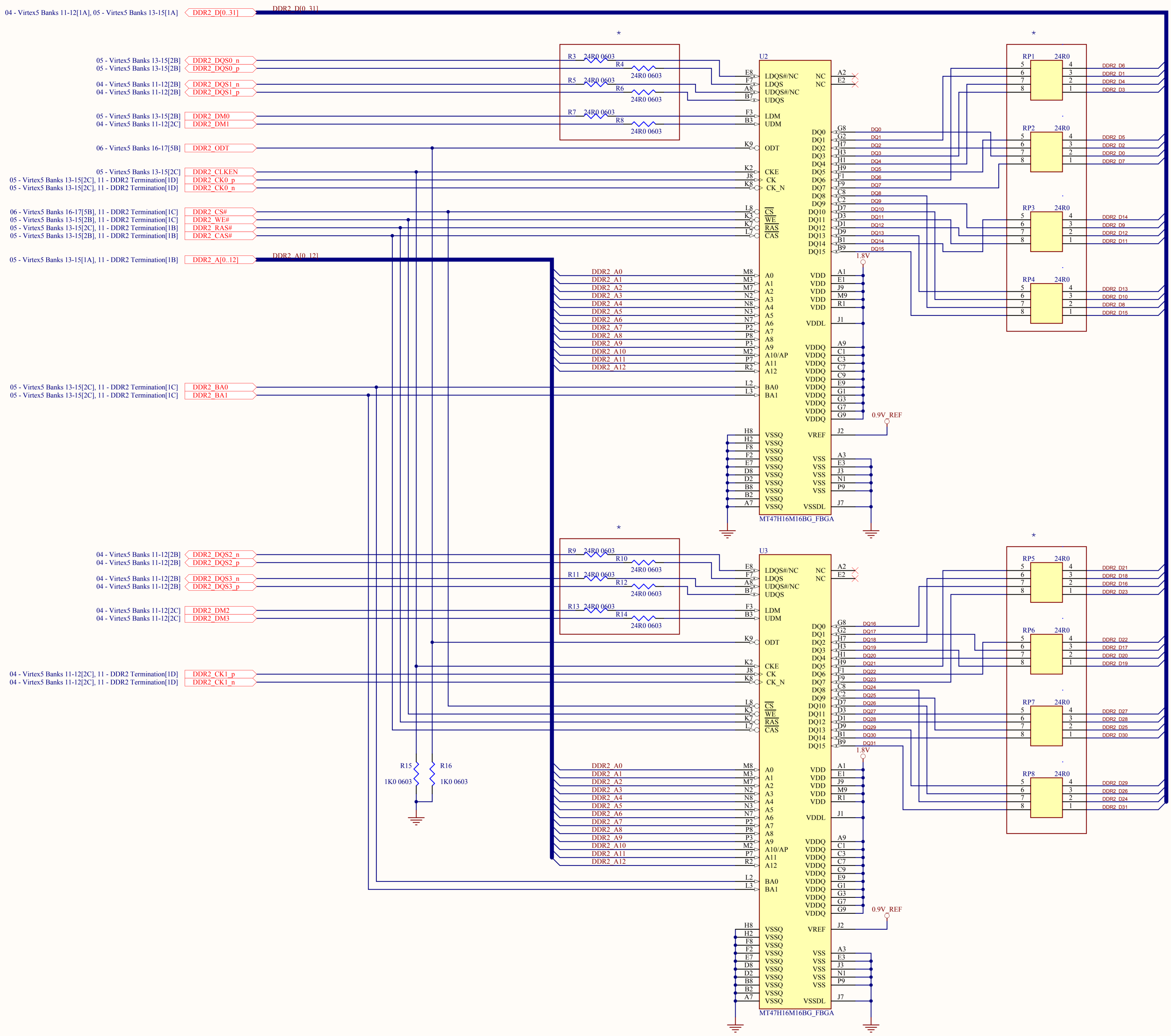
XC5VFX30T-1FFG665C

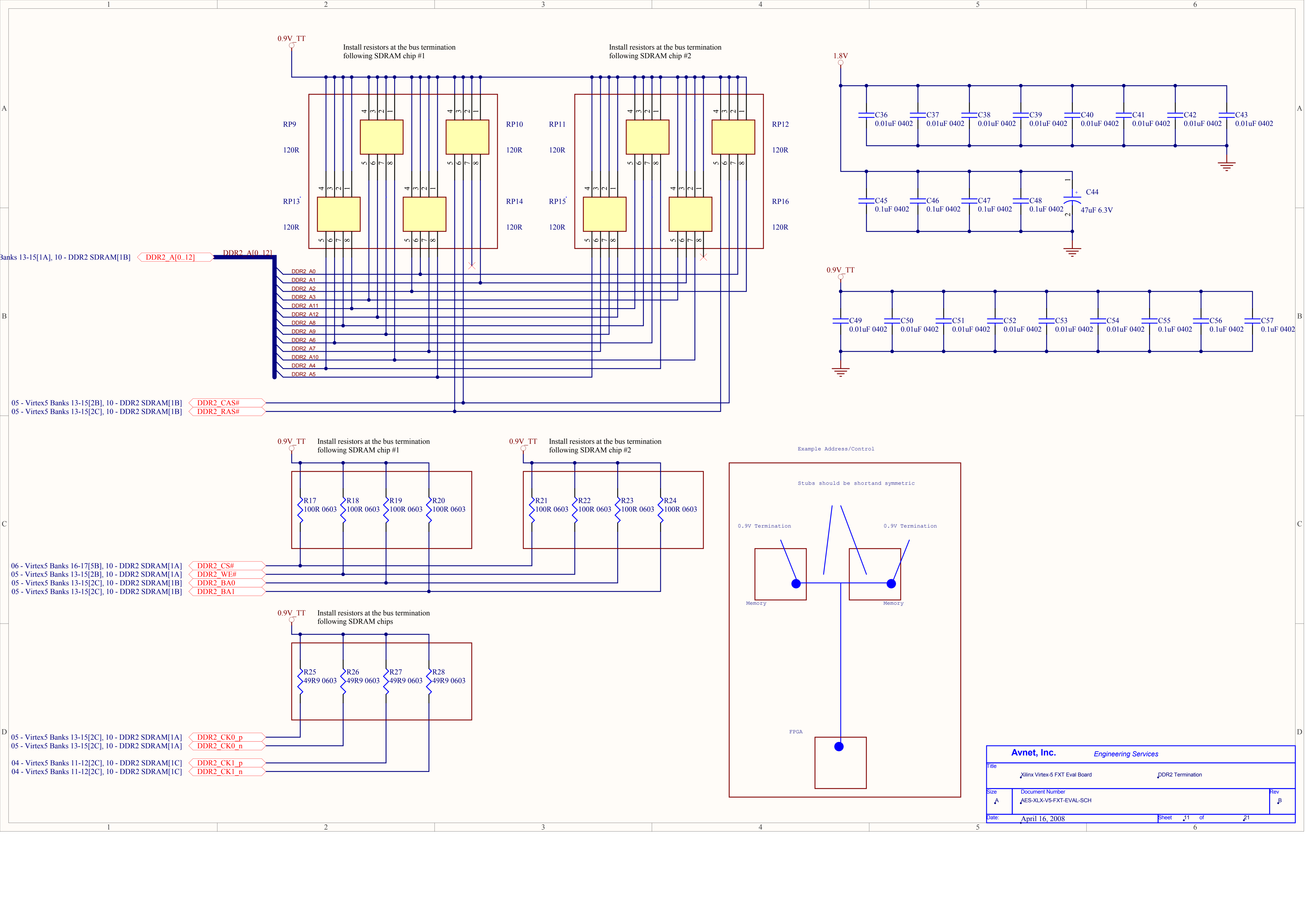


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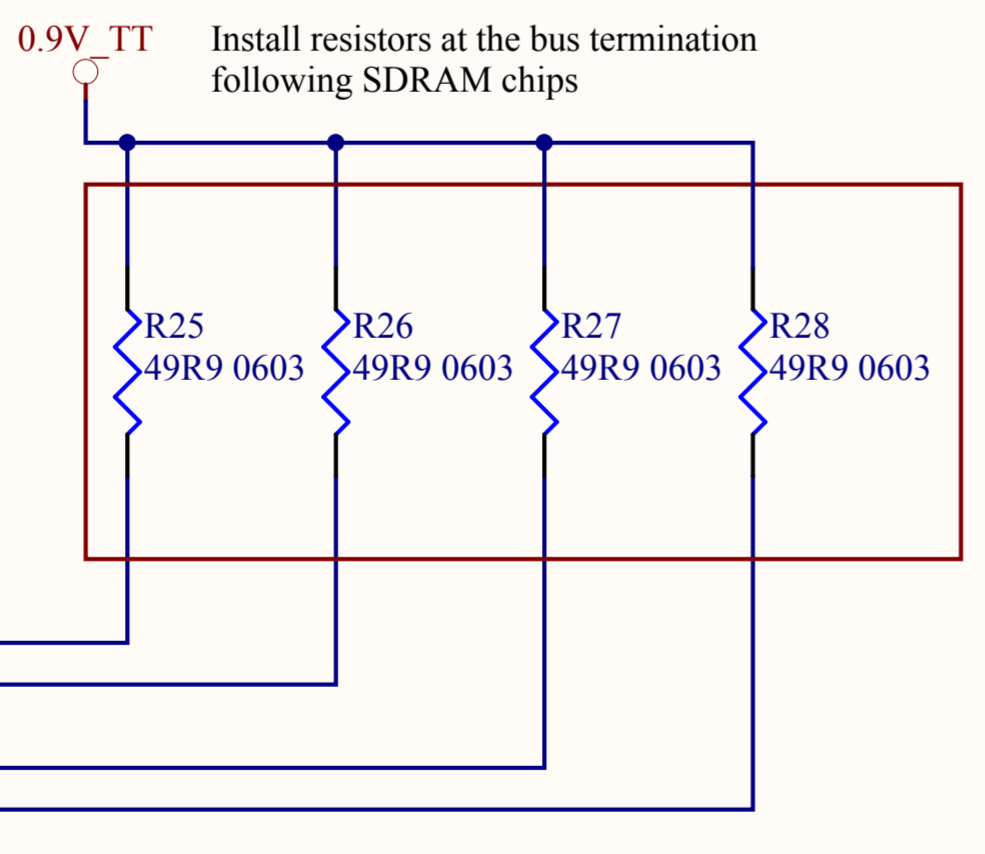
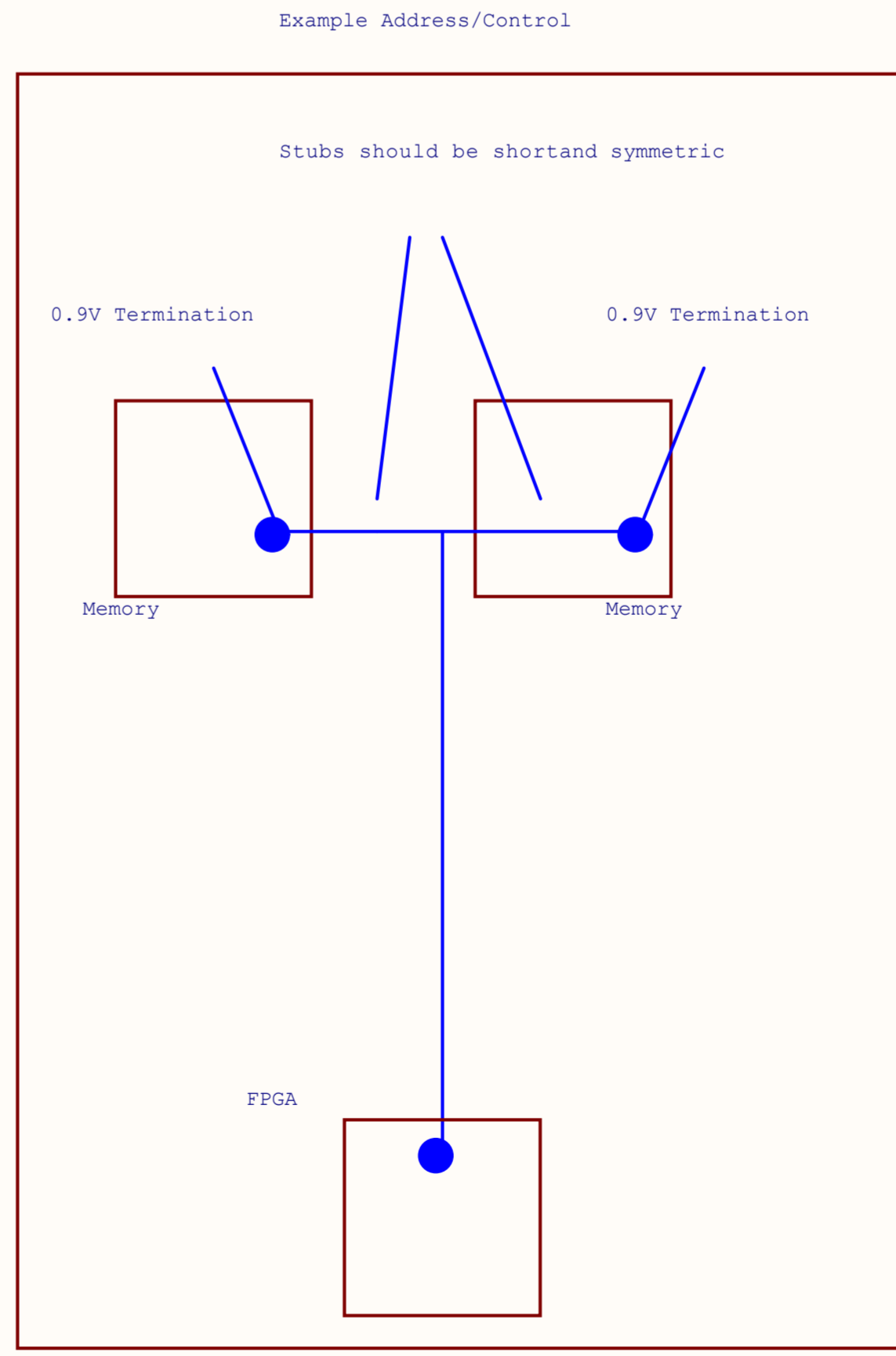
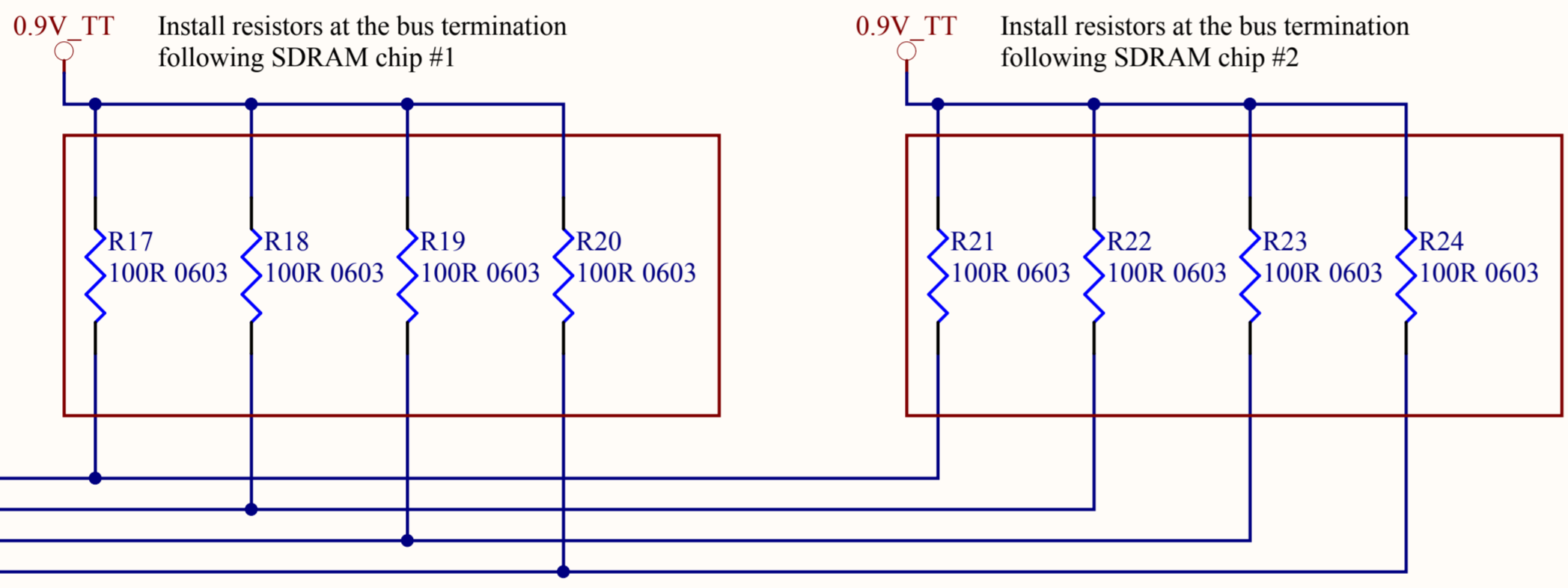
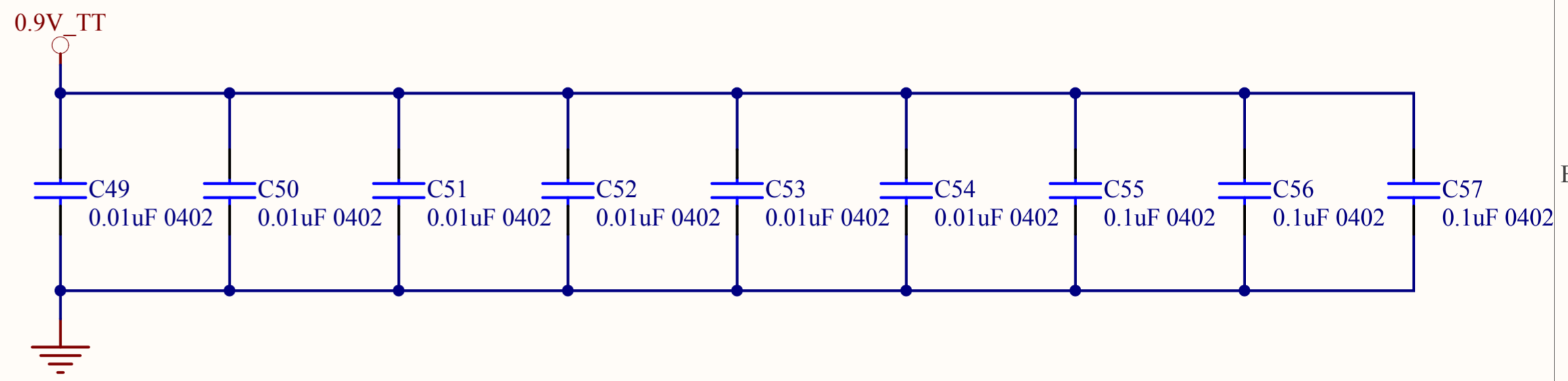
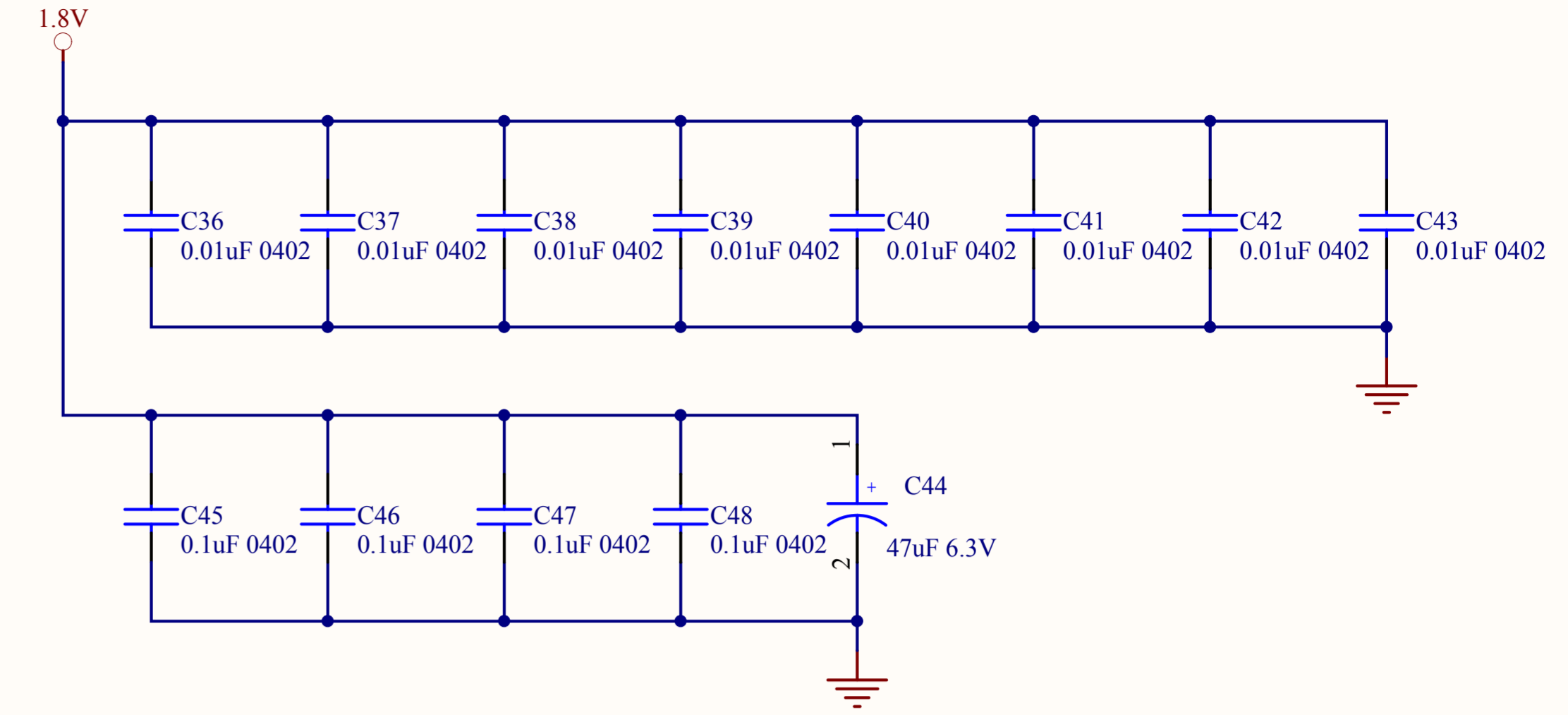
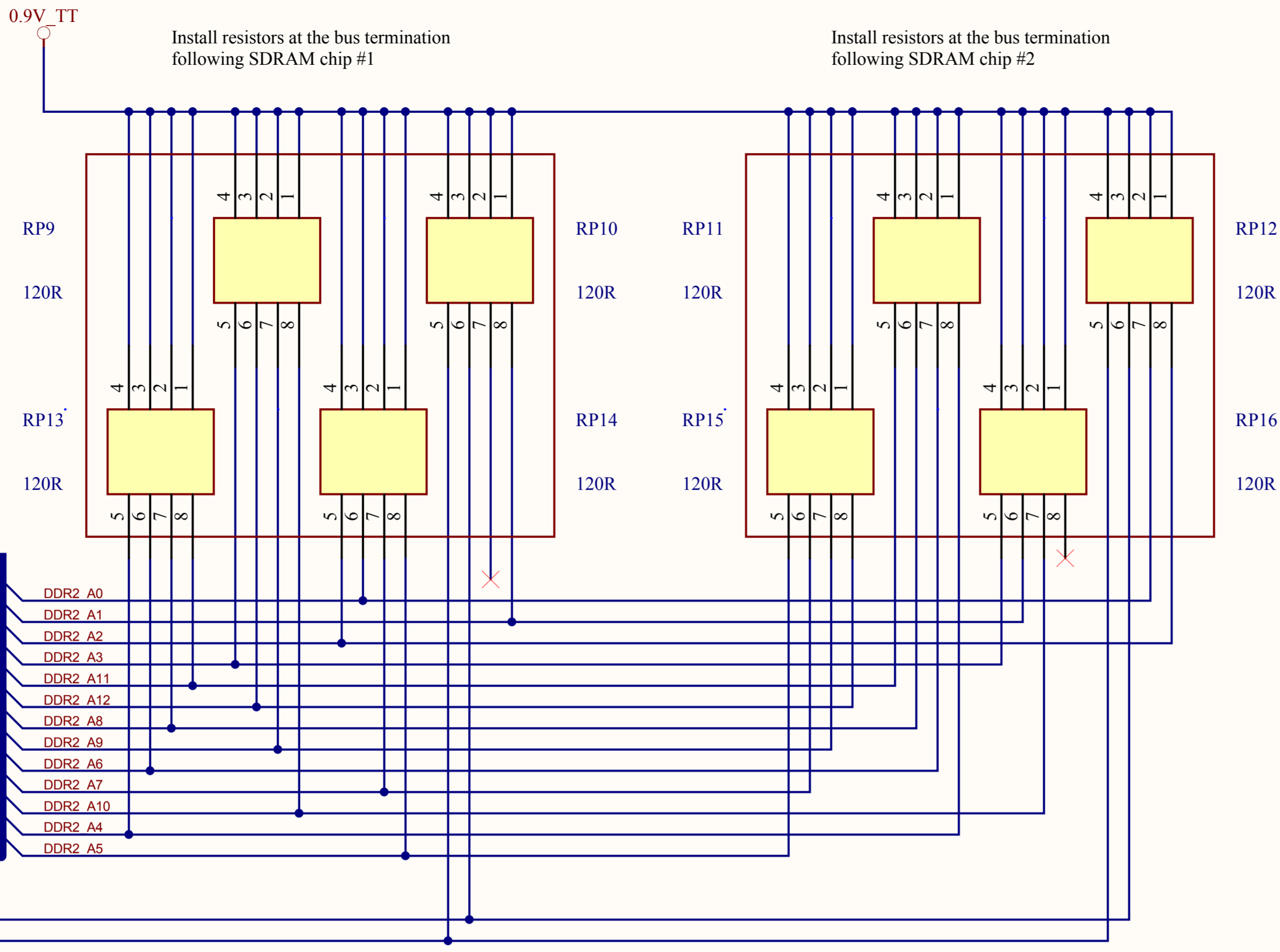
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Size	Document Number
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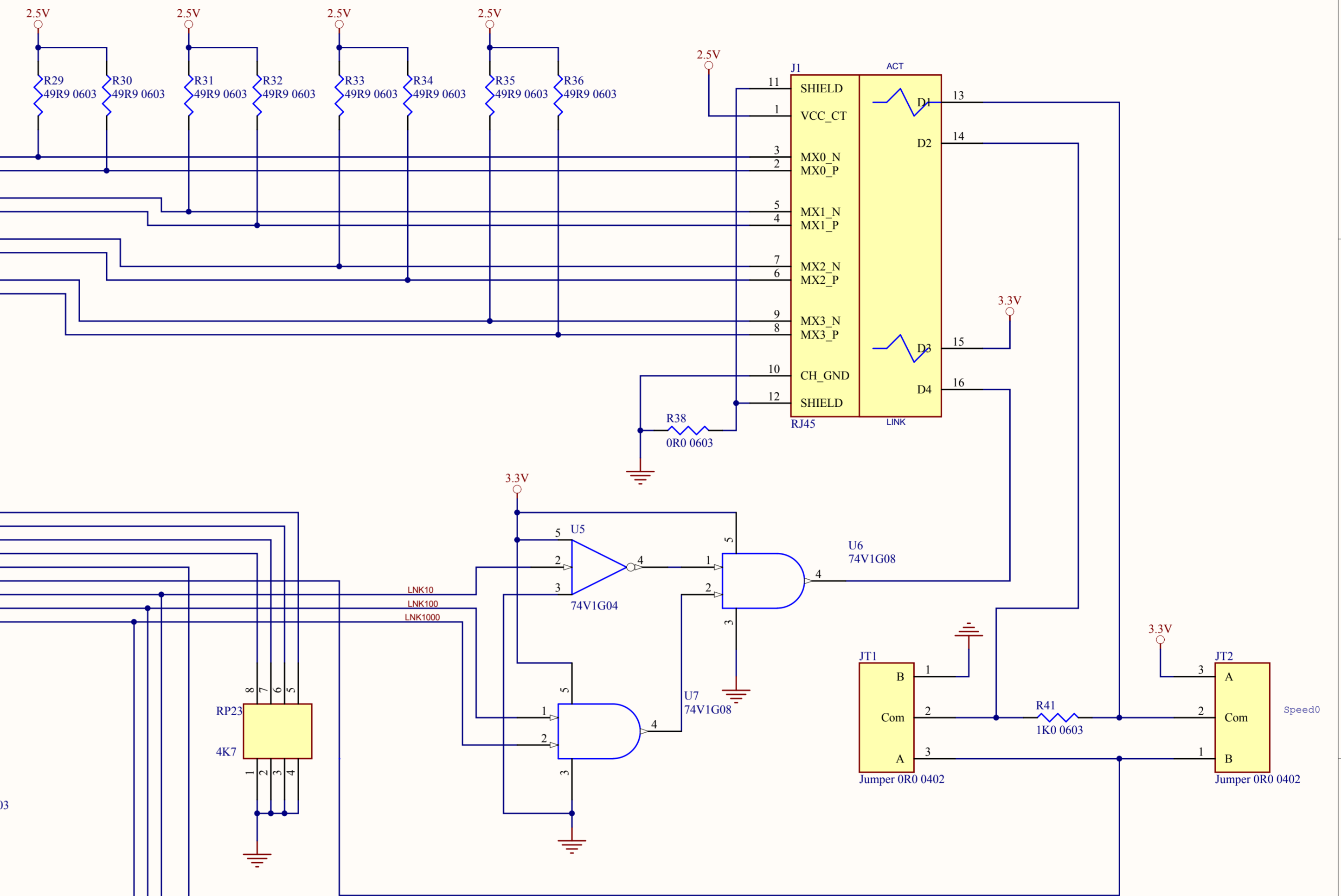
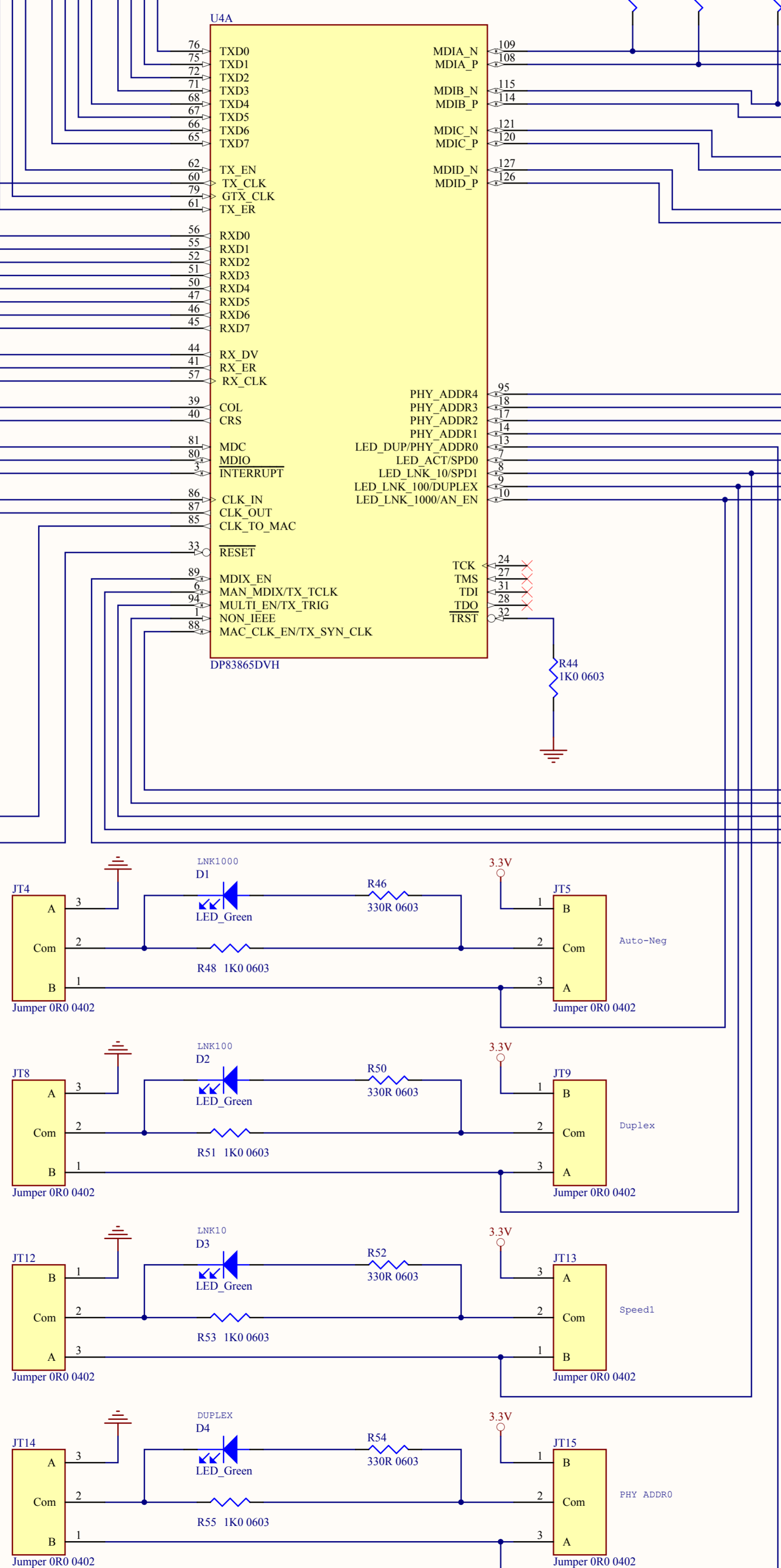
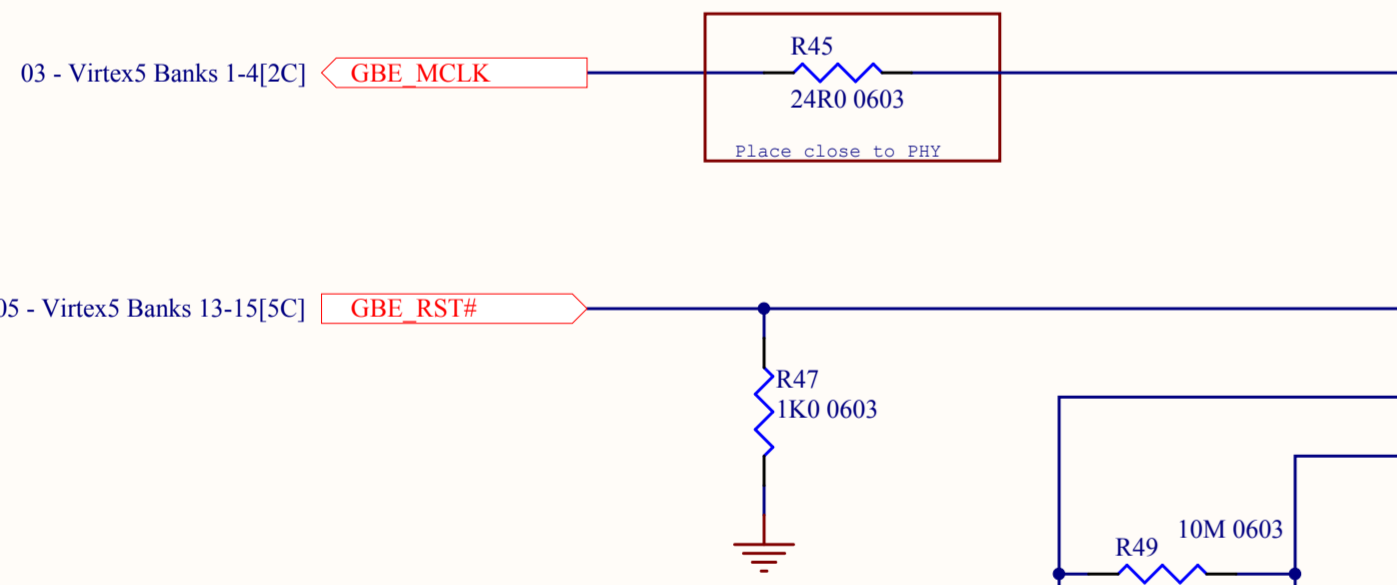
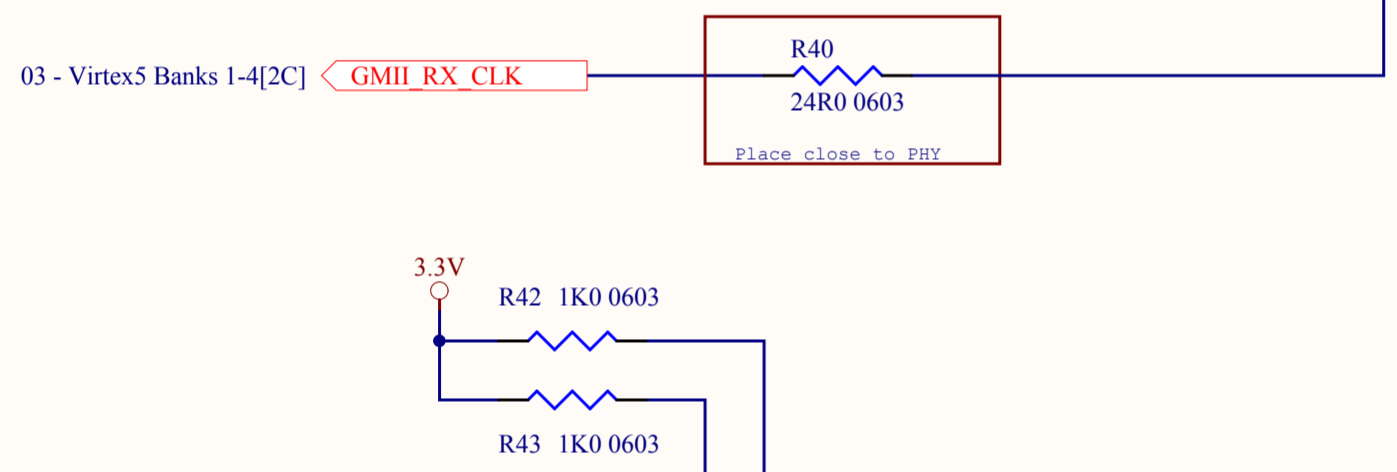
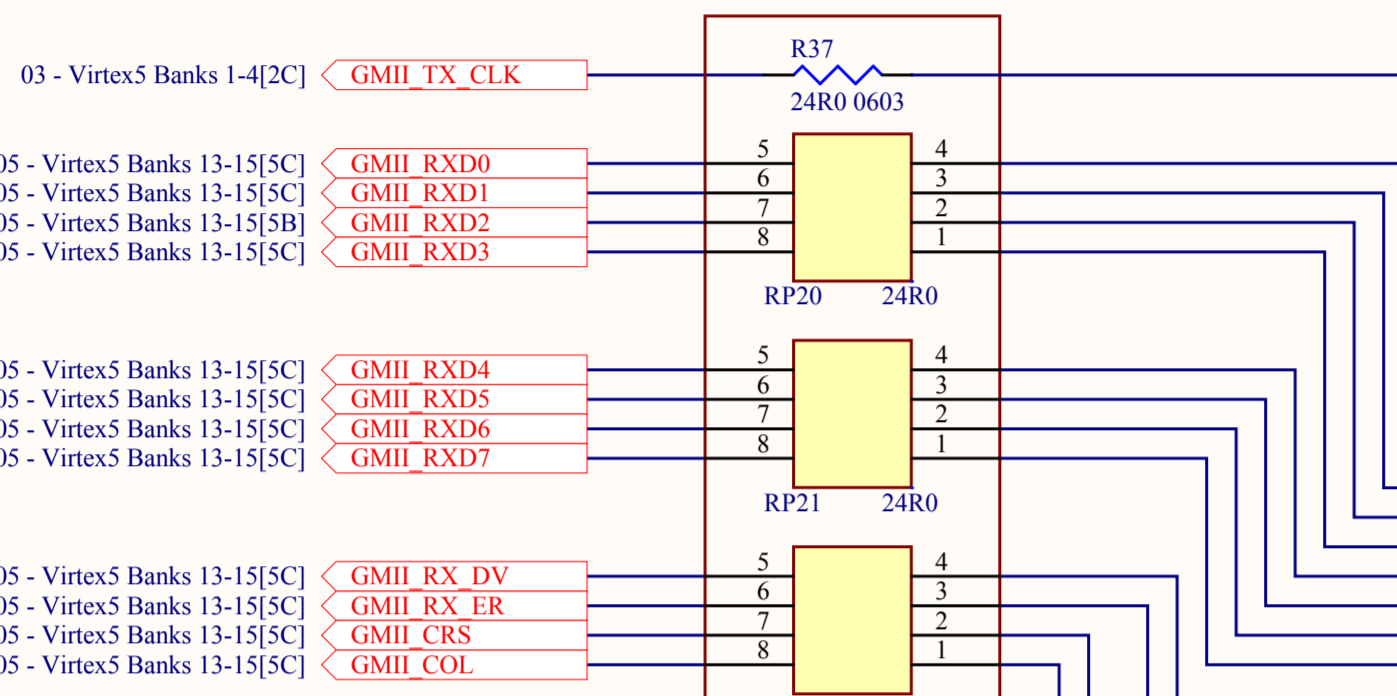
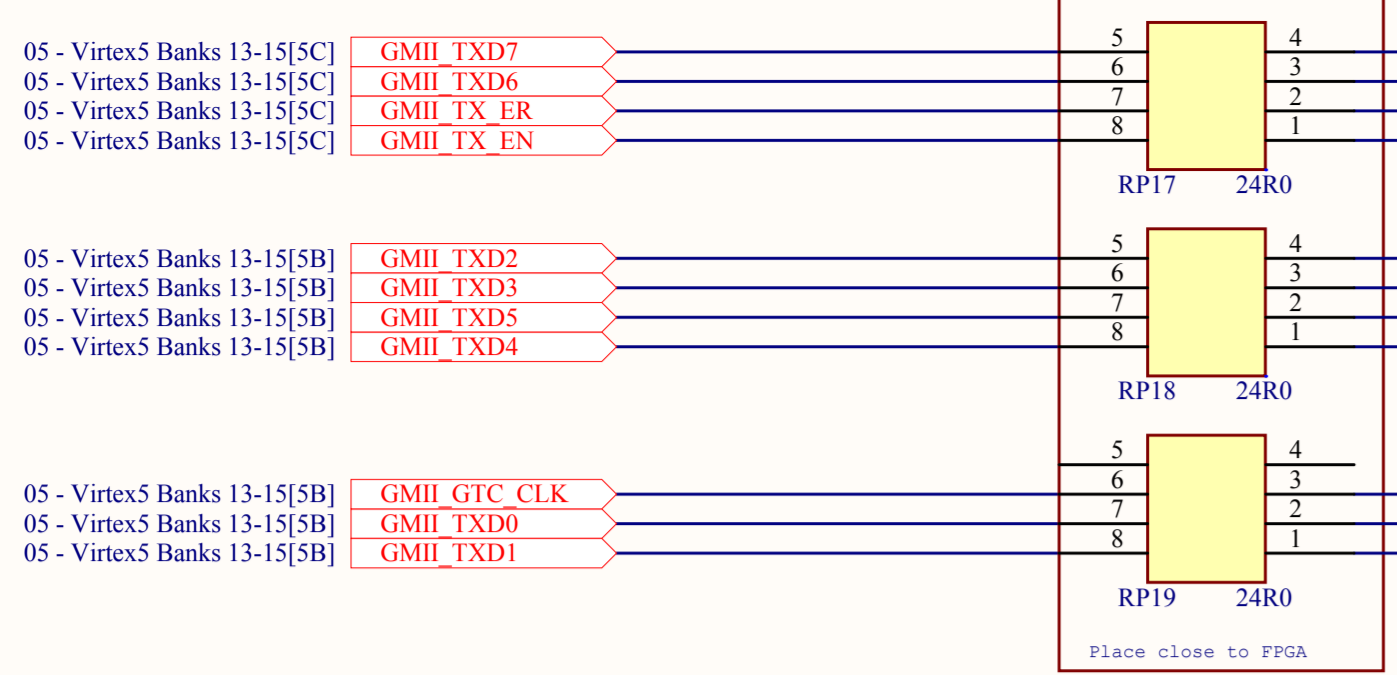
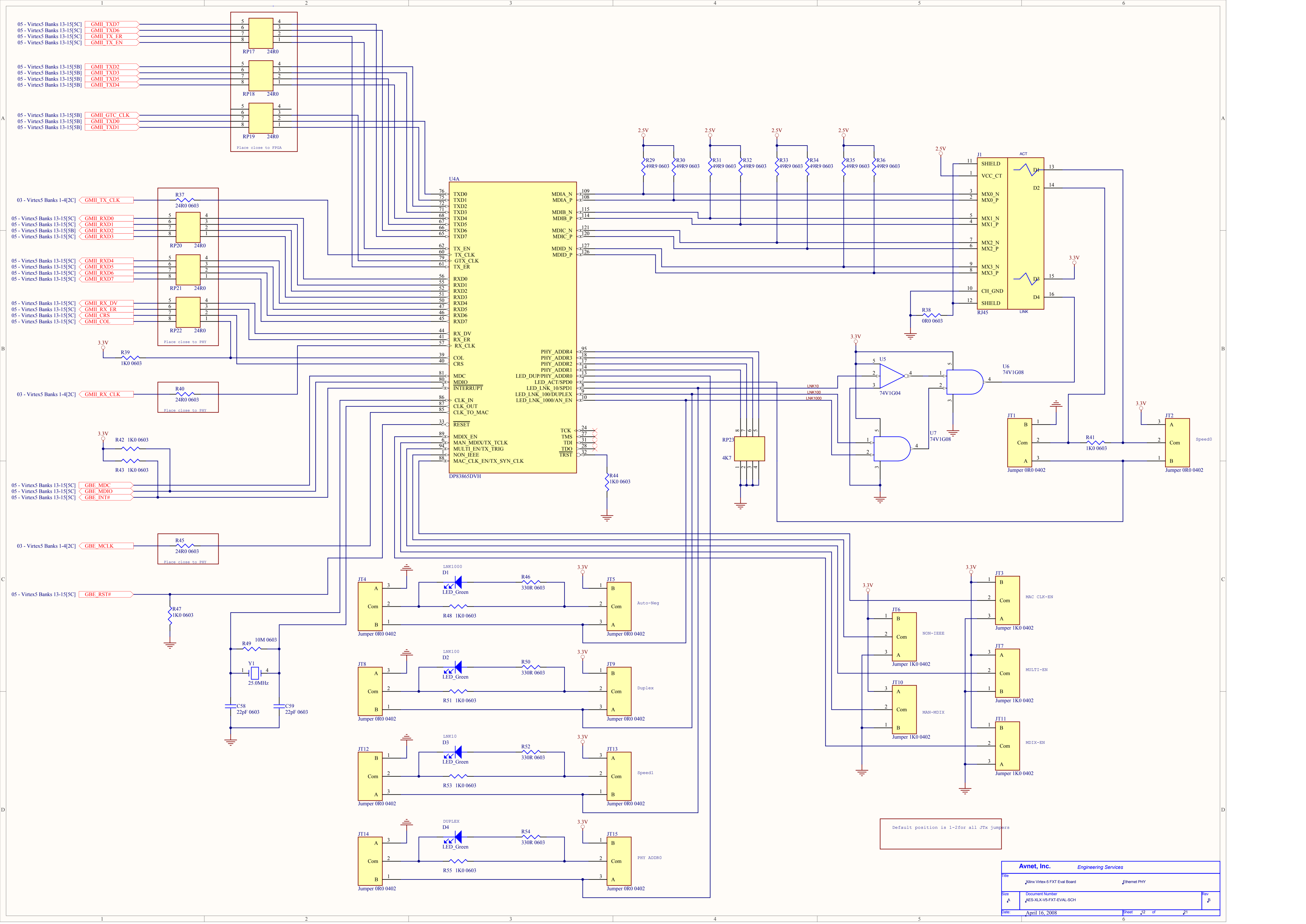


Install resistors at the bus termination following SDRAM chip #1

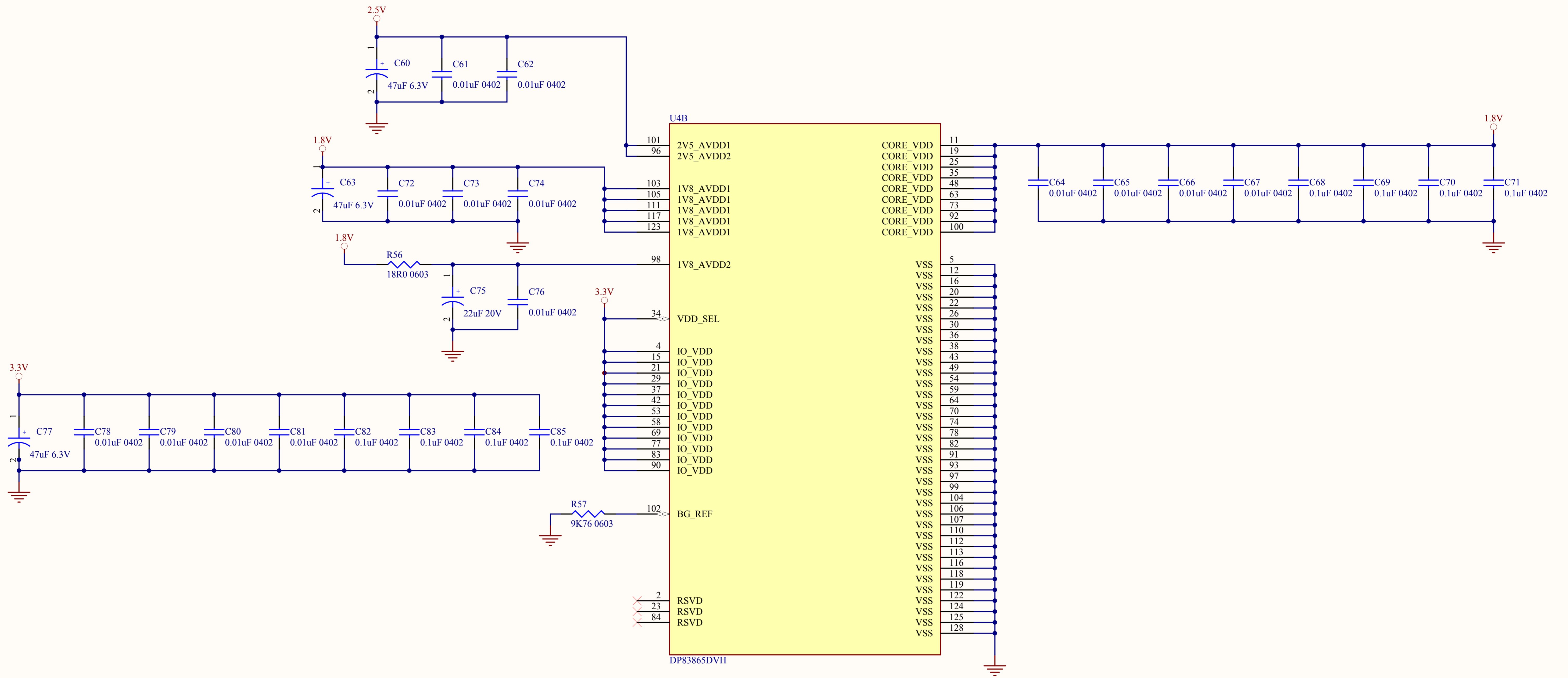
Install resistors at the bus termination following SDRAM chip #2



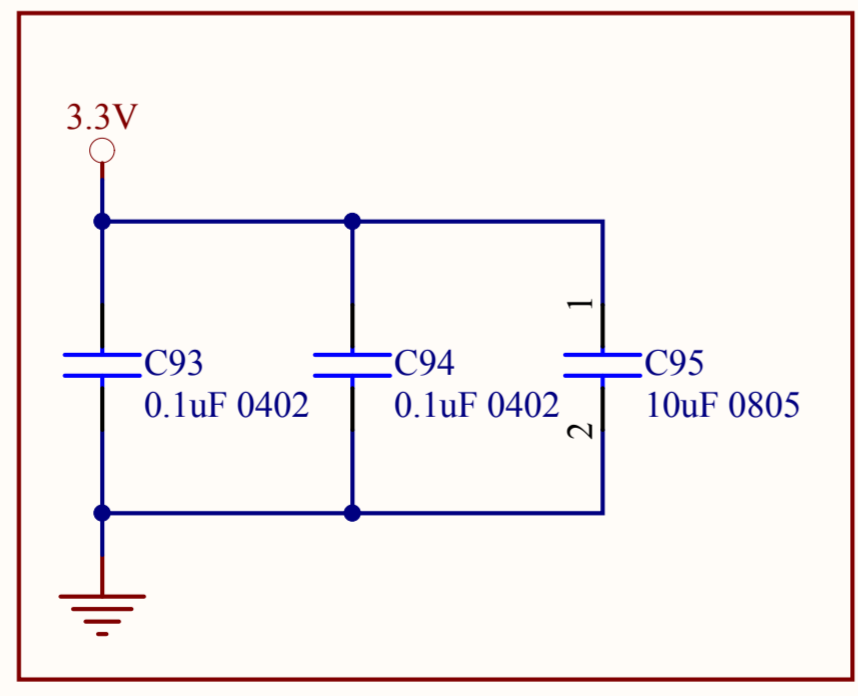
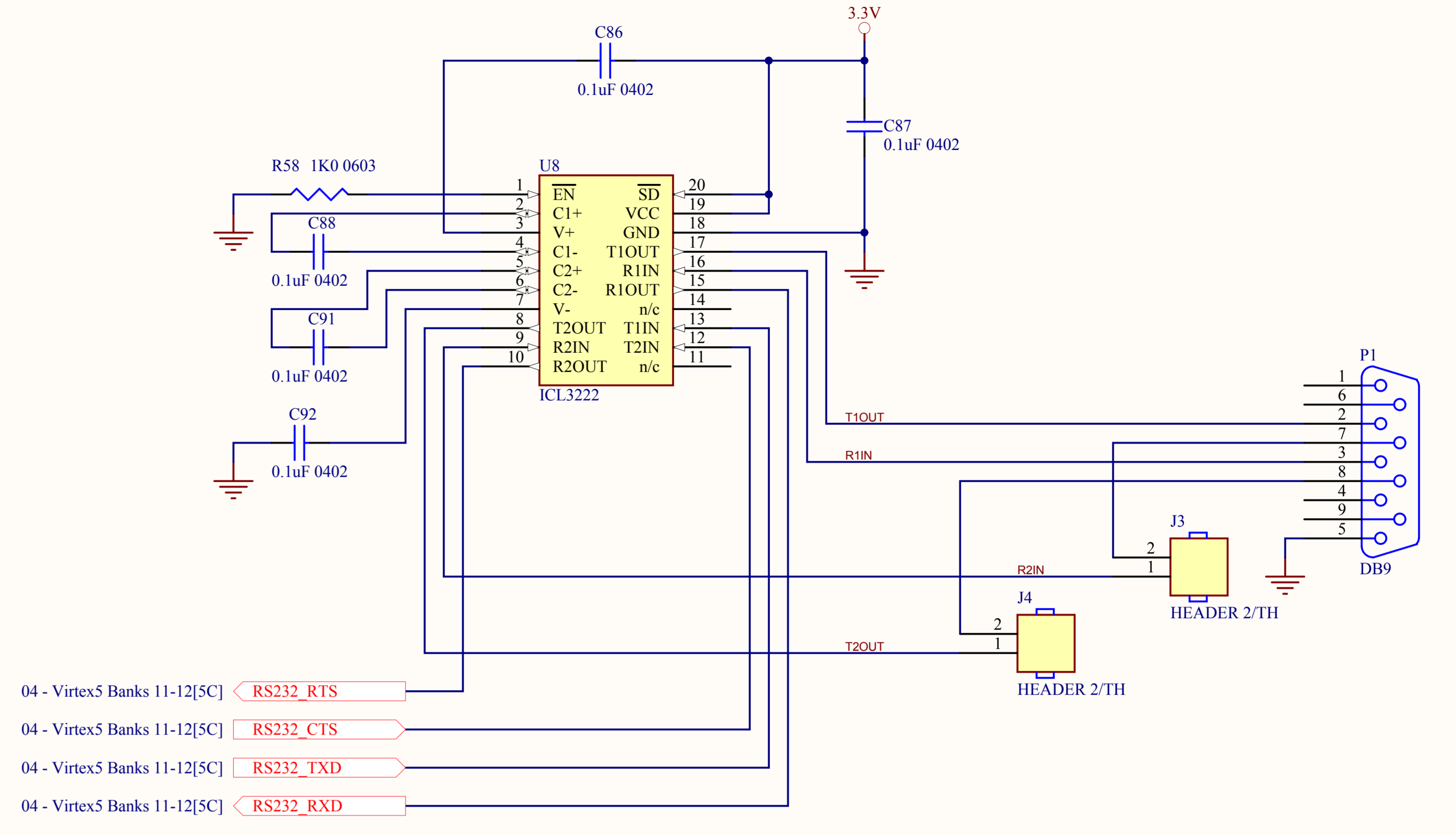
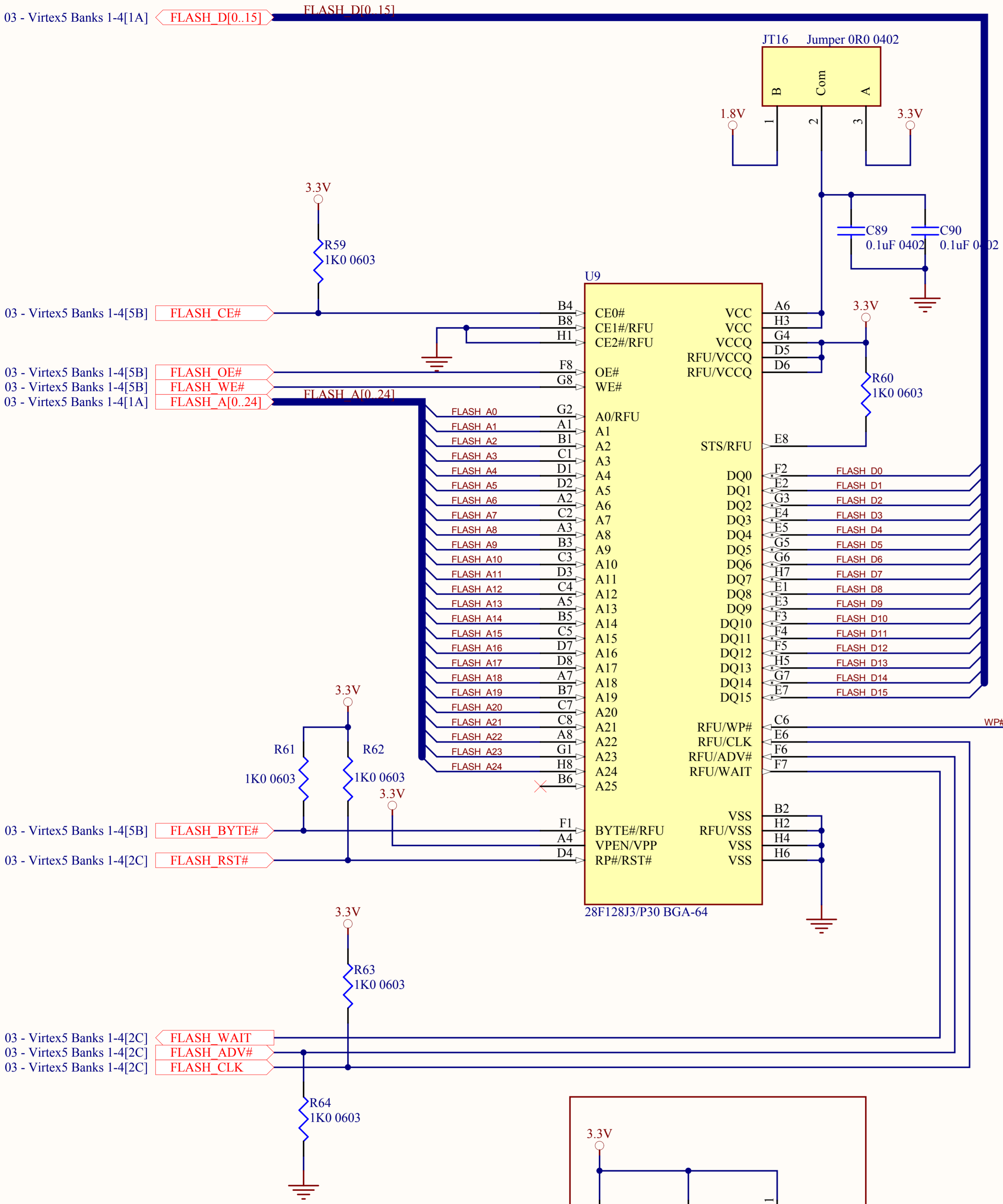
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Size	Document Number
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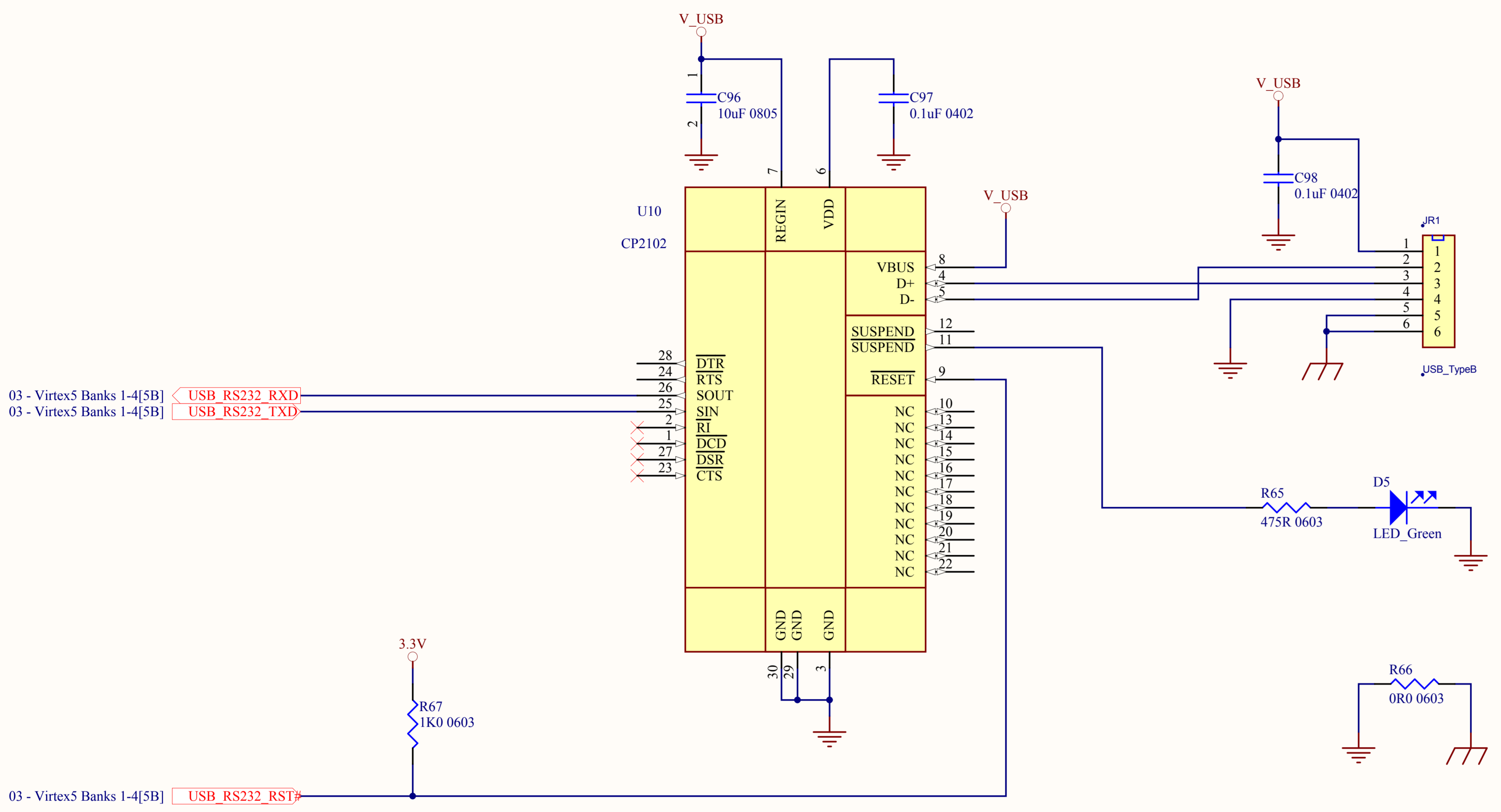
Default position is 1-2 for all JTx jumpers



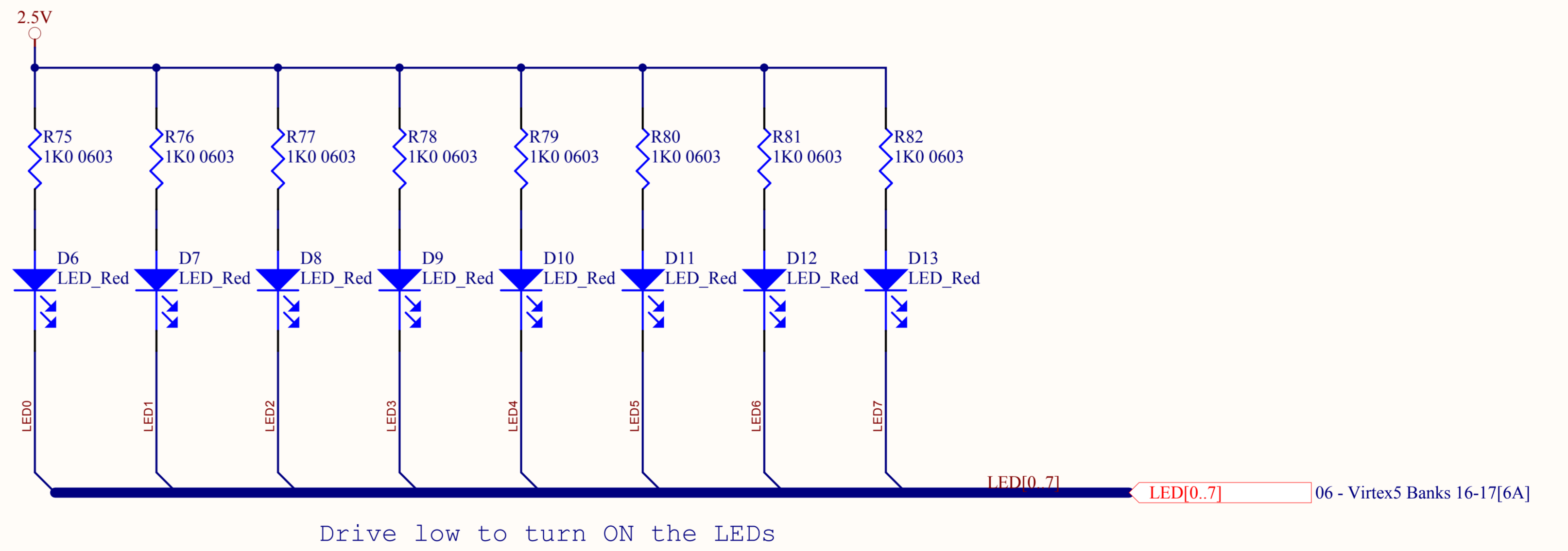
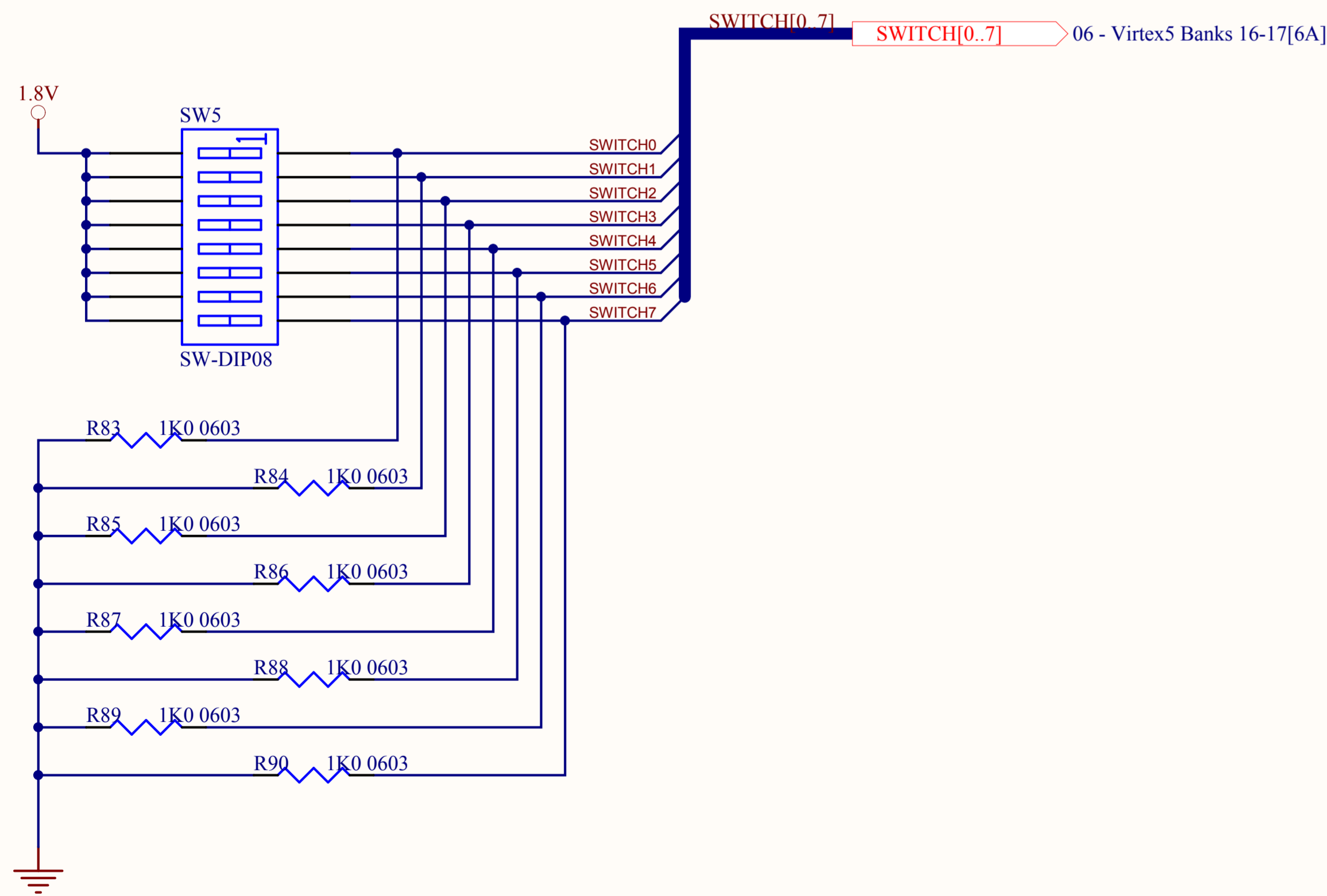
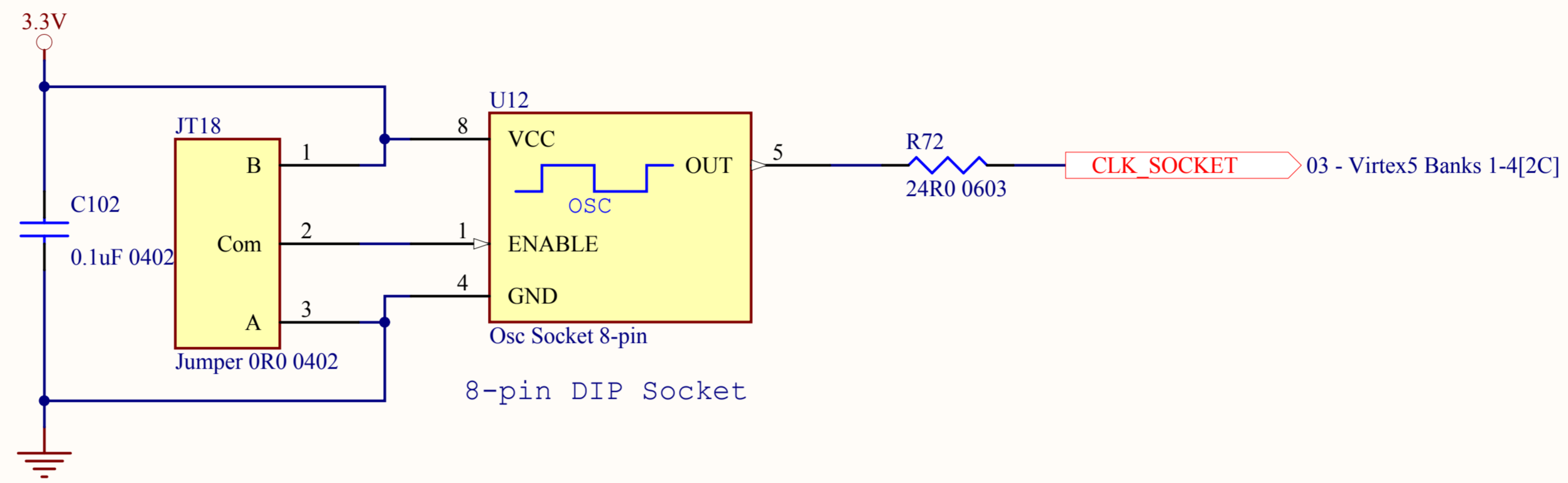
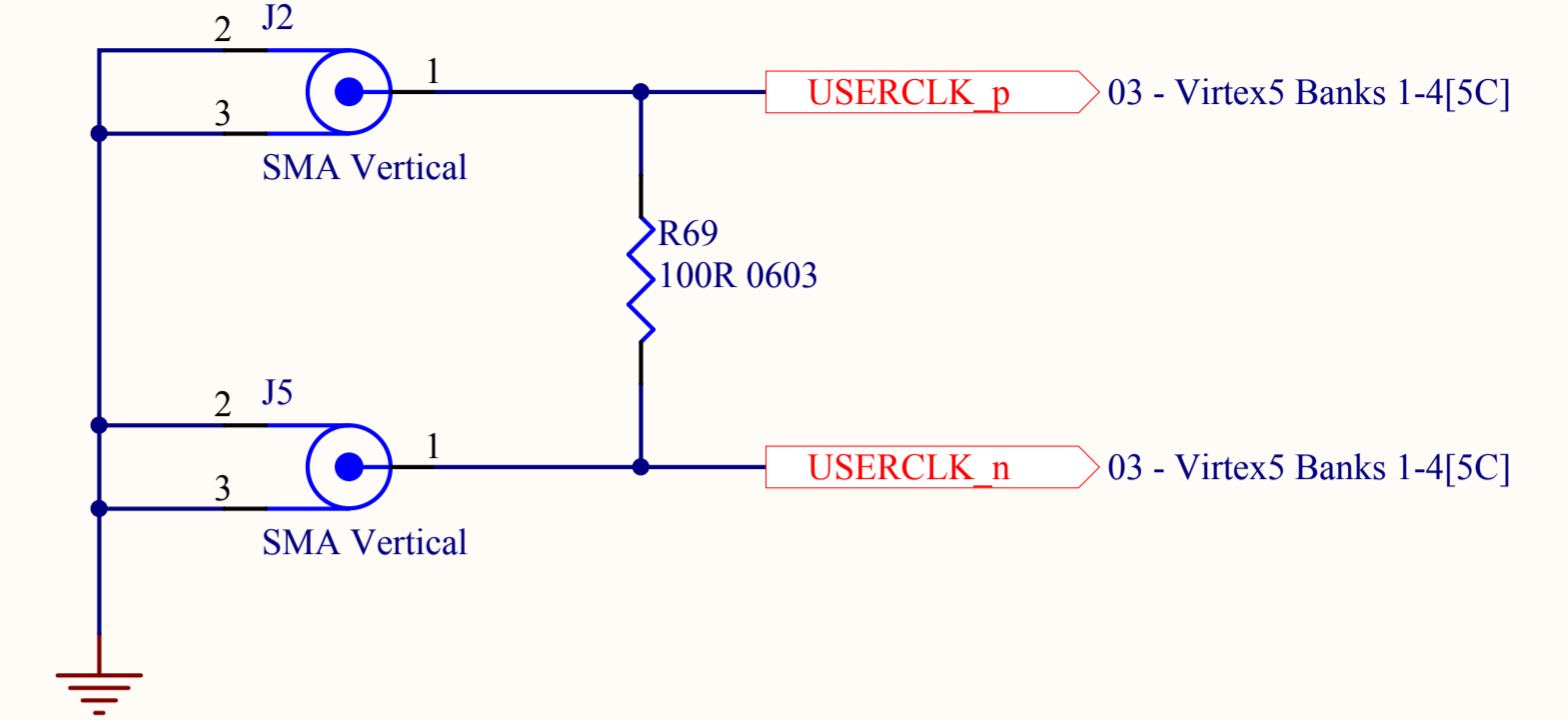
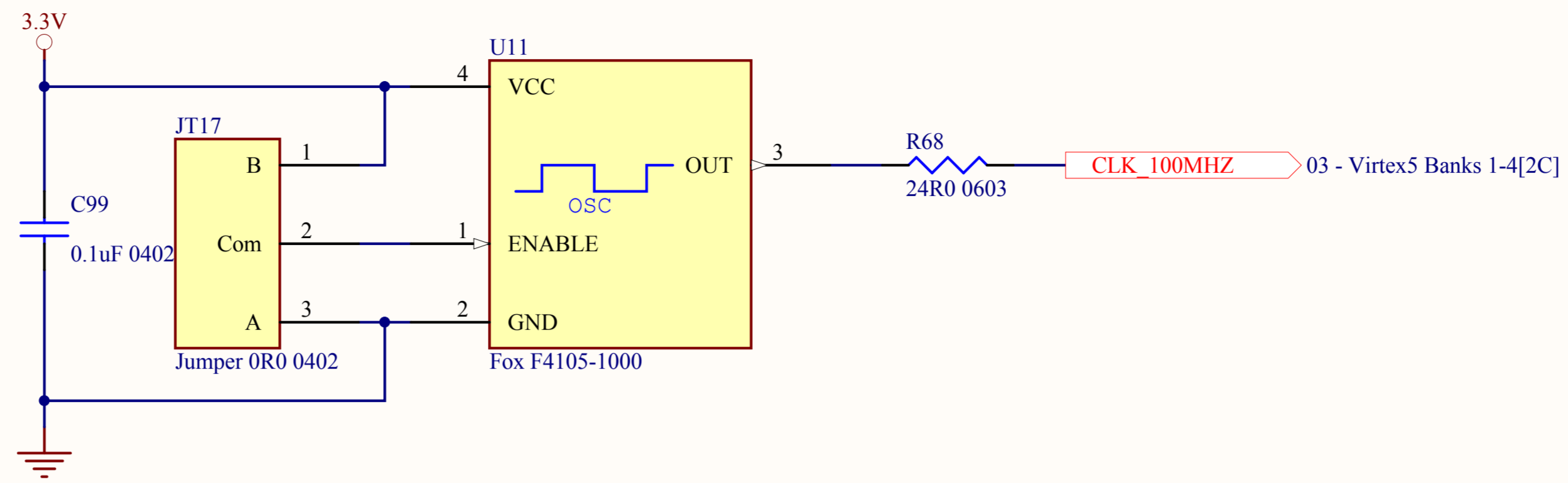
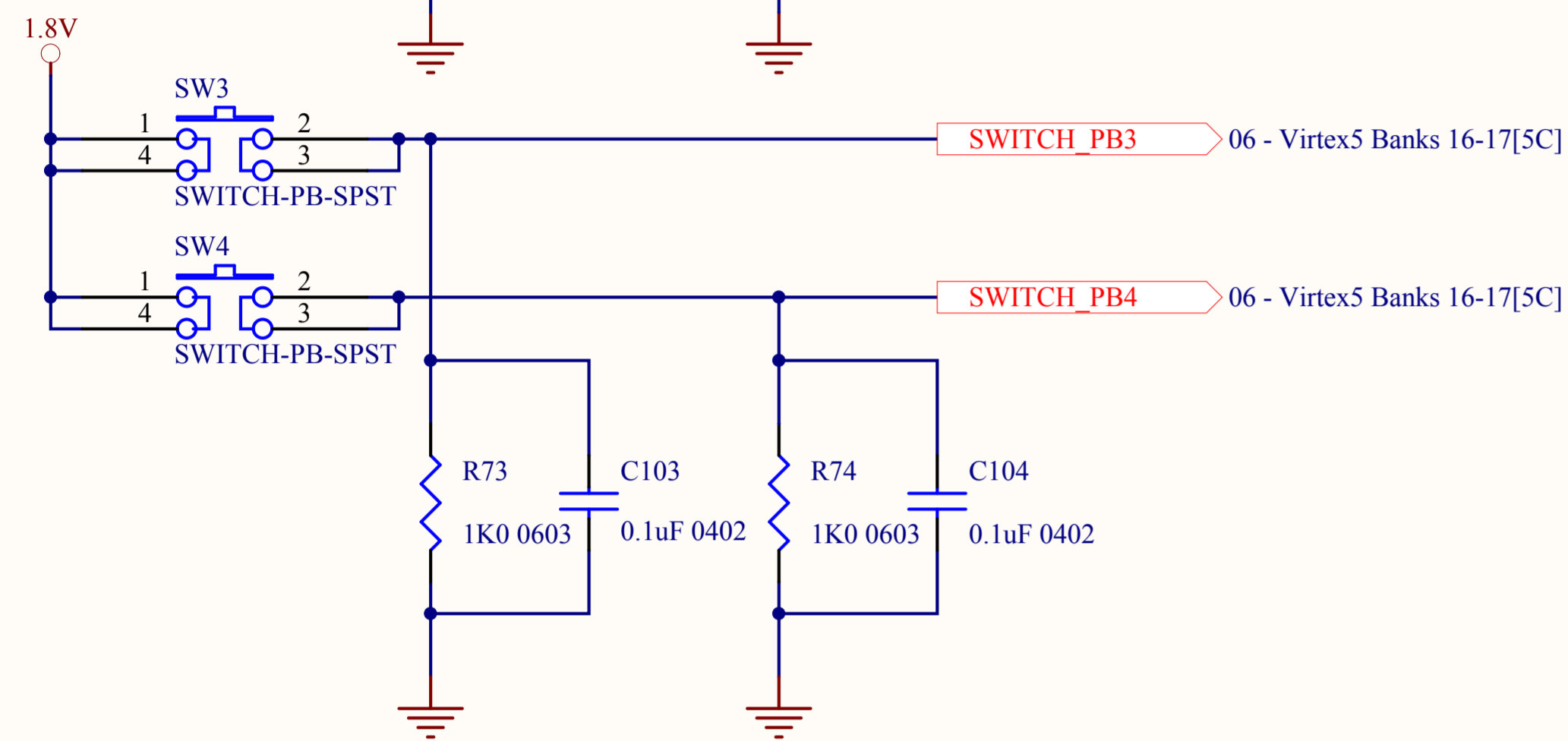
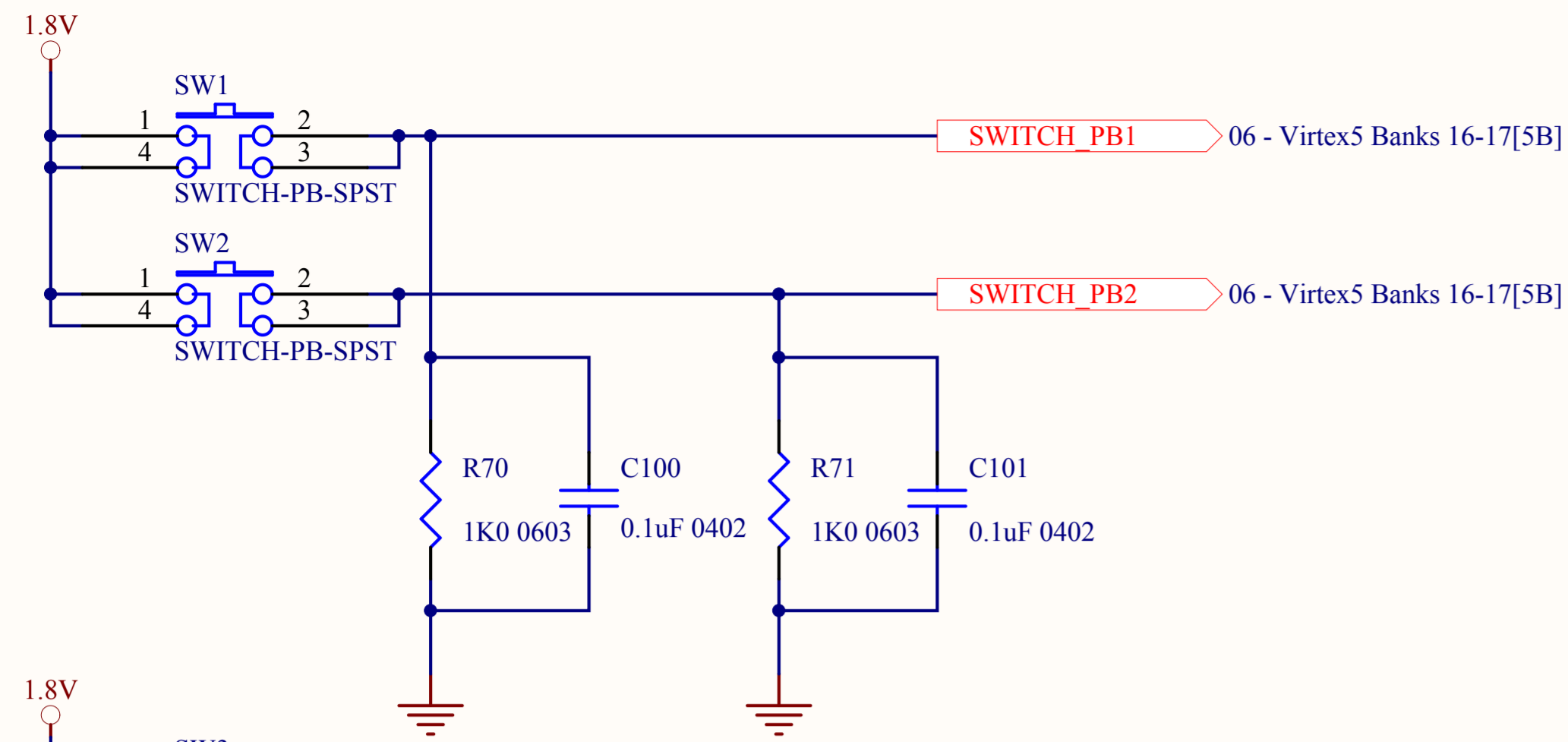
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Size A	Document Number AES-XLX-V5-FXT-EVAL-SCH
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USB-to-RS232		
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06 - Virtex5 Banks 16-17[1A] EXP1_SE_IO [0..33]

EXP1_SE_IO [0..33]

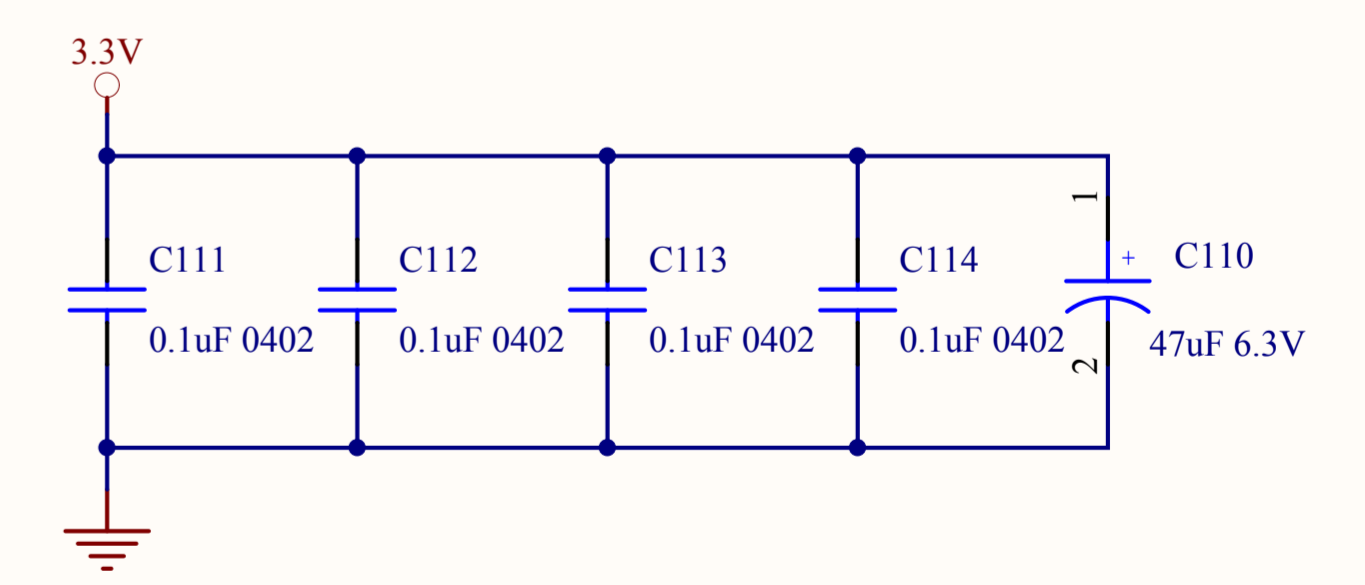
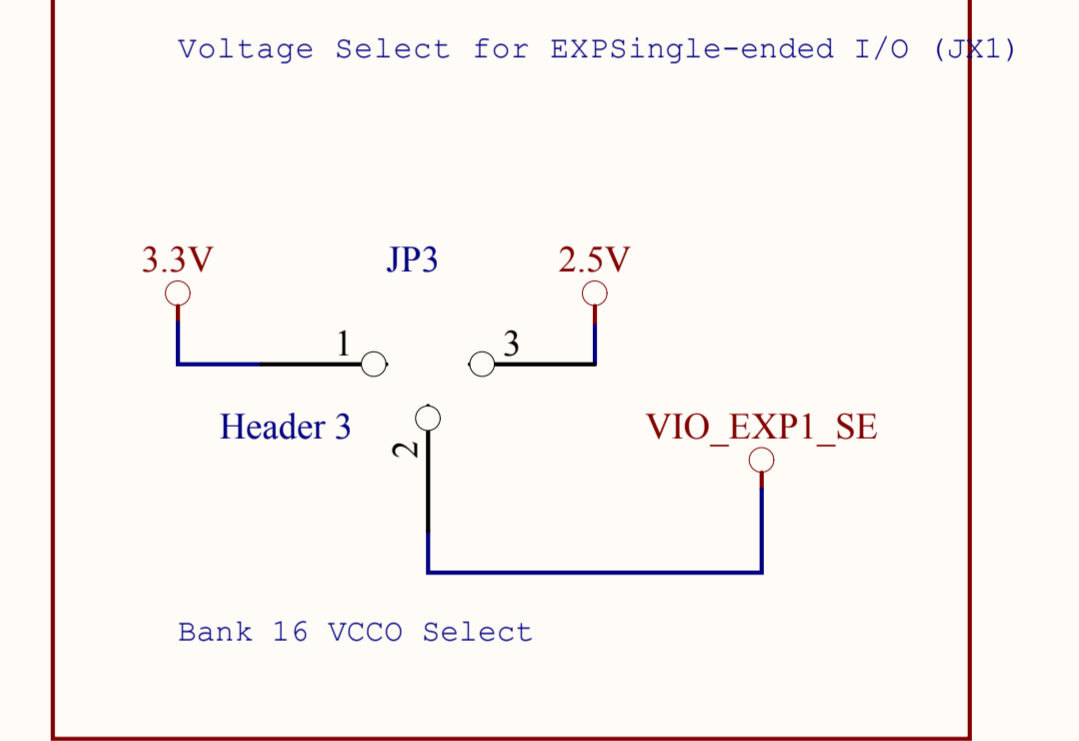
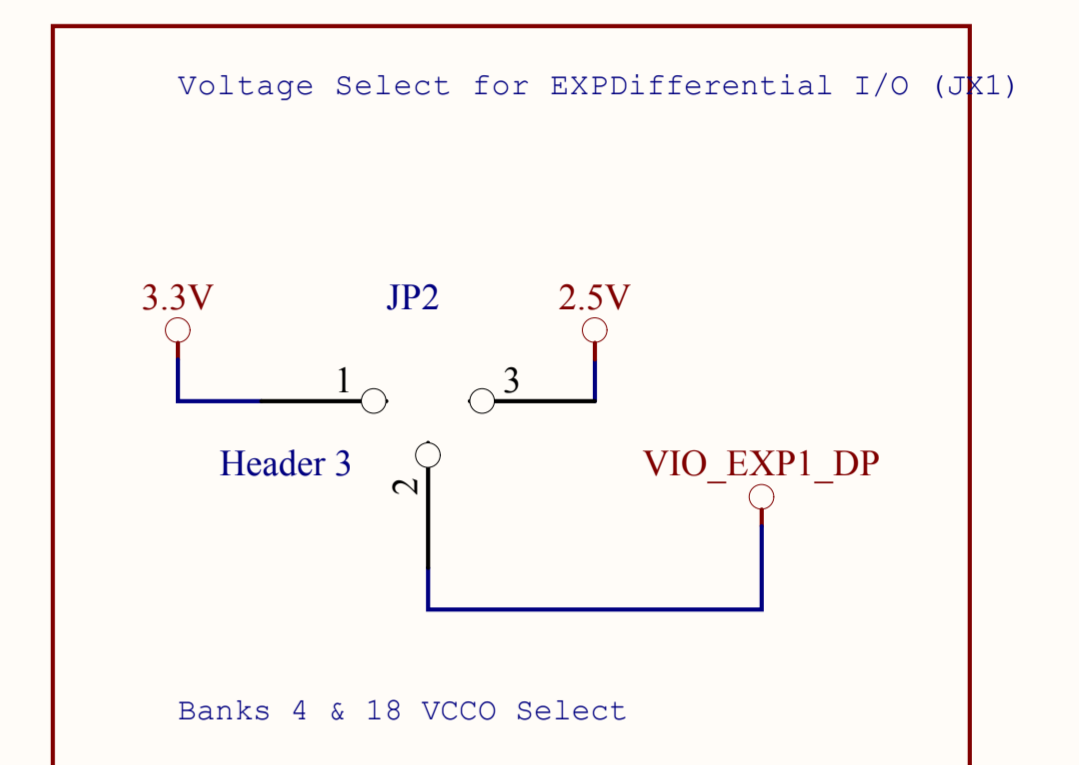
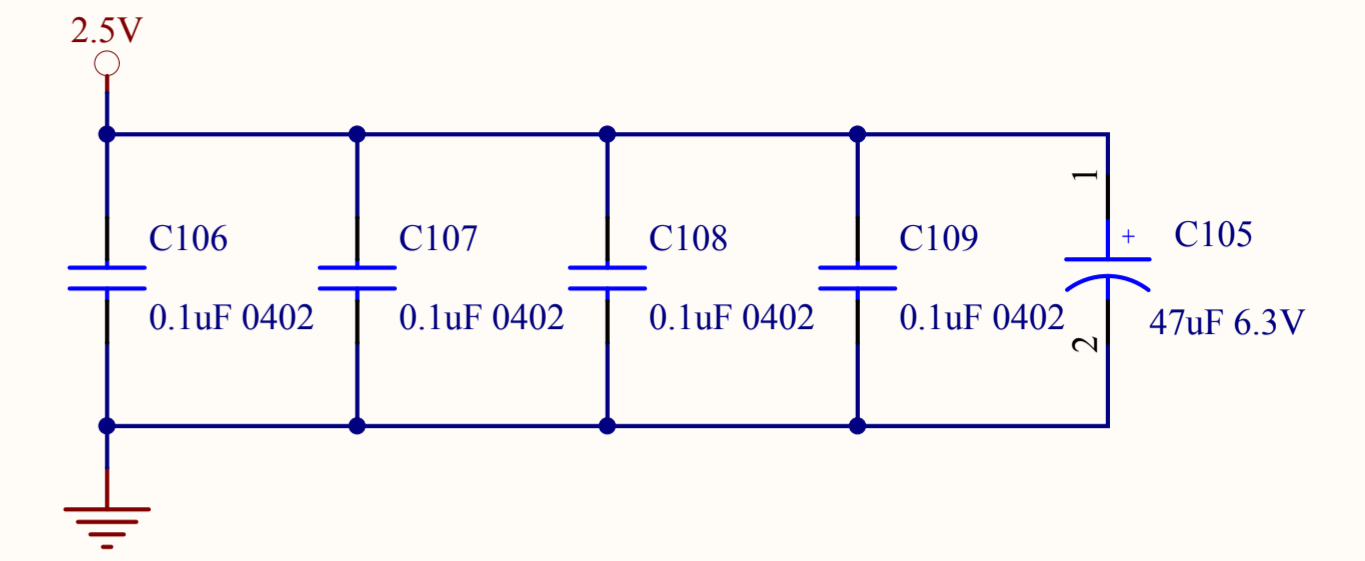
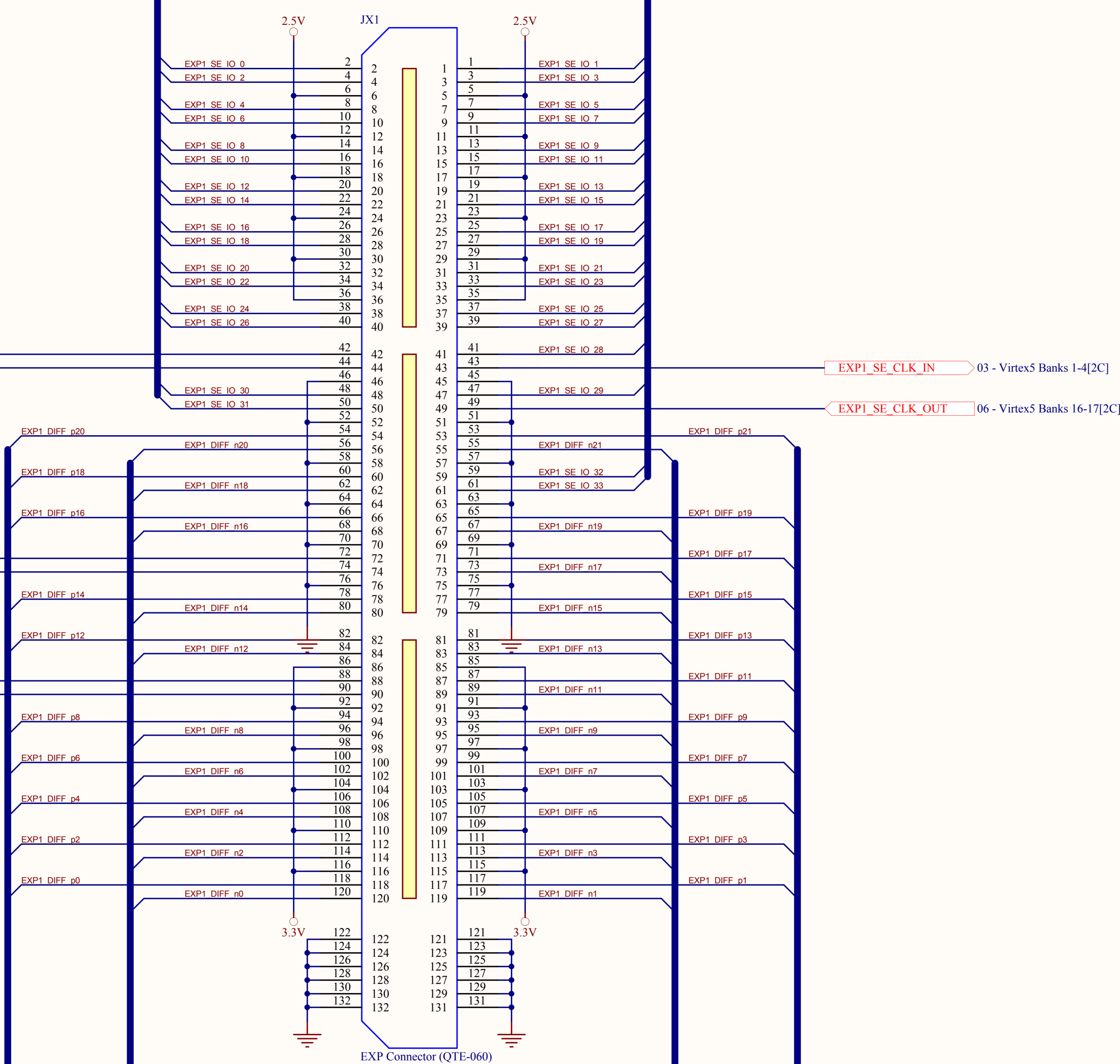
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03 - Virtex5 Banks 1-4[5C] EXP1_DIFF_CLK_IN_n

03 - Virtex5 Banks 1-4[5C] EXP1_DIFF_CLK_OUT_p
03 - Virtex5 Banks 1-4[5C] EXP1_DIFF_CLK_OUT_n

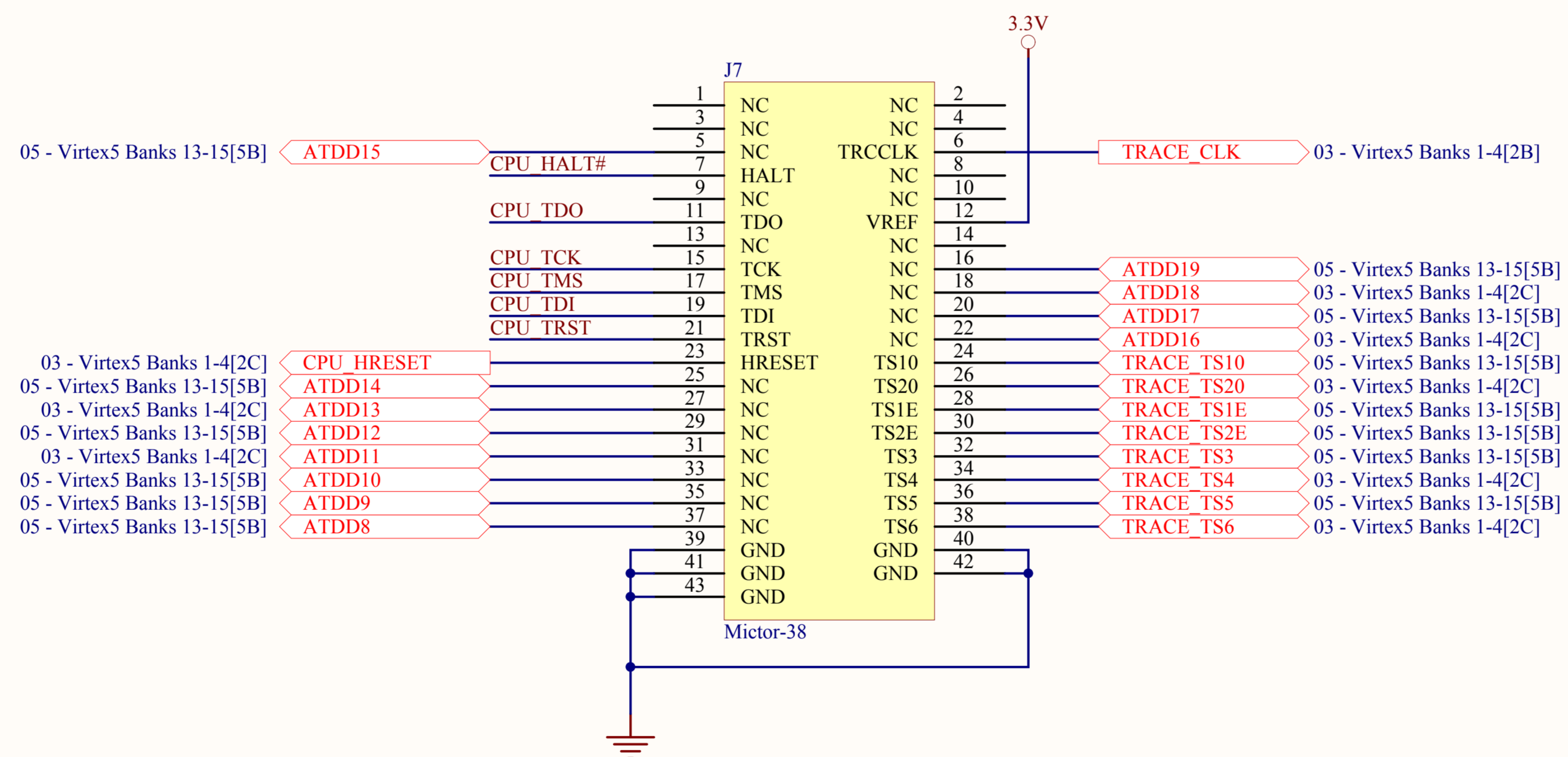
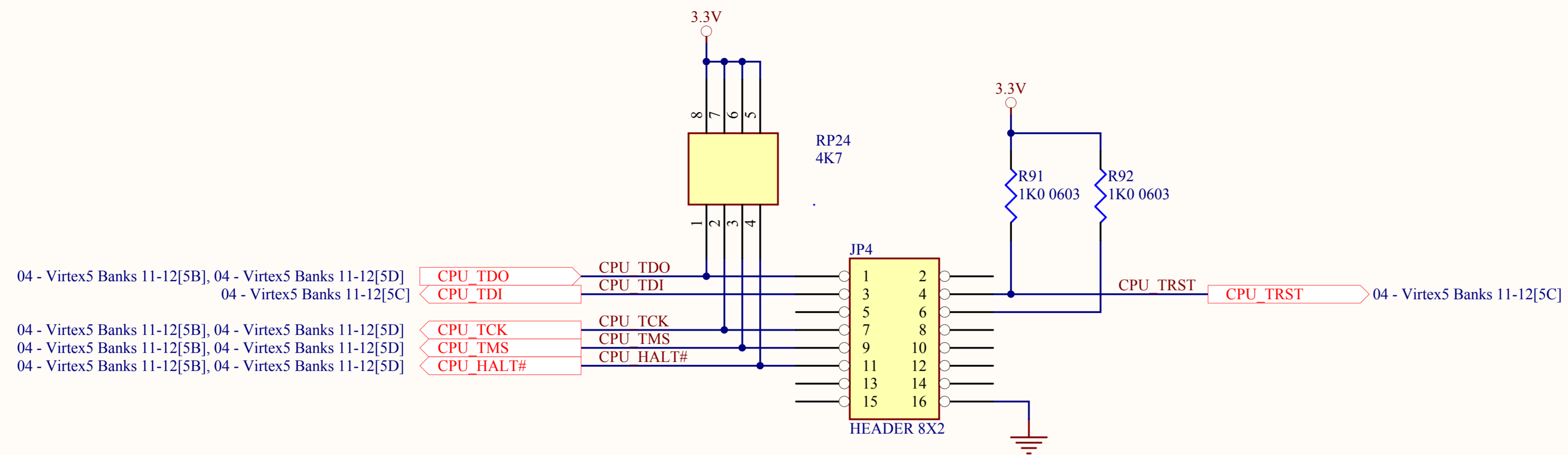
07 - Virtex5 Bank 18[4C] EXP1_RCLK_DIFF_p
07 - Virtex5 Bank 18[4C] EXP1_RCLK_DIFF_n

03 - Virtex5 Banks 1-4[5D], 07 - Virtex5 Bank 18[5A] EXP1_DIFF_p[0..21]

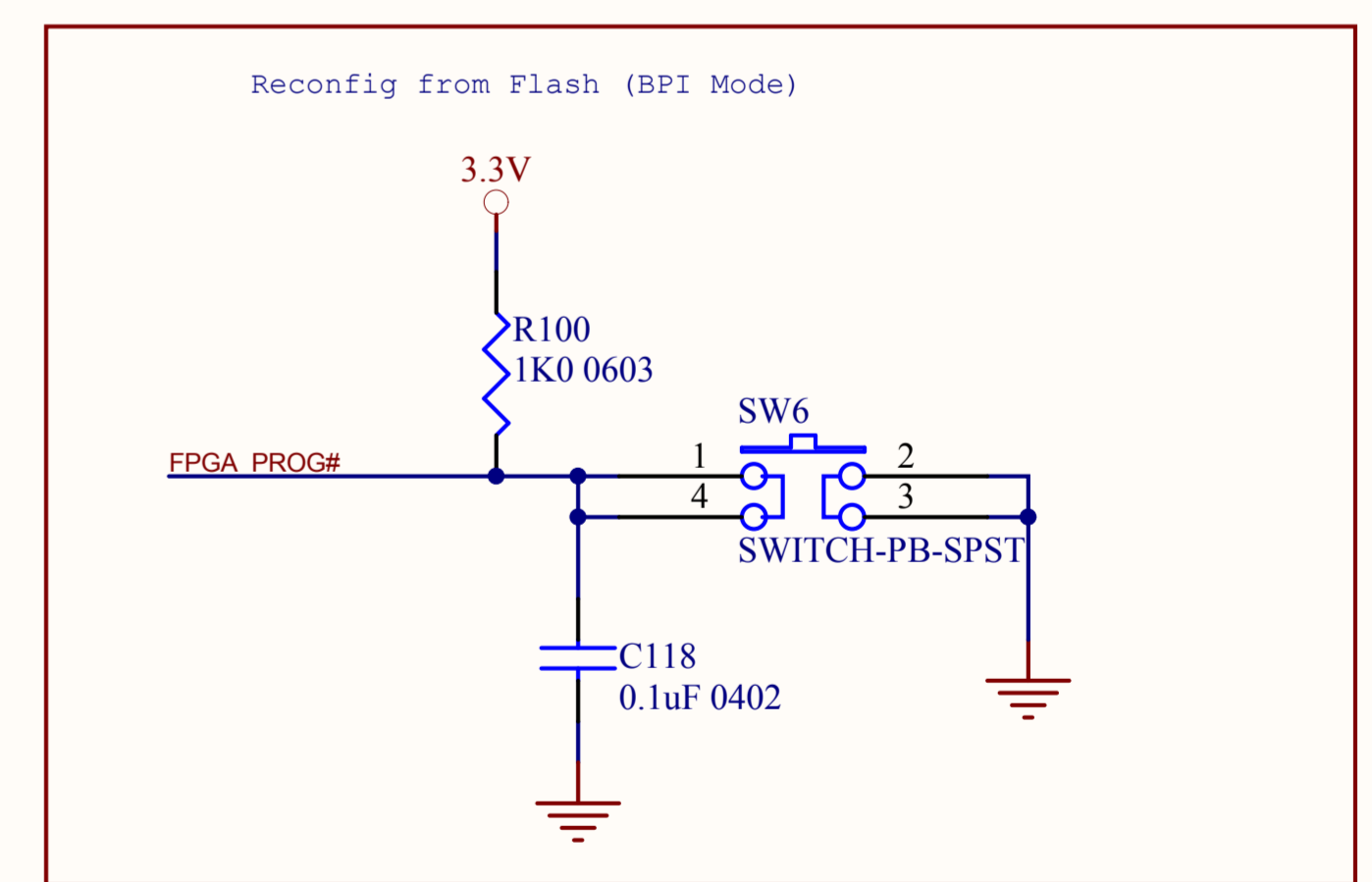
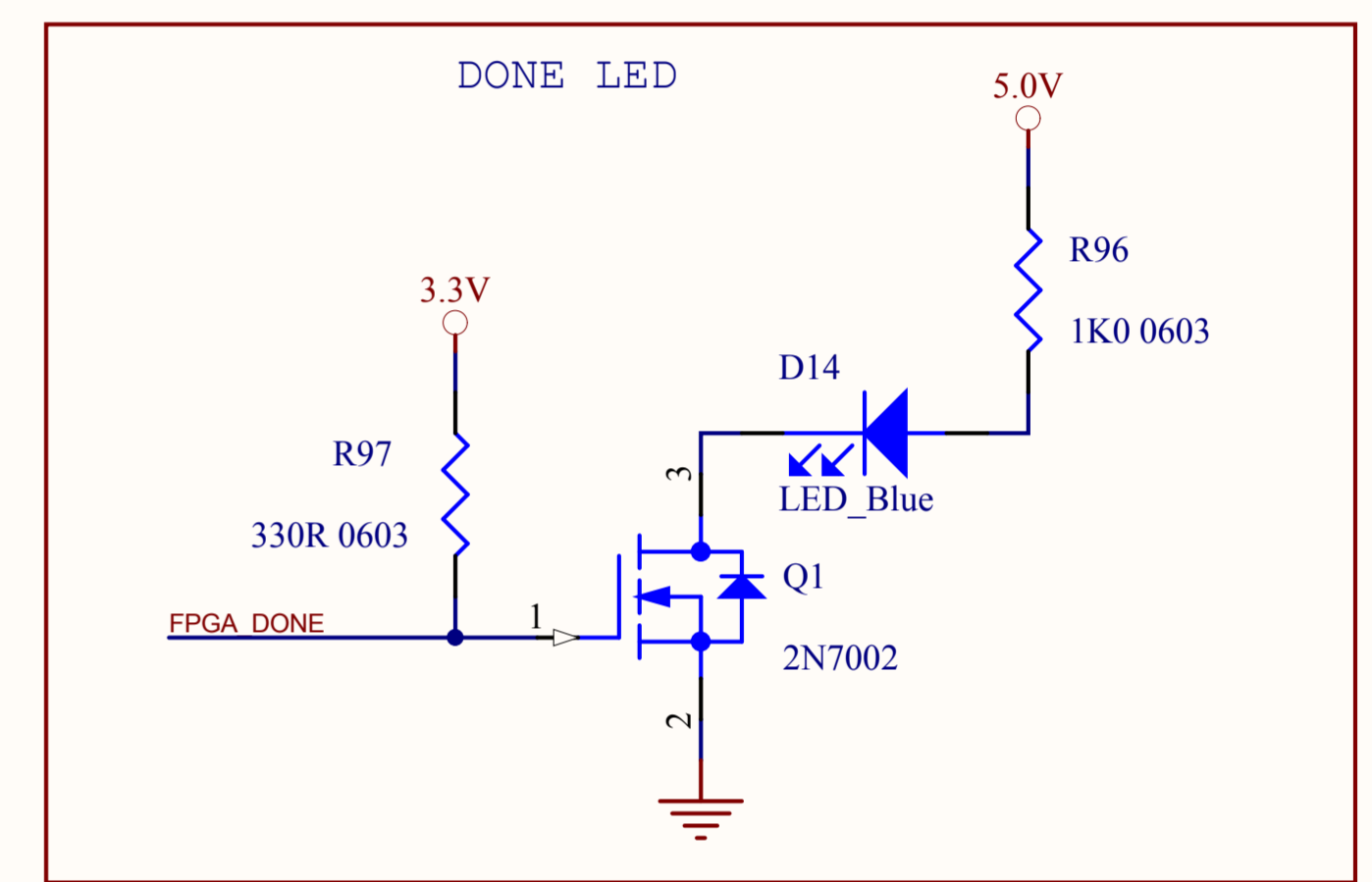
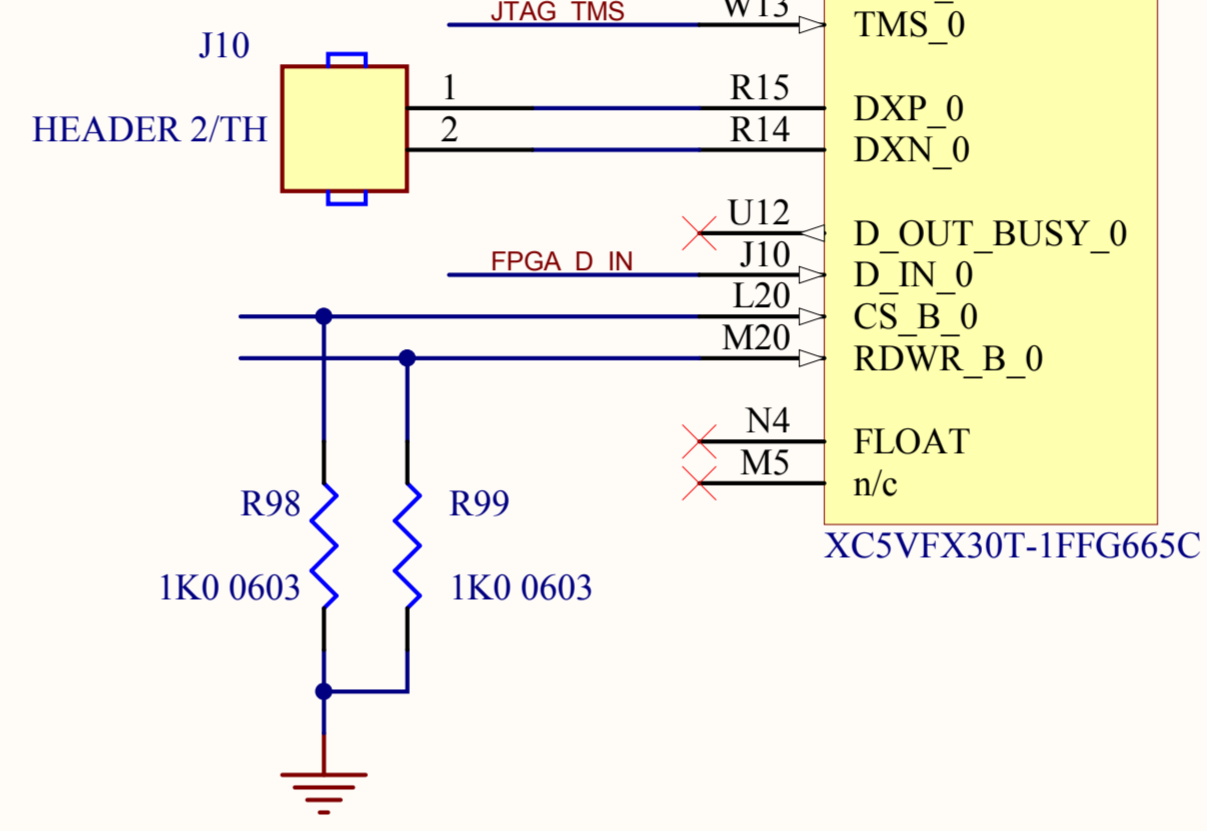
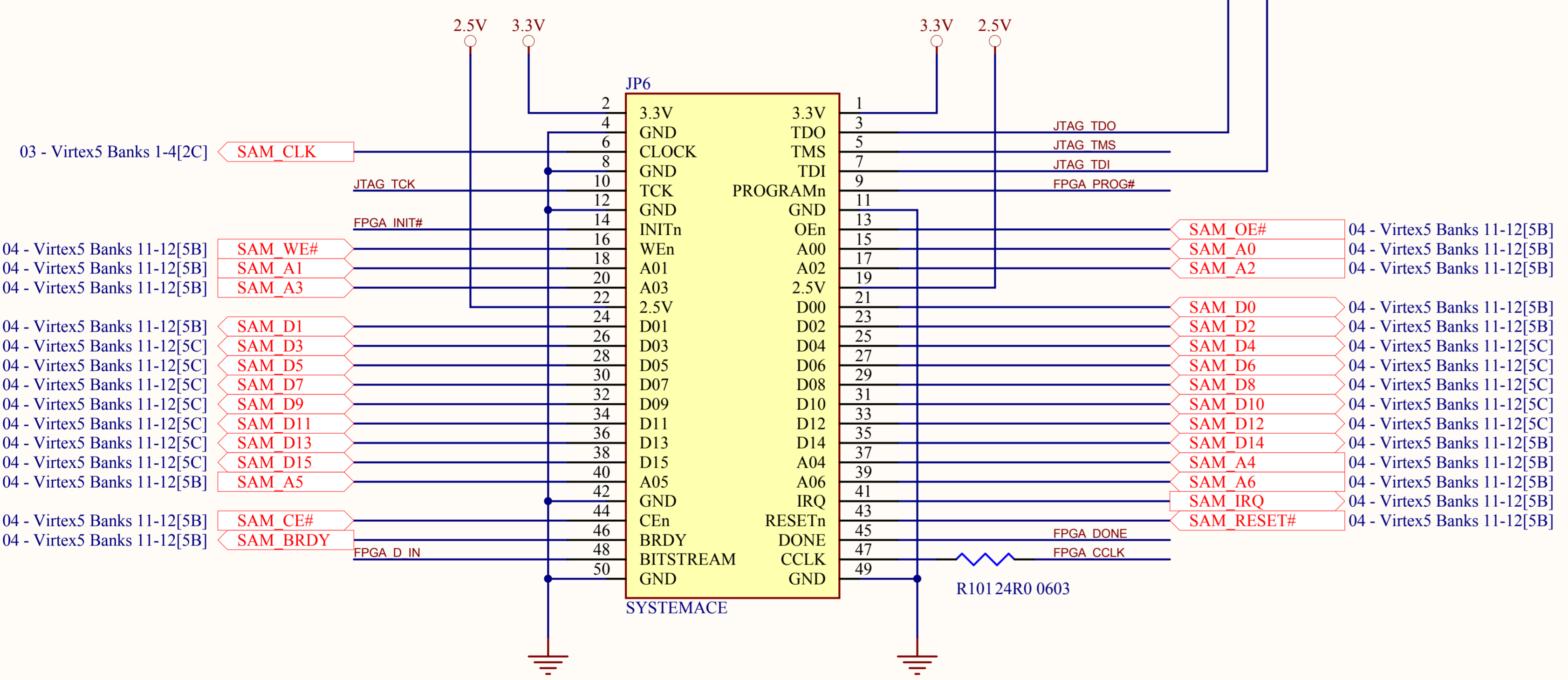
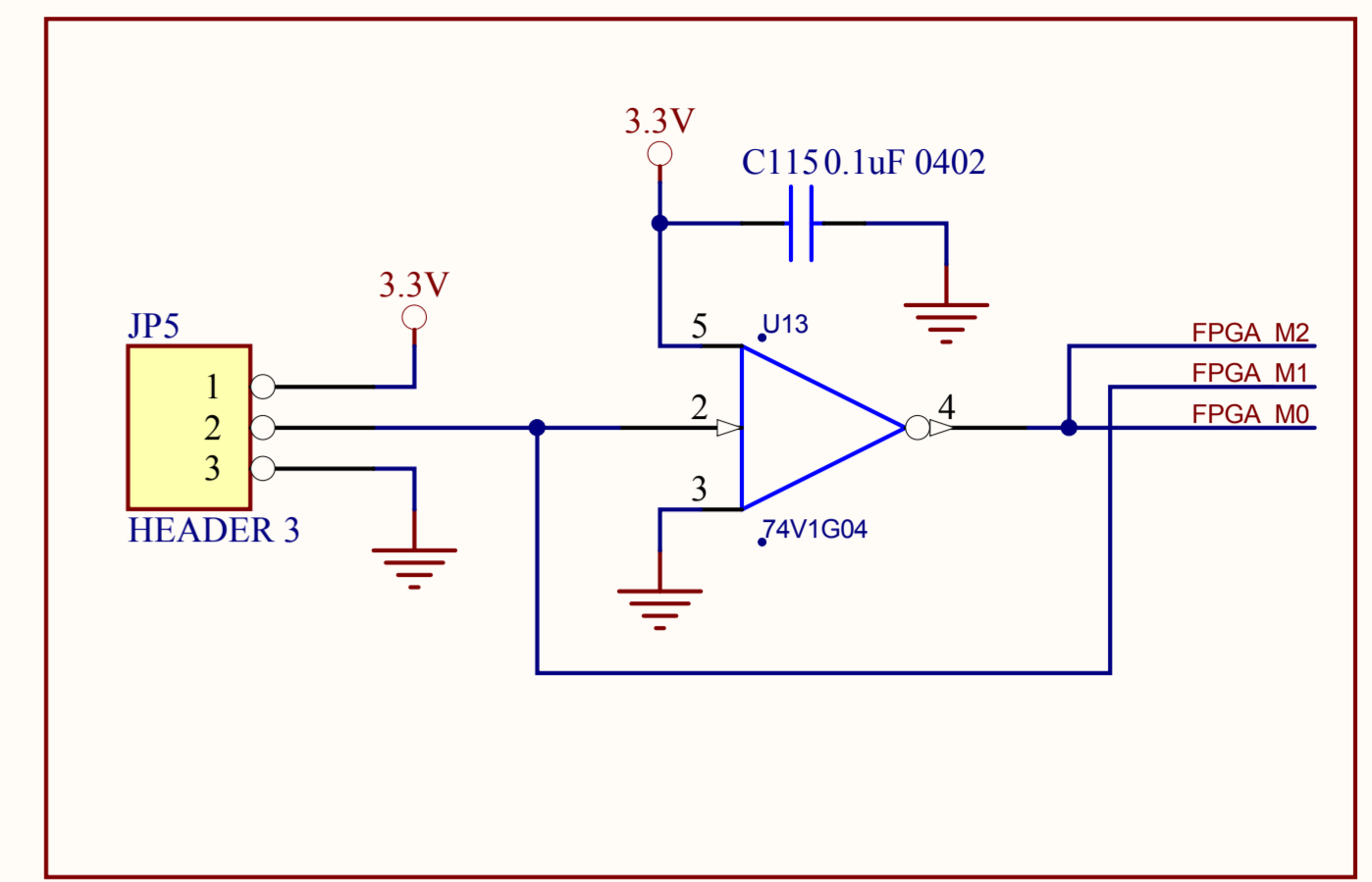
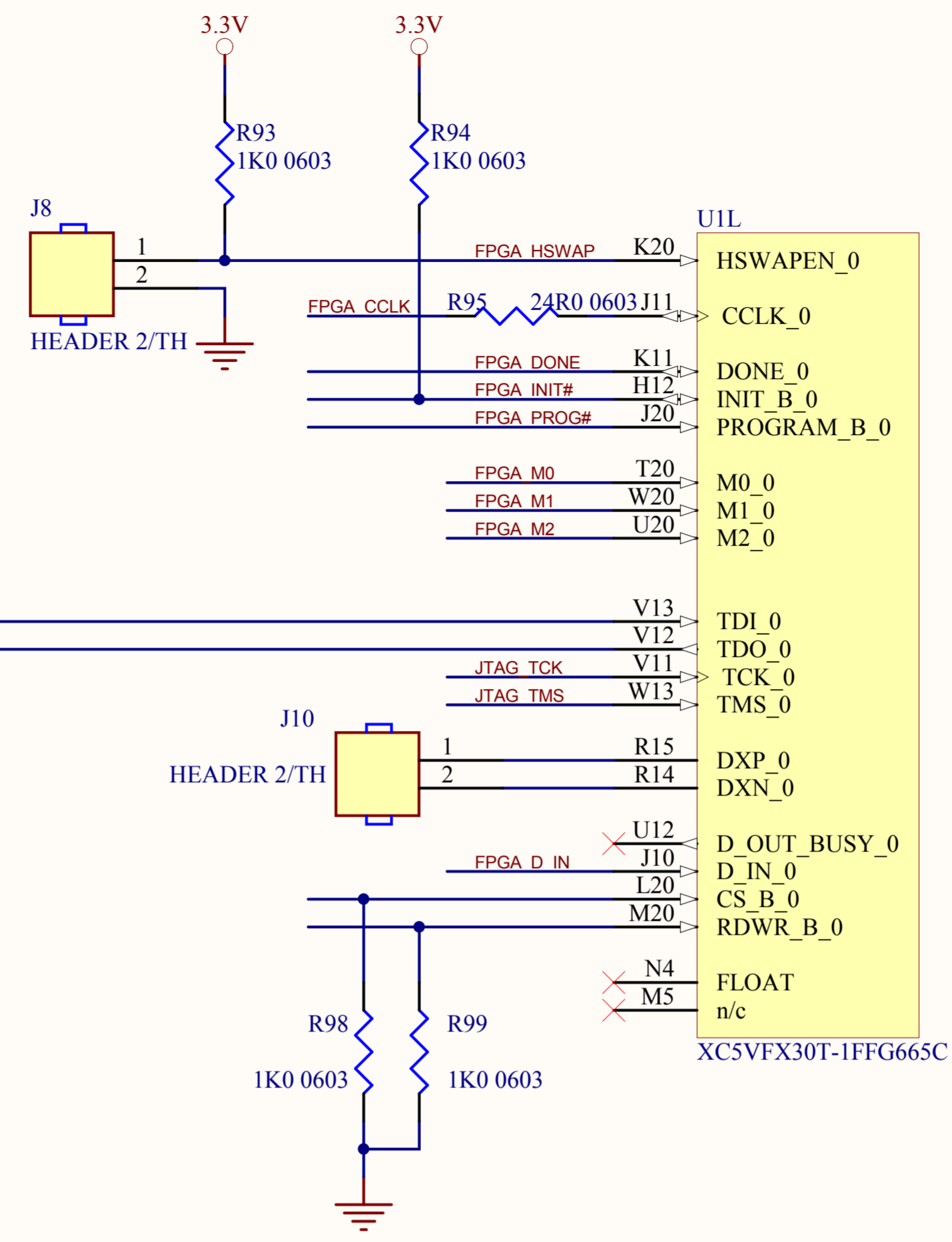
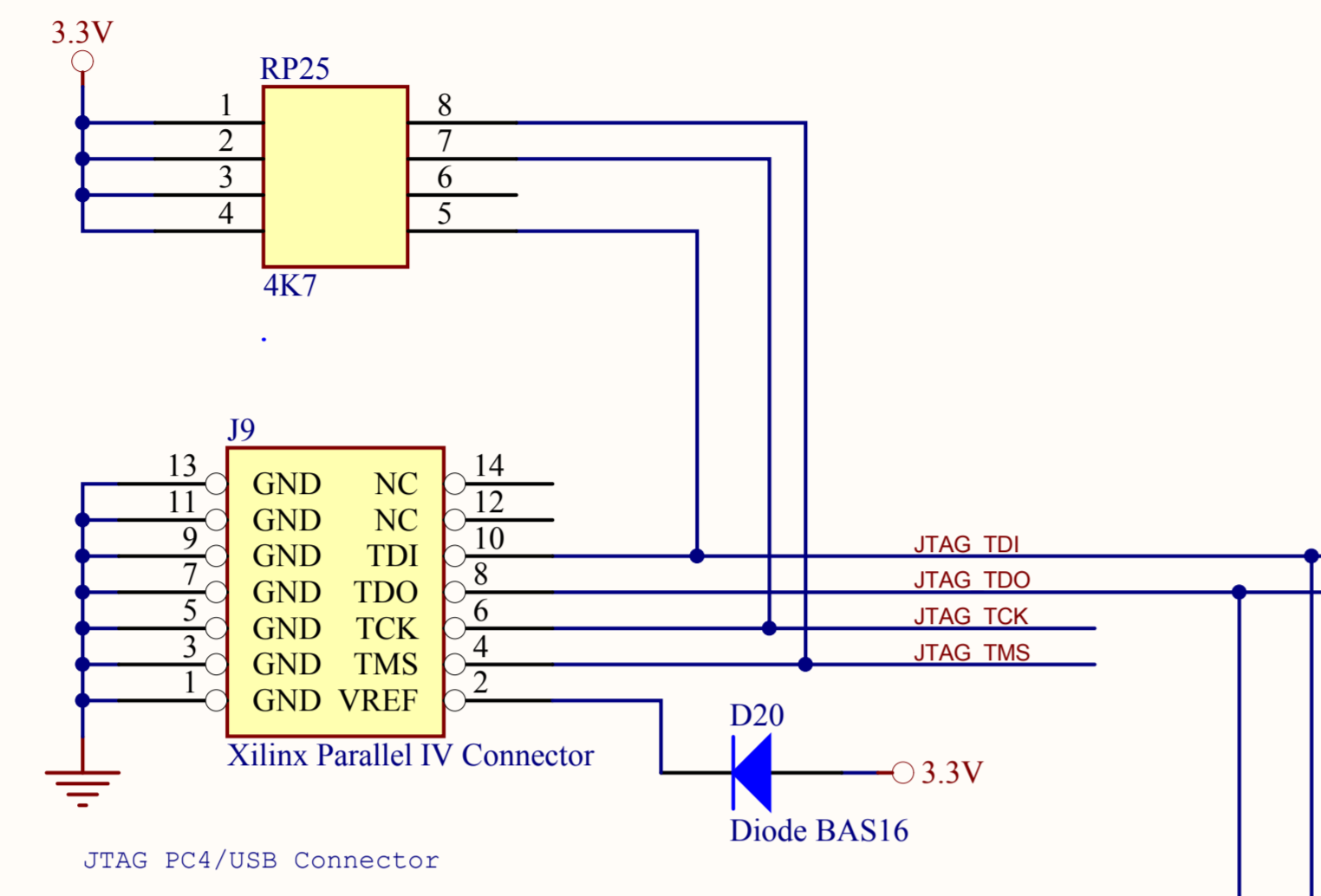
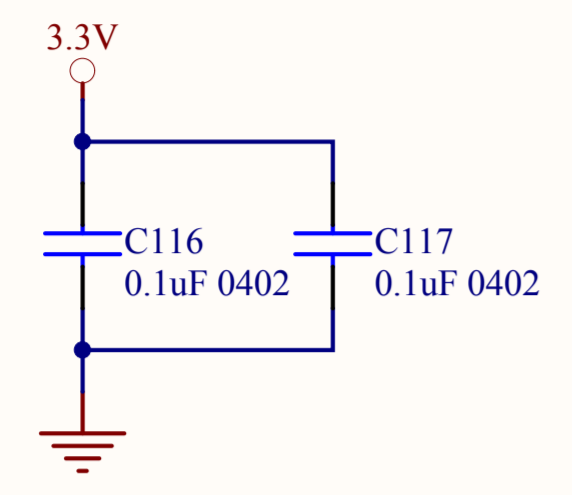
03 - Virtex5 Banks 1-4[5D], 07 - Virtex5 Bank 18[5A] EXP1_DIFF_n[0..21]

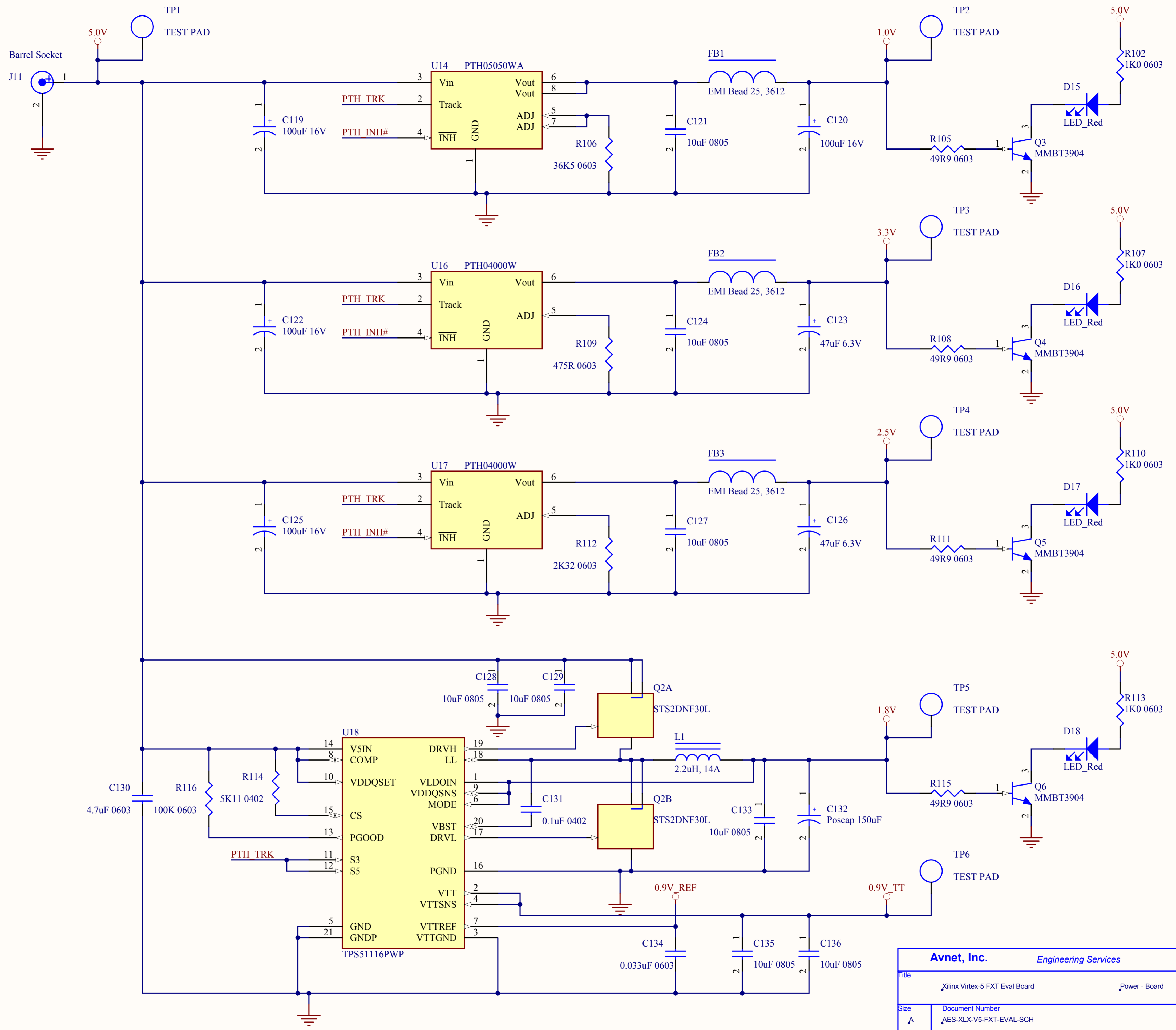
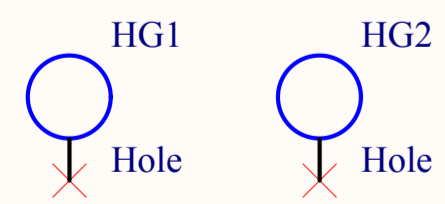
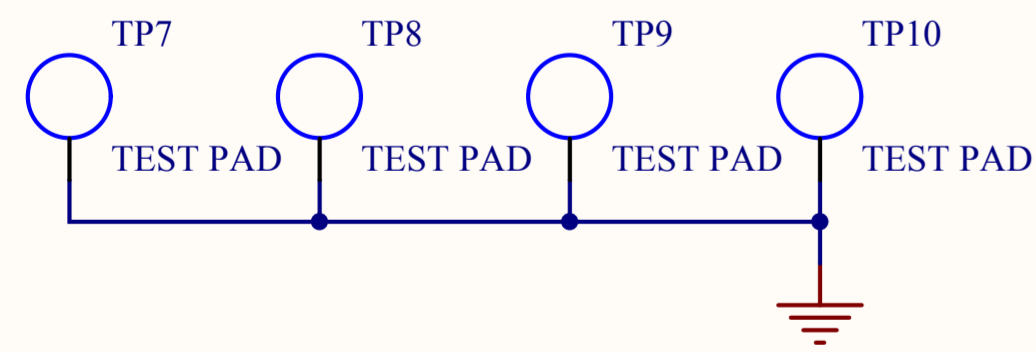
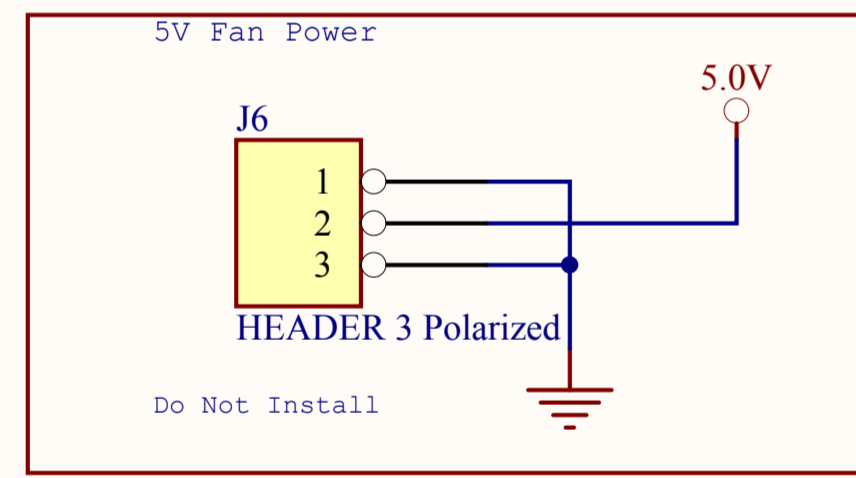
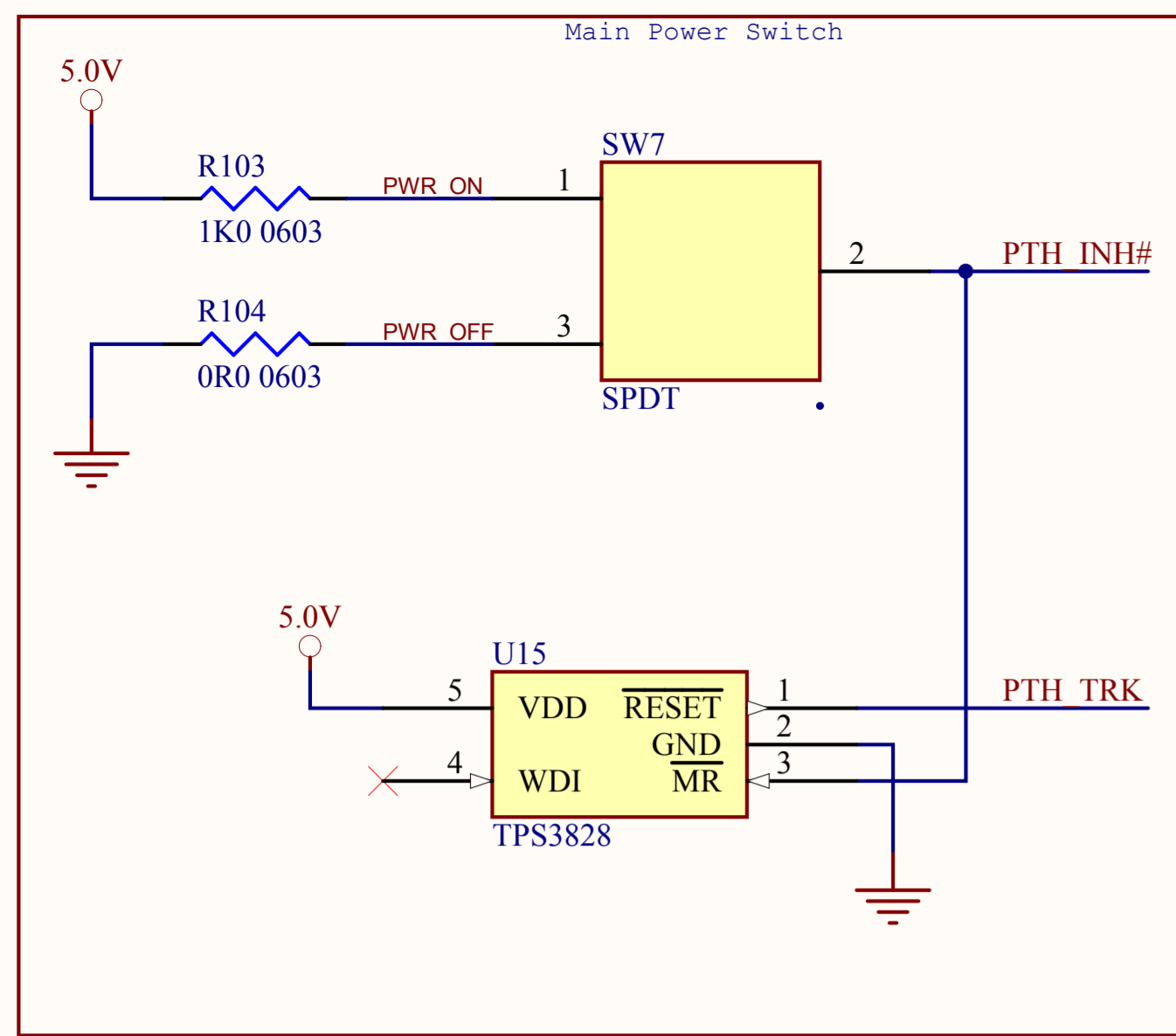


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