Xilinx® Virtex™ -5 FXT Evaluation Kit
User Guide

AVNET electronics marketing

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1.0 Introduction

The purpose of this manual is to describe the functionality and contents of the Virtex-5 FXT Evaluation Kit from Avnet Electronics Marketing. This document includes instructions for operating the board, descriptions of the hardware features and explanations of the test code programmed in the on-board flash.

1.1 Description

The Virtex-5 FXT Evaluation Kit provides a complete hardware environment for designers to accelerate their time to market. The kit delivers a stable platform to develop and test designs targeted to the advanced Xilinx FPGA family. The installed Virtex-5 FX30T device offers a prototyping environment to effectively demonstrate the enhanced benefits of leading edge Xilinx FPGA solutions. Reference designs are included with the kit to exercise standard peripherals on the development board for a quick start to device familiarization.

1.2 Board Features

FPGA

- Xilinx Virtex-5 XC5VFX30T-FF665 FPGA

I/O Connectors

- One EXP general-purpose I/O expansion connectors
- One 50-pin 0.1" Header supports Avnet System ACE Module (SAM)
- 16-pin 0.1" CPU debug header
- Mictor CPU Trace Port
- User Clock Inputs via Differential SMA Connectors

Memory

- 64 MB DDR2 SDRAM
- 16 MB FLASH

Communication

- RS-232 serial port
- USB-RS232 Port
- 10/100/1000 Ethernet PHY

Power

- Regulated 3.3V, 2.5V, and 1.0V supply voltages derived from an external 5V supply
- DDR2 termination (0.9V) and supply/reference voltage (1.8V) regulator.

Configuration

- Xilinx Parallel Cable IV or Platform USB Cable support for JTAG Programming/Configuration
- 16MB Intel BPI Flash

1.3 Test Files

The flash memory on the Virtex-5 FX30T Evaluation Board comes programmed with a factory test design that can be used as base tests for some of the peripherals on the board. The test designs listed below are discussed in Section 3.0. The factory test will test the following interfaces/peripherals:

- DDR2 memory
- Flash memory
- User LEDs
- User push-buttons

Other factory test designs for testing the Ethernet and USB-RS232 interfaces are available on the Avnet Design Resource Center web site (www.em.avnet.com/drc).

1.4 Reference Designs

Reference designs that demonstrate some of the potential applications of the board can be downloaded from the Avnet Design Resource Center (www.em.avnet.com/drc). The reference designs include all of the source code and project files necessary to implement the designs. See the PDF document included with each reference design for a complete description of the design and detailed instructions for running a demonstration on the evaluation board. Check the DRC periodically for updates and new designs.

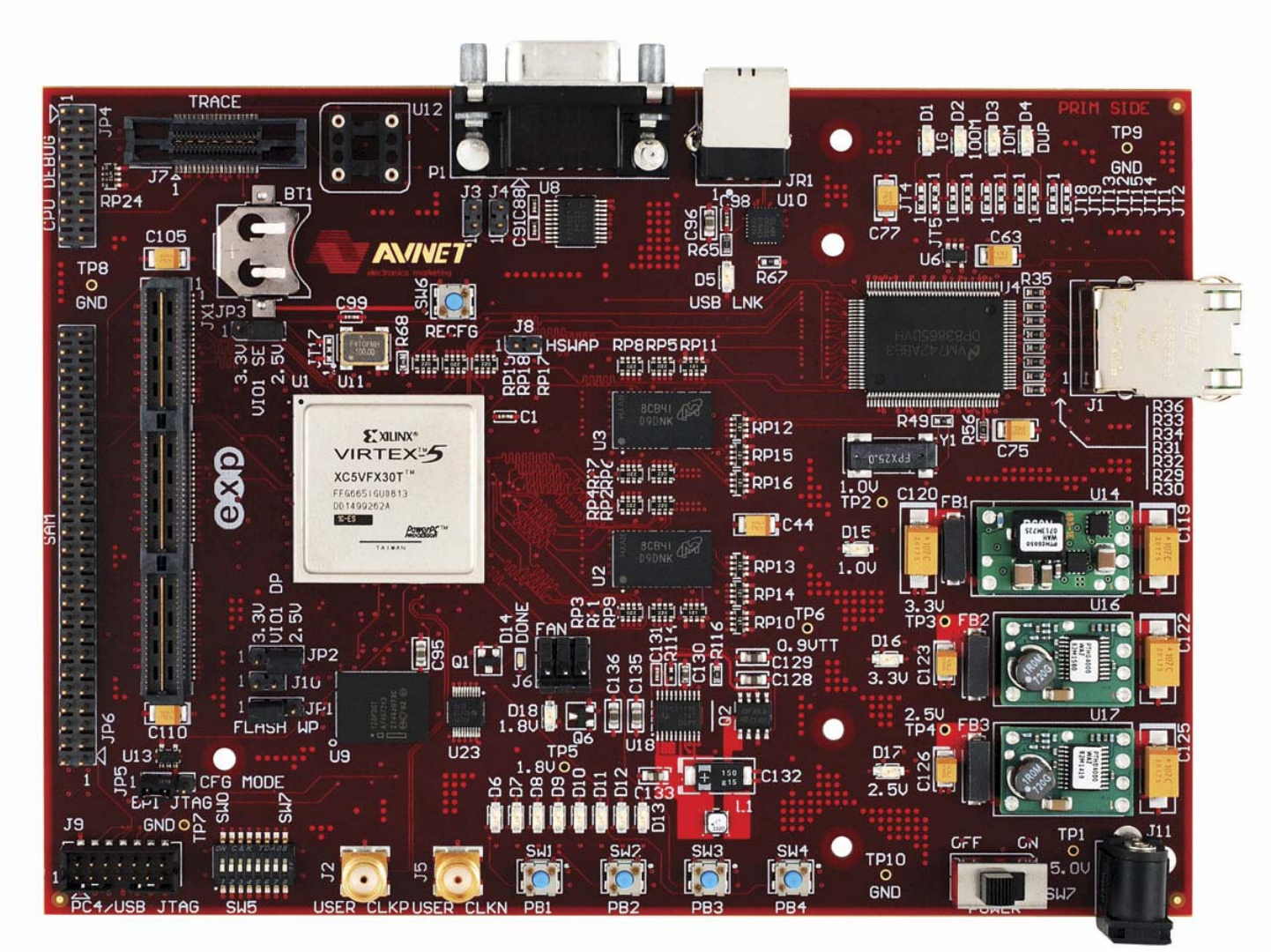


Figure 1 - Virtex-5 FXT Evaluation Board Picture

1.5 Ordering Information

The following table lists the development kit part number.
Internet link at http://www.em.avnet.com/drc

Part Number	Hardware
AES-V5FXT-EVL30-G	Xilinx Virtex-5 FXT Kit populated with an XC5VFX30T -1 speed grade device

Table 1 - Ordering Information

2.0 Functional Description

A high-level block diagram of the Virtex-5 FXT Evaluation board is shown below followed by a brief description of each sub-section.

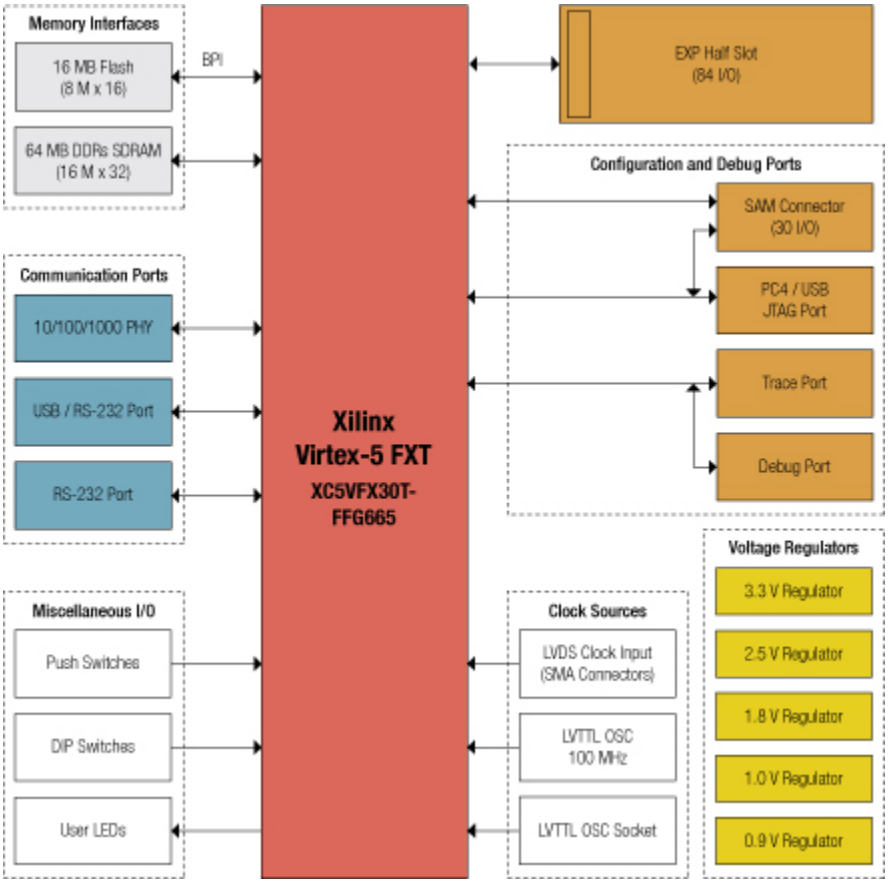


Figure 2 - Virtex-5 FXT Evaluation Board Block Diagram

2.1 Xilinx Virtex-5 FX30T FPGA

The Virtex-5 FX30T FPGA features 4 DCMs, 2 PLLs, and 1.25 Gbps LVDS I/O. The following table shows some other main features of the FF676 package.

Device	Number of Slices	BlockRAM (Kb)	DSP48E Slices
XC5VFX30T	5,120	2,448	64

Table 2 - XC5FX30T Features

Please refer to the Virtex-5 FX30T Data sheet for a complete detailed summary of all device features.

324 of the 360 available I/O on the Virtex-5 FX30T device are used in the design.

2.2 Memory

The Virtex-5 FXT Evaluation Board is populated with both high-speed RAM and non-volatile Flash to support various types of applications. The board has 64 Megabytes (MB) of DDR2 SDRAM and 16 MB of Flash. The following figure shows a high-level block diagram of the memory interfaces on the evaluation board. If additional memory is necessary for development, check the Avnet Design Resource Center (DRC) for the availability of EXP compliant daughter cards with expansion memory (sold separately). Here is the link to the DRC web page: www.em.avnet.com/drc.

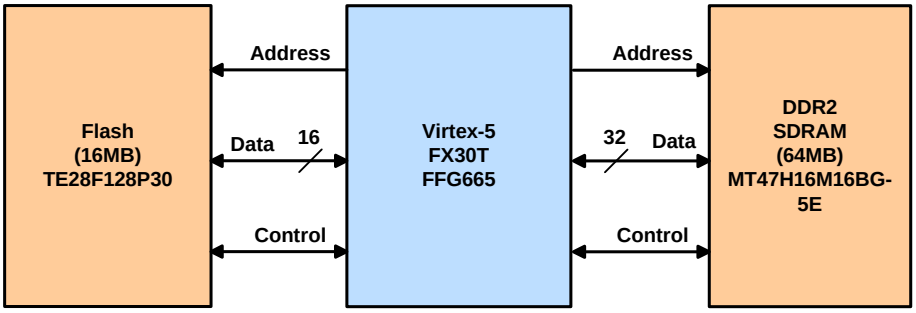


Figure 3 - Virtex-5 FXT Evaluation Board Memory Interfaces

2.2.1 DDR2 SDRAM Interface

Two Micron DDR2 SDRAM devices, part number **MT47H16M16BG-5E**, make up the 32-bit data bus. Each device provides 32MB of memory on a single IC and is organized as 4 Megabits x 16 x 4 banks (256 Megabit). The device has an operating voltage of 1.8V and the interface is JEDEC Standard SSTL_2 (Class I for unidirectional signals, Class II for bidirectional signals). The -5E speed grade supports 5 ns cycle times with a 3 clock read latency (DDR2-400). DDR2 On-Die-Termination (ODT) is also supported. The following figure shows a high-level block diagram of the DDR SDRAM interface on the Virtex-5 FXT Evaluation Board.

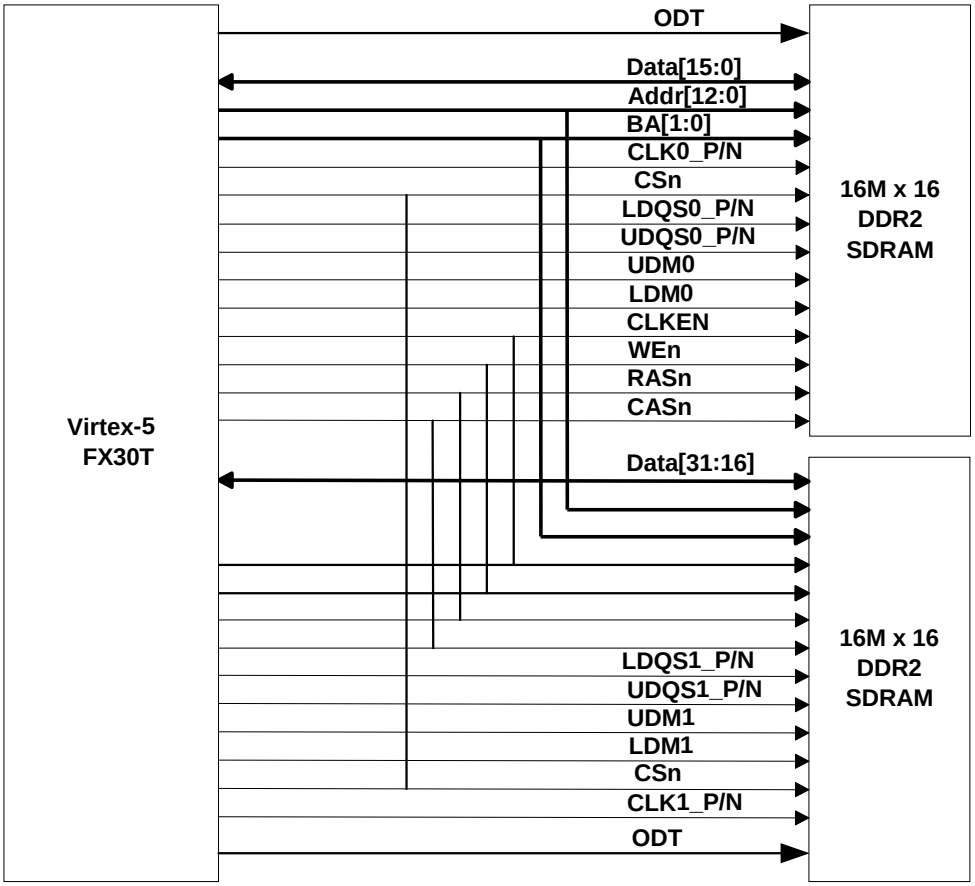


Figure 4 - DDR2 SDRAM Interface

The following table provides timing and other information about the Micron device necessary to implement a DDR2 memory controller.

MT47H16M16BG-5E: Timing Parameters	Time (ps) or Number
Load Mode Register time (TMRD)	25000
Write Recovery time (TWR)	15000
Write-to-Read Command Delay (TWTR)	1
Delay between ACT and PRE Commands (TRAS)	90000
Delay after ACT before another ACT (TRC)	65000
Delay after AUTOREFRESH Command (TRFC)	115000
Delay after ACT before READ/WRITE (TRCD)	25000
Delay after ACT before another row ACT (TRRD)	15000
Delay after PRECHARGE Command (TRP)	20000
Refresh Command Interval (TREFC)	115000
Avg. Refresh Period (TREFI)	7800000
Memory Data Width (DWIDTH) (x2 devices)	32
Row Address Width (AWIDTH)	13
Column Address Width (COL_AWIDTH)	9
Bank Address Width (BANK_AWIDTH)	2
Memory Range (64 MB total)	0x3FFFFFF

Table 3 - DDR2 SDRAM Timing Parameters

The following guidelines were used in the design of the DDR2 interface to the Virtex-5 FX30T FPGA. These guidelines are based on Micron recommendations and board level simulation.

- Dedicated bus with matched trace lengths (+/- 100 mils)
- Memory clocks routed differentially
- 50 ohm* controlled trace impedance
- Series termination on bidirectional signals at the memory device
- Parallel termination following the memory device connection on all signals
- 100 ohm* pull-up resistor to the termination supply on each branch of shared signals (control, address)
- Termination supply that can source both termination and reference voltages.

* Ideal impedance values. Actual may vary.

Some of the design considerations were specific to the Virtex-5 architecture. For example, the data strobe signals (DQS) were placed on Clock Capable I/O pins in order to support data capture techniques utilizing the SERDES function of the Virtex-5 I/O blocks. The appropriate DDR2 memory signals were placed in the clock regions that correspond to these particular Clock Capable I/O pins.

The DDR2 signals are connected to I/O Banks 11 and 13 of the Virtex-5 FX30T FPGA. The output supply pins (VCCO) for Banks 11 and 13 are connected to 1.8 Volts. This supply rail can be measured at test point TP5, which can be found in the area around the power modules. The reference voltage pins (VREF) for Banks 11 and 13 are connected to the reference output of the Texas Instruments TPS51116 DDR2 Power Solution Regulator. This rail provides the voltage reference necessary for the SSTL_2 I/O standard as well as the termination supply rail. The termination voltage is 0.9 Volts and can be measured at test point TP6.

The following table contains the FPGA pin numbers for the DDR2 SDRAM interface.

Signal Name	Virtex-5 pin		Signal Name	Virtex-5 pin
DDR_A0	U25		DDR_D0	R22
DDR_A1	T25		DDR_D1	R23
DDR_A2	T24		DDR_D2	P23
DDR_A3	T23		DDR_D3	P24
DDR_A4	U24		DDR_D4	R25
DDR_A5	V24		DDR_D5	P25
DDR_A6	Y23		DDR_D6	R26
DDR_A7	W23		DDR_D7	P26
DDR_A8	AA25		DDR_D8	M26
DDR_A9	AB26		DDR_D9	N26
DDR_A10	AB25		DDR_D10	K25
DDR_A11	AB24		DDR_D11	L24
DDR_A12	AA23		DDR_D12	K26
			DDR_D13	J26
			DDR_D14	J25
DDR_BA0	U21		DDR_D15	N21
DDR_BA1	V22			
			DDR_D16	M21
DDR_CS#	AD24		DDR_D17	J23
ODT	AF24		DDR_D18	H23
			DDR_D19	H22
DDR_WE#	AA22		DDR_D20	G22
DDR_RAS#	Y22		DDR_D21	F22
DDR_CAS#	W24		DDR_D22	F23
DDR_CLKEN	T22		DDR_D23	E23
DM0	U26		DDR_D24	G24
DM1	N24		DDR_D25	F24
DM2	M24		DDR_D26	G25
DM3	M25		DDR_D27	H26
			DDR_D28	G26
DQS0 P,N	W26, W25		DDR_D29	F25
DQS1 P,N	L23, L22		DDR_D30	E25
DQS2 P,N	K22, K23		DDR_D31	E26
DDR2_CLK0 P,N	V21, W21			
DDR2_CLK1 P,N	N22, M22			

Table 4 - Virtex-5 FXT DDR2 FPGA Pinouts

2.2.2 Flash Memory

The Virtex-5 FXT Evaluation Board has 16 MB of non-volatile flash memory on board. The flash device is made by Intel, part number: **PC28F128P30T85**. The flash memory interface utilizes a 16-bit data bus and can be accessed directly without any external hardware settings or jumpers. See the following table for the flash memory to Virtex-5 pinout.

Signal Name	Virtex-5 Pin		Signal Name	Virtex-5 Pin
FLASH_A0	Y11		FLASH_D0	AA15
FLASH_A1	H9		FLASH_D1	Y15
FLASH_A2	G10		FLASH_D2	W14
FLASH_A3	H21		FLASH_D3	Y13
FLASH_A4	G20		FLASH_D4	W16
FLASH_A5	H11		FLASH_D5	Y16
FLASH_A6	G11		FLASH_D6	AA14
FLASH_A7	H19		FLASH_D7	AA13
FLASH_A8	H18		FLASH_D8	AB12
FLASH_A9	G12		FLASH_D9	AC11
FLASH_A10	F13		FLASH_D10	AB20
FLASH_A11	G19		FLASH_D11	AB21
FLASH_A12	F18		FLASH_D12	AB11
FLASH_A13	F14		FLASH_D13	AB10
FLASH_A14	F15		FLASH_D14	AA20
FLASH_A15	F17		FLASH_D15	Y21
FLASH_A16	G17			
FLASH_A17	G14		FLASH_CE#	Y12
FLASH_A18	H13		FLASH_OE#	AA12
FLASH_A19	G16		FLASH_WE#	AA17
FLASH_A20	G15		FLASH_RST#	D13
FLASH_A21	Y18		FLASH_BYTE#	Y17
FLASH_A22	AA18		FLASH_WAIT#	D16
FLASH_A23	Y10		FLASH_ADV#	F19
FLASH_A24	W11			

Table 5 - Virtex-5 Flash Memory Pinout

2.3 Clock Sources

The Virtex-5 FXT Evaluation Board includes all of the necessary clocks on the board to implement designs as well as providing the flexibility for the user to supply their own application specific clocks. The clock sources described in this section are used to derive the required clocks for the memory and communications devices, and the general system clocks for the logic design. This section also provides information on how to supply external user clocks to the FPGA via the on-board connectors and oscillator socket.

The following figure shows the clock nets connected to the I/O banks containing the global clock input pins on the Virtex-5 FX30T FPGA. Ten out of the twenty global clock inputs of the Virtex-5 FPGA are utilized on the board as clock resources. The other global clock inputs are used for user I/O. It should be noted that single-ended clock inputs must be connected to the P-side of the pin pair because a direct connection to the global clock tree only exists on this pin. The I/O voltage (VCCO) for Bank 3 is set at 3.3V. Bank 4 is jumper selectable via JP2 to either 2.5V or 3.3V. In order to use the differential clock inputs as LVDS inputs, the VCCO voltage for the corresponding bank must be set for 2.5V since the Virtex-5 FPGA does not support 3.3V differential signaling. Single-ended clock inputs do not have this restriction and may be either 2.5V or 3.3V. The interface clocks and other I/O signals coming from 3.3V devices on the board are level-shifted to the appropriate VCCO voltage by CB3T standard logic devices prior to the Virtex-5 input pins.

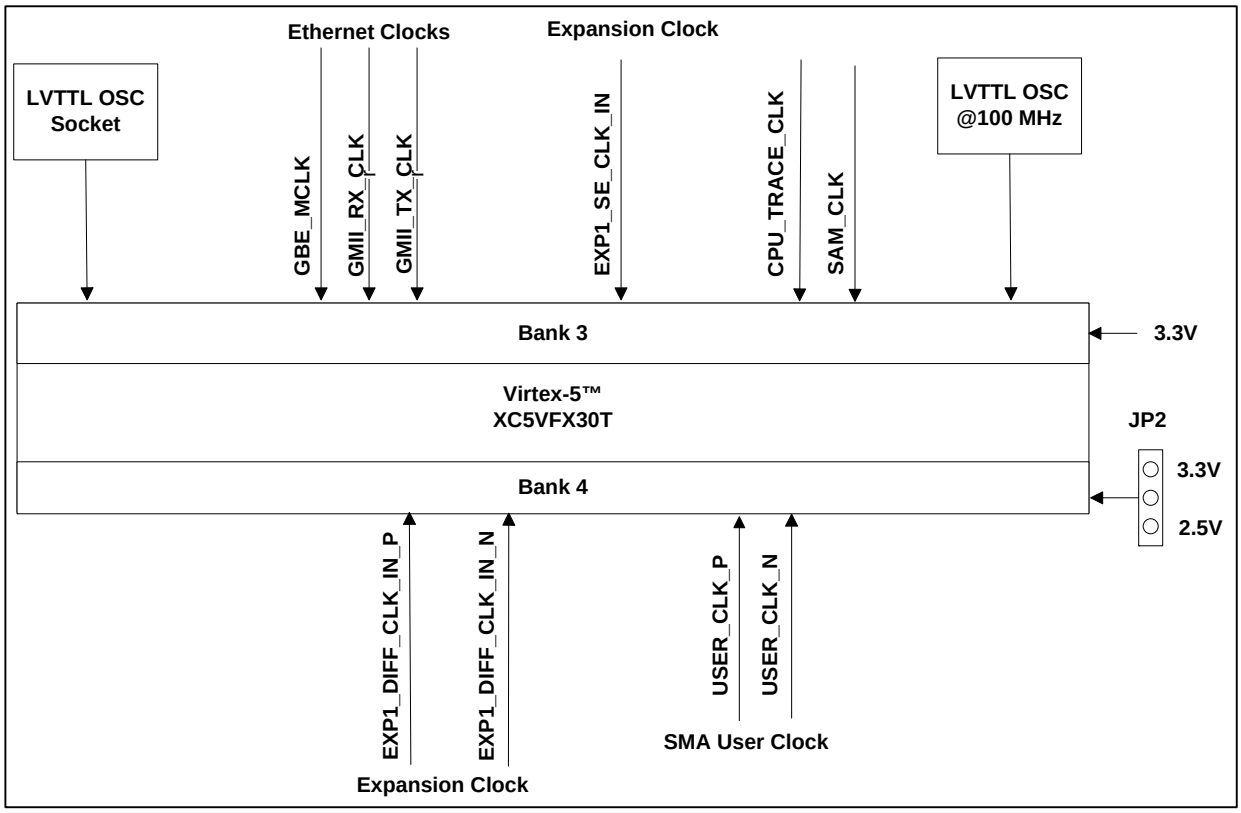


Figure 5 - Clock Nets Connected to Global Clock Inputs

The on-board 100MHz oscillator provides the system clock input to the global clock tree. This single-ended, 100 MHz clock can be used in conjunction with the Virtex-5 Digital Clock Managers (DCMs) to generate the various processor clocks and the clocks forwarded to the DDR SDRAM devices. The interface clocks supplied by the communications devices are derived from dedicated crystal oscillators.

Reference#	Frequency	Derived Interface Clock	Derived Frequency	Virtex-5 pin#
U11	100 MHz	CLK_100MHZ	100 MHz	E18
U12 (sckt)	User defined	User Defined	User Defined	E13
J2, J5	User Defined	User Defined	User Defined	AB15. AB16
		GMII_RX_CLK	2.5, 25, 125 MHz	E20
		GMII_TX_CLK		E17
Y1	25 MHz	GBE_MCLK	125 MHz	F20

Table 6 - On-Board Clock Sources

The clock socket is an 8-pin DIP clock socket that allows the user to select an oscillator of choice. The socket is a single-ended, LVTTL or LVCMOS compatible clock input to the FPGA that can be used as an alternate source for the system clock.

Signal Name	Socket pin#
Enable	1
GND	4
Output	5
VDD	8

Table 7 - Clock Socket "U12" Pin-out

Net Name	Input Type	Connector.pin#	Virtex-5 pin#
CLK_SOCKET	Global clock	U16.5	E13

Table 8 - User Clock Input

2.4 Communication

The Virtex-5 FX30T FPGA has access to Ethernet and RS232 physical layer transceivers for communication purposes. Network access is provided by a 10/100/1000 Mb/s Ethernet PHY, which is connected to the Virtex-5 via a standard GMII interface. The PHY connects to the outside world with a standard RJ45 connector (J1) and is located in the upper right corner of the board.

A USB compatible RS232 transceiver is available for use as well. The USB Type B peripheral connector (JR1) is mounted on the top right corner of the board. A second, standard DB9 Serial port (P1) to the embedded processor or FPGA fabric is provided through a dual-channel RS232 transceiver.

2.4.1 10/100/1000 Ethernet PHY

The PHY is a National DP83865DVH Gig PHYTER® V. The DP83865 is a low power version of National's Gig PHYTER V with a 1.8V core voltage and 3.3V I/O voltage. The PHY also supports 2.5V I/O, but the 2.5V option is used on the board. The PHY is connected to a Tyco RJ-45 jack with integrated magnetics (part number: 1-6605833-1). The jack also integrates two LEDs and their corresponding resistors as well as several other passive components. External logic is used to logically OR the three link indicators for 10, 100 and 1000 Mb/s to drive a Link LED on the RJ-45 jack. The external logic is for the default strap options and may not work if the strap options are changed. Four more LEDs are provided on the board for status indication. These LEDs indicate lnk at 10 Mb/s, link at 100 Mb/s, link at 1000 Mb/s and Full Duplex operation. The PHY clock is generated from its own 25 MHz crystal. The following figure shows a high-level block diagram of the interface to the DP83865 Tri-mode Ethernet PHY.

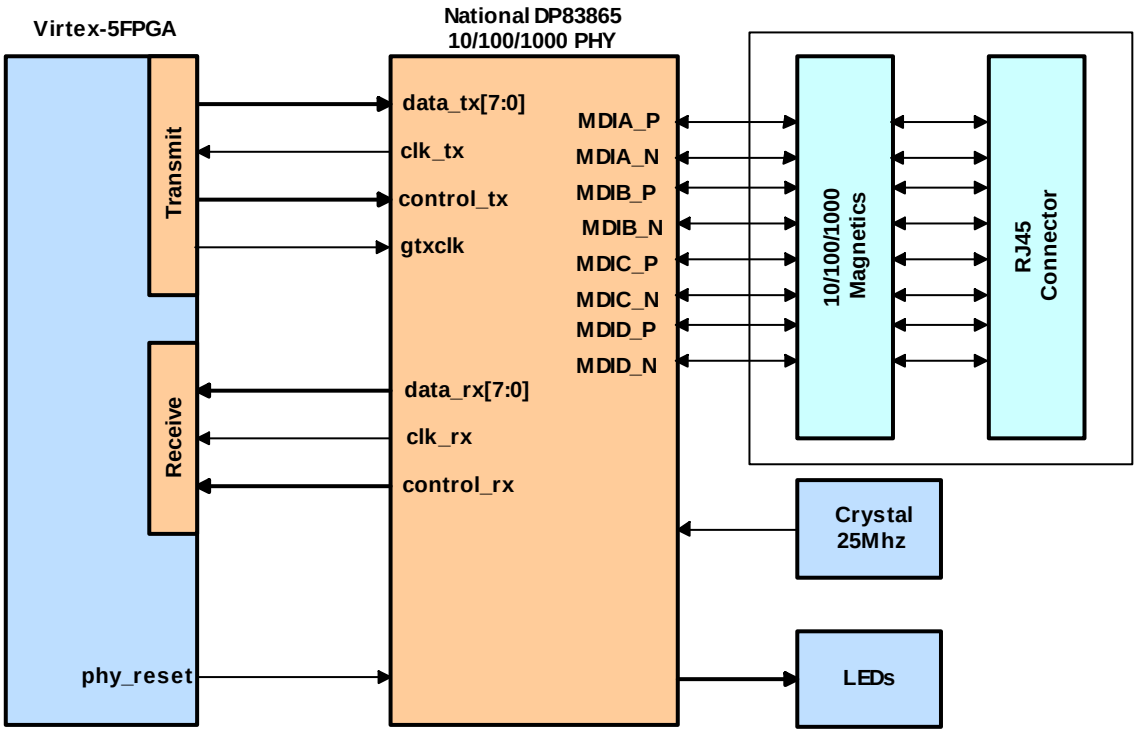


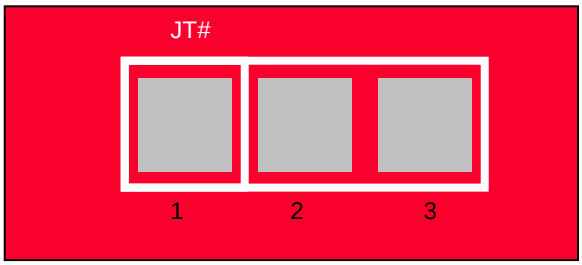
Figure 6 - 10/100/1000 Mb/s Ethernet Interface

The PHY address is set to 0b00001 by default. PHY address 0b00000 is reserved for a test mode and should not be used. Three-pad resistor jumpers are used to set the strapping options. These jumper pads provide the user with the ability to change the settings by moving the resistors. The strapping options are shown in the following table. The dual-function pins that are used for both a strapping option and to drive an LED, have a set of two jumpers per pin. The dual-function pins are indicated by an asterisk in the table.

Function	Jumper Installation	Resistor	Mode Enabled
Auto-Negotiation*	JT4: pins 1-2 JT5: pins 1-2	0 ohm 0 ohm	Auto-negotiation enabled (default)
	JT4: pins 2-3 JT5: pins 2-3	0 ohm 0 ohm	Auto-negotiation disabled
Full/Half Duplex*	JT8: pins 1-2 JT9: pins 1-2	0 ohm 0 ohm	Full Duplex (default)
	JT8: pins 2-3 JT9: pins 2-3	0 ohm 0 ohm	Half Duplex
Speed 1*	JT1: pins 1-2 JT2: pins 1-2	0 ohm 0 ohm	Speed Selection: (Auto-Neg enabled) Speed1 Speed0 Speed Advertised 1 1 1000BASE-T, 10BASE-T 1 0 1000BASE-T 0 1 1000BASE-T, 100BASE-TX 0 0 1000BASE-T, 100BASE-TX, 10BASE-T Default: 1000BASE-T, 100BASE-TX, 10BASE-T
Speed 0*	JT1: pins 1-2 JT2: pins 1-2	0 ohm 0 ohm	
PHY address 0*	JT9: pins 1-2 JT10: pins 1-2	0 ohm 0 ohm	PHY Address 0b00001 (default)
	JT9: pins 2-3 JT10: pins 2-3	0 ohm 0 ohm	PHY Address 0b00000
Non-IEEE Compliant Mode	JT6: pins 1-2	1 K	Compliant and Non-comp. Operation (default)
	JT6: pins 2-3	1 K	Inhibits Non-compliant operation
Manual MDIX Setting	JT10: pins 1-2	1 K	Straight Mode (default)
	JT10 pins 2-3	1 K	Cross-over Mode
Auto MDIX Enable	JT11: pins 1-2	1 K	Automatic Pair Swap – MDIX (default)
	J11: pins 2-3	1 K	Set to manual preset – Manual MDIX Setting (JT12)
Multiple Node Enable	JT7: pins 1-2	1 K	Single node – NIC (default)
	JT7: pins 2-3	1 K	Multiple node priority – switch/hub
Clock to MAC Enable	JT3: pins 1-2	1 K	CLK_TO_MAC output enabled (default)
	JT3: pins 2-3	1 K	CLK_TO_MAC output disabled

Table 9 - Ethernet PHY Hardware Strapping Options

The default options as indicated in Table 23 are Auto-Negotiation enabled, Full Duplex mode, speed advertised as 10/100/1000 Mb/s, PHY address 0b00001, IEEE Compliant and Non-compliant support, straight cable in non-MDIX mode, auto-MDIX mode enabled, Single node (NIC) and CLK_TO_MAC enabled. The pin-out for a jumper pad is shown below.



The auto-MDIX mode provides automatic swapping of the differential pairs. This allows the PHY to work with either a straight-through cable or crossover cable. Use a CAT-5e or CAT-6 Ethernet cable when operating at 1000 Mb/s (Gigabit Ethernet). The boundary-scan Test Access Port (TAP) controller of the DP83865 must be in reset for normal operation. This active low reset pin of the TAP (TRST) is pulled low through a 1K resistor on the board. The following table provides the Virtex-5 pin assignments for the Ethernet PHY interface.

Net Name	Virtex-5 pin		Net Name	Virtex-5 pin
GBE_MDC	D26		GBE_INT#	C24
GBE_MDIO	D25		GBE_RST#	B26
GBE_MCLK	F20		GMII_CRS	A25
GMII_GTC_CLK	A19		GMII_COL	A24
GMII_TXD0	D19		GMII_RXD0	D24
GMII_TXD1	C19		GMII_RXD1	D23
GMII_TXD2	A20		GMII_RXD2	D21
GMII_TXD3	B20		GMII_RXD3	C26
GMII_TXD4	B19		GMII_RXD4	D20
GMII_TXD5	A15		GMII_RXD5	C23
GMII_TXD6	B22		GMII_RXD6	B25
GMII_TXD7	B21		GMII_RXD7	C22
GMII_TX_EN	A23		GMII_RX_DV	C21
GMII_TX_ER	A22		GMII_RX_ER	B24
GMII_TX_CLK	E17		GMII_RX_CLK	E20

Table 10 - Ethernet PHY Pin Assignments

2.4.2 Universal Serial Bus (USB) to UART Bridge Transceiver

The Virtex-5 FXT Evaluation Board utilizes a SiLabs CP2120 USB to UART transceiver to support PC's that do not support the standard DB9 serial COM port. The diagram below shows how the CP2120 interfaces to the FPGA.

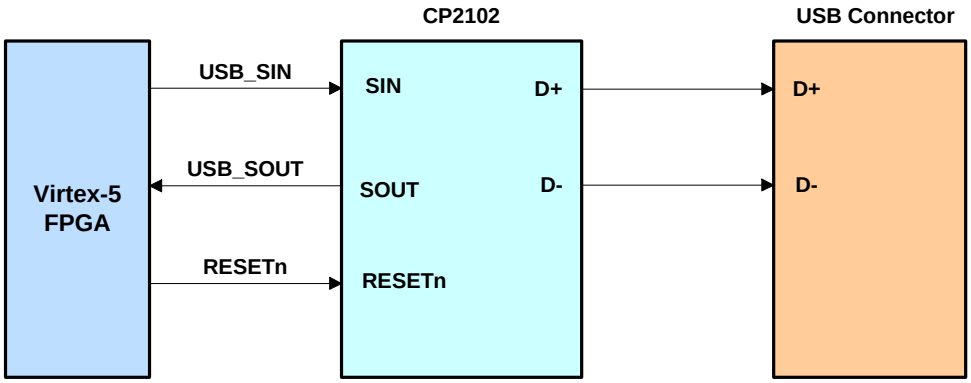


Figure 7 - USB to UART Transceiver Interface

Signal Name	Virtex-5 Pin
USB_RS232_TXD	AA19
USB_RS232_RXD	AA10
USB_RS232_RST#	Y20

Table 11 - USB to UART Interface FPGA Pin-out

2.4.3 RS232

The RS232 transceiver is a 3222 available from Harris/Intersil (ICL3222CA) and Analog Devices (ADM3222). This transceiver operates at 3.3V with an internal charge pump to create the RS232 compatible output levels. This level converter supports two channels. The primary channel is used for transmit and receive data (TXD and RXD). The secondary channel may be connected to the FPGA by installing jumpers on "J3" and "J4" for use as CTS and RTS signals. The RS232 console interface is brought out on the DB9 connector labeled "P1".

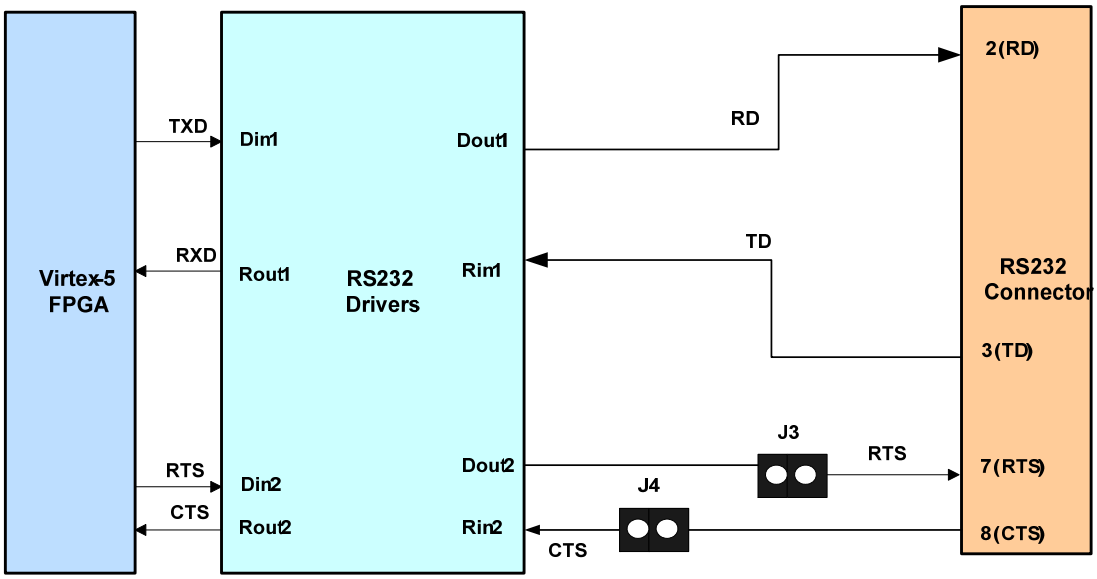


Figure 8 - RS232 Interface

A male-to-female serial cable should be used to plug “P1” into a standard PC serial port (male DB9). The following table shows the FPGA pin-out and jumper settings for the RS232 interface.

Net Name	Description	Virtex-5 Pin
RS232_RXD	Received Data, RD	K8
RS232_TXD	Transmit Data, TD	L8
RS232_RTS	Request To Send, RTS	N8
RS232_CTS	Clear To Send, CTS	R8

Table 12 - RS232 Signals

2.5 User Switches

Four momentary closure push buttons have been installed on the board and connected to the FPGA. These buttons can be programmed by the user and are ideal for logic reset and similar functions. Pull down resistors hold the signals low until the switch closure pulls it high (active high signals).

Net Name	Reference	Virtex-5 Pin
SWITCH_PB1	SW1	AF20
SWITCH_PB2	SW2	AE20
SWITCH_PB3	SW3	AD19
SWITCH_PB4	SW4	AD20

Table 13 - Push-Button Pin Assignments

An eight-position dipswitch (SPST) has been installed on the board and connected to the FPGA. These switches provide digital inputs to user logic as needed. The signals are pulled low by 1K ohm resistors when the switch is open and tied high to 1.8V when flipped to the ON position.

Net Name	Reference	Virtex-5 Pin
SWITCH0	SW5 – 0	AD13
SWITCH1	SW5 – 1	AE13
SWITCH2	SW5 – 2	AF13
SWITCH3	SW5 – 3	AD15
SWITCH4	SW5 – 4	AD14
SWITCH5	SW5 – 5	AF14
SWITCH6	SW5 – 6	AE15
SWITCH7	SW5 – 7	AF15

Table 14 - DIP Switch Pin Assignments

2.6 User LEDs

Eight discrete LEDs are installed on the board and can be used to display the status of the internal logic. These LEDs are attached as shown below and are lit by forcing the associated FPGA I/O pin to a logic '0' or low and are off when the pin is logic level '1' or high.

Net Name	Reference	Virtex-5 Pin#
LED0	D6	AF22
LED1	D7	AF23
LED2	D8	AF25
LED3	D9	AE25
LED4	D10	AD25
LED5	D11	AE26
LED6	D12	AD26
LED7	D13	AC26

Table 15 - LED Pin Assignments

2.7 Configuration and Debug Ports

2.7.1 Configuration Modes

The Virtex-5 FXT Evaluation Board supports three methods of configuring the FPGA. The possible configuration methods include Boundary-scan (JTAG cable), BPI Flash, and the System ACE Module (SAM) header. The Virtex-5 device also supports configuration from BPI Flash. The blue LED labeled "DONE" on the board illuminates to indicate when the FPGA has been successfully configured.

JP5 is the mode jumper that is used to tell the FPGA to configure in JTAG mode or Flash BPI mode. In JTAG mode a Xilinx parallel JTAG cable must be used (PC4 or USB). When the jumper is set for BPI mode, the flash must be programmed with a BPI-UP image in order for the FPGA to successfully configure. For configuration from a System ACE Module, the JTAG setting must be used.

The Virtex-5 FXT Evaluation Board come pre-programmed with the factory test image in the BPI flash. The table below shows the correct jumper configuration for each configuration mode.

Configuration Mode	JP5 Position
JTAG	2-3
System ACE	2-3
BPI-UP *	1-2

Table 16 - FPGA Configuration Modes

*Default assembled state

2.7.2 System ACE™ Module Connector

The Virtex-5 FXT Evaluation Board provides support for the Avnet System ACE Module (SAM) via the 50-pin connector labeled "JP6" on the board. The SAM can be used to configure the FPGA or to provide bulk Flash to the processor. This interface gives software designers the ability to run real-time operating systems (RTOS) from removable CompactFlash cards. The Avnet System ACE module (DS-KIT-SYSTEMACE) is sold separately. The figure below shows the System ACE Module connected to the header on the Virtex-5 FXT Evaluation Board.

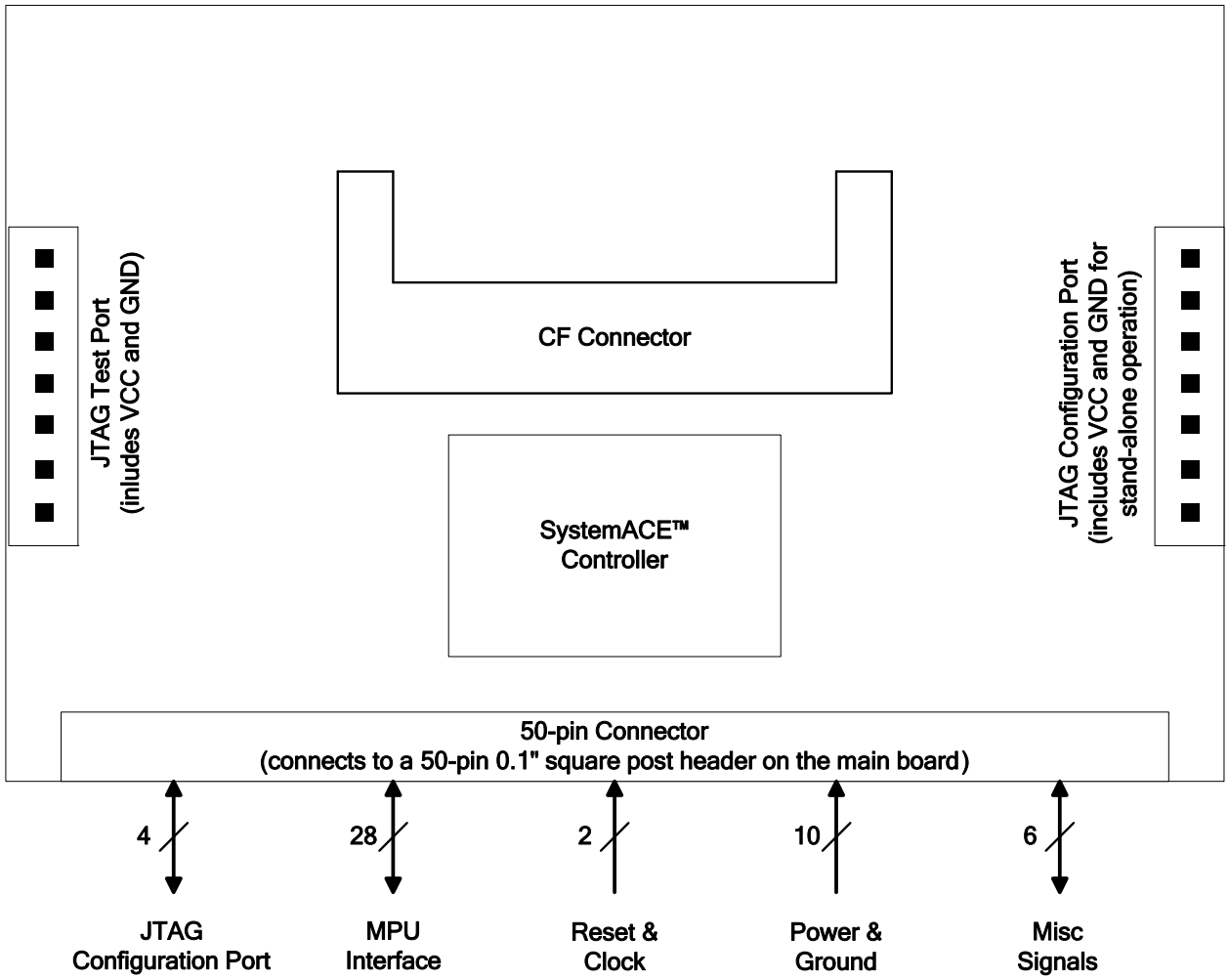


Figure 9 - SAM Interface (50-pin header)

The following table shows the System ACE ports that are accessible over the SAM header. The majority of the pins on this header may be used as general purpose I/O when not using a System ACE Module. The Virtex-5 pin numbers are provided for these general purpose pins.

Virtex-5 Pin	System ACE Signal Name	SAM Connector Pin # (JP11)		System ACE Signal Name	Virtex-5 Pin
-	**3.3V**	1	2	**3.3V**	**-**
-	JTAG_TDO	3	4	**GND**	**-**
-	JTAG_TMS	5	6	SAM_CLK	F12
-	JTAG_TDI	7	8	**GND**	**-**
-	FPGA_PROG#	9	10	JTAG_TCK	-
-	**GND**	11	12	**GND**	**-**
Y6	SAM_OE#	13	14	FPGA_INIT#	-
Y5	SAM_A0	15	16	SAM_WE#	Y4
W6	SAM_A2	17	18	SAM_A1	V7
-	**2.5V**	19	20	SAM_A3	W5
F5	SAM_D0	21	22	**2.5V**	**-**
V6	SAM_D2	23	24	SAM_D1	U7
U6	SAM_D4	25	26	SAM_D3	U5
T7	SAM_D6	27	28	SAM_D5	T5
R7	SAM_D8	29	30	SAM_D7	R6
P6	SAM_D10	31	32	SAM_D9	R5
N6	SAM_D12	33	34	SAM_D11	P8
K5	SAM_D14	35	36	SAM_D13	M7
K6	SAM_A4	37	38	SAM_D15	L7
J6	SAM_A6	39	40	SAM_A5	J5
H4	SAM_IRQ	41	42	**GND**	**-**
H6	SAM_RESET#	43	44	SAM_CE#	G4
-	FPGA_DONE	45	46	SAM_BRDY	G5
-	FPGA_CCLK	47	48	FPGA_D_IN	-
-	**GND**	49	50	**GND**	**-**

Table 17 - SAM Interface Signals

2.7.3 JTAG Port (PC4)

The Virtex-5 FXT Evaluation Board provides a JTAG port (PC4 type) connector (J9) for configuration of the FPGA. The following figure shows the pin assignments for the PC4 header on this development board.

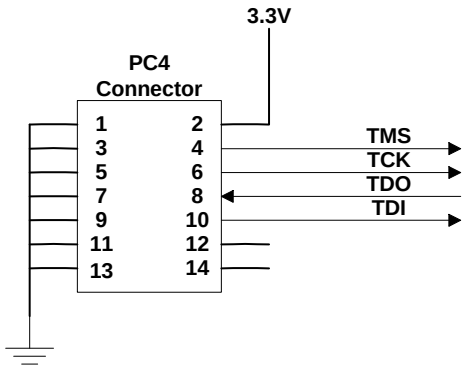


Figure 10 - PC4 JTAG Port Connector

2.7.4 CPU Debug Port

The Virtex-5 FXT Evaluation Board provides a CPU Debug header for connection of a debug probe to the integrated PowerPC processor.

CPU Debug connector JP4 can be used to download code into the Virtex-5 FXT integrated PowerPC processor. The JTAG port can also be used as the processor debug port. The FPGA general-purpose I/O pins are used for this interface. The following figure shows the CPU Debug Connector.

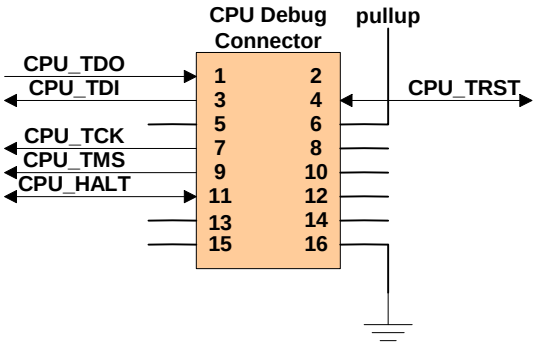


Figure 11 - CPU Debug Connector

2.7.5 CPU Trace Port

The Virtex-5 FXT Evaluation Board provides a CPU Trace header for connection of a trace probe to the integrated PowerPC processor. The FPGA general-purpose I/O pins are used for this interface.

The processor uses the trace interface when operating in real-time trace-debug mode. Real-time trace-debug mode supports real-time tracing of the instruction stream executed by the processor. In this mode, debug events are used to cause external trigger events. An external trace tool uses the trigger events to control the collection of trace information. The broadcast of trace information on the trace interface occurs independently of external trigger events (trace information is always supplied by the processor). Real-time trace-debug does not affect processor performance. The following figure shows the CPU Trace connector on the Virtex-5 FXT Evaluation Board.

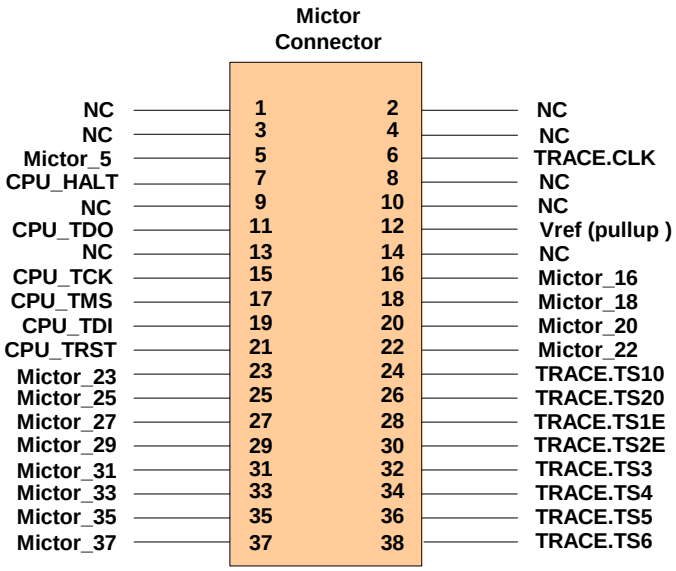


Figure 12 - CPU Trace Connector

2.8 Power

The Virtex-5 FXT Evaluation Board power is developed from a +5V input provided by the external 5V 2.5A wall outlet transformer. The transformer cable plugs into the board at the barrel connector labeled "J11". The +3.3V, +2.5V, and +1.0V power rails are developed by TI PTH series adjustable power modules. The DDR2 +0.9V DDR2 termination and +1.8V supply/reference voltages are supplied by a Texas Instruments TPS51116 regulator sourced by the board's 5.0V rail. The following figure shows a high-level block diagram of the main power supply on the Virtex-5 FXT Evaluation Board.

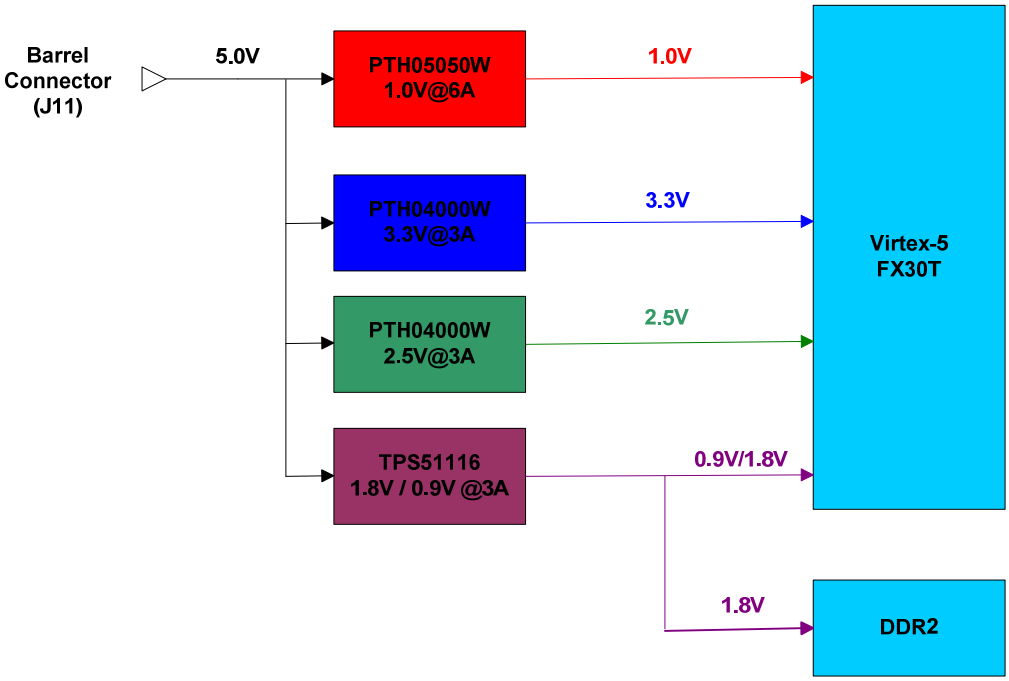


Figure 13 - Virtex-5 FXT Evaluation Board Power

2.8.1 FPGA I/O Voltage (Vcco)

All FPGA bank voltages are preset to specific I/O levels with the exception of Banks 4, 16 and 18. Those banks are used for the EXP expansion connector which is utilizes selectable voltages of either 2.5V or 3.3V for both the single ended signals and the differential pair signals. A user can select which voltage to use for each type of signals. It is important to note however, that the Virtex-5 family of FPGAs requires 2.5V bank voltage to utilize differential pair signaling. Bank 18 is fully utilized with differential pair signals that can also be used as single ended I/O if the user wishes. All fixed voltage I/O that is wired to a selectable voltage bank uses voltage translators to convert those signals to the proper bank voltage. Below is a table that shows the bank voltages for each bank on the V5FX30T FPGA.

Bank #	1.8V	2.5V	3.3V	Selectable Rail
0			X	-
1			X	-
2			X	-
3			X	-
4		X	X	VIO_EXP1_DP **(JP2)**
11	X			-
12			X	-
13	X			-
15			X	-
16		X	X	VIO_EXP1_SE **(JP3)**
17	X			-
18		X	X	VIO_EXP1_DP **(JP2)**

Table 18 - V5FX30T I/O Bank Voltages

2.8.2 FPGA Reference Voltage (Vref)

The Virtex-5 FXT Evaluation Board provides the reference voltage of +0.9V to FPGA banks 11, 13, and 17, all of which are connected to DDR2 memory signals.

2.9 Expansion Connectors

The Virtex-5 FXT Evaluation Board provides expansion capabilities for customized user application daughter cards and interfaces over one EXP expansion connector. The EXP expansion connector on the board can support one half-card EXP module. Both off-the-shelf EXP modules and user-developed modules can easily be plugged onto the Virtex-5 FXT Evaluation Board to add features and functions to the backend application of the main board. For more information, view the EXP specification at www.em.avnet.com/exp.

2.9.1 EXP Interface

The EXP specification defines a 132-pin connector, with 24 power, 24 grounds, and 84 user I/Os. The standard EXP configuration implemented on the Virtex-5 FXT Evaluation Board uses one EXP connector (Samtec part number QTE-060-09-F-D-A), for a total of 84 user I/Os. Using jumpers, you can set the voltage levels for the EXP user I/O to either 2.5V or 3.3V. As shown in the following figure, "JP2" sets the I/O voltage for the EXP connector's differential signals and "JP3" sets the I/O voltage for the EXP connector's single ended signals.

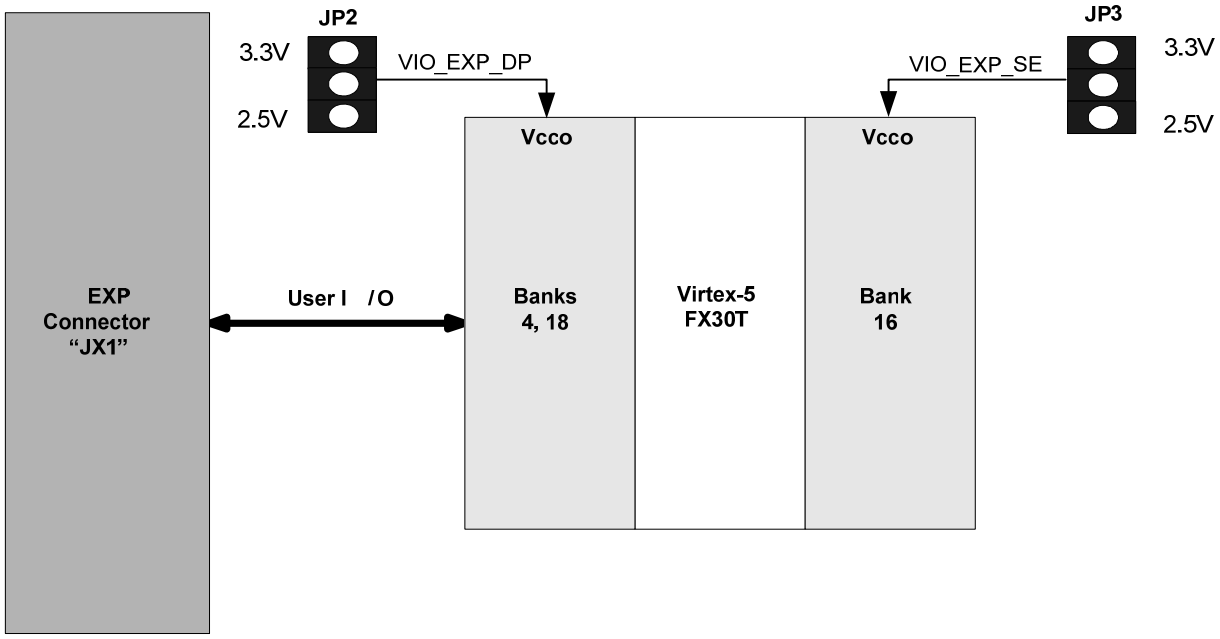


Figure 14 - EXP I/O Voltage Jumpers

The EXP specification defines four user signal types: Single Ended I/O, Differential I/O, Differential and Single Ended Clock Inputs, and Differential and Single Ended Clock Outputs. Because the FPGA I/Os can be configured for either single-ended or differential use, the differential I/Os defined in the EXP specification can serve a dual role. All the differential I/O signals can be configured as either differential pairs or single-ended signals, as required by the end application. In providing differential signaling, higher performance LVDS interfaces can be implemented between the baseboard and EXP module. Connection to high speed A/Ds, D/As, and flat panel displays are possible with this signaling configuration. Applications that require single-ended signals only can use each differential pair as two single-ended signals, for a total of 84 single-ended I/O per connector.

Net Names	Signal Description	Pins per Connector
EXP1_SE_IO	Single-ended I/O	34
EXP1_SE_CLK_IN	Single-ended clock input	1
EXP1_SE_CLK_OUT	Single-ended clock output	1
EXP1_DIFF_p/n	Differential I/O pairs	21*
EXP1_DIFF_CLK_IN_p/n	Differential clock input pair, global	1
EXP1_DIFF_CLK_OUT_p/n	Differential clock output pairs	1
EXP1_RCLK_DIFF_p/n10	Differential clock input pair, regional	1*
Total		84

Table 19 - EXP Connector Signals

* Since the Virtex-5 FPGA supports regional clocking, the optional RCLK pair defined in version 1.2 of the EXP specification is utilized reducing the number of output-capable differential pairs from 22 down to 21.

The Virtex-5 FPGA user I/O pins that connect to the EXP connector is shown in the following table. The Samtec QTE connector plug on the Virtex-5 FXT Evaluation Board (part number: QTE-060-09-F-D-A) mates with the Samtec QSE high-performance receptacles (part number: QSE-060-01-F-D-A), located on the daughter card. Samtec also provides several high-performance ribbon cables that will mate to the "JX1" connector.

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Virtex-5 Pin	Net Name	EXP Connector Pin # (JX1)		Net Name	Virtex-5 Pin
A8	EXP1_SE_IO_0	2	1	EXP1_SE_IO_1	A12
B10	EXP1_SE_IO_2	4	3	EXP1_SE_IO_3	A10
-	**2.5V**	6	5	**2.5V**	-
B9	EXP1_SE_IO_4	8	7	EXP1_SE_IO_5	A9
A5	EXP1_SE_IO_6	10	9	EXP1_SE_IO_7	B11
-	**2.5V**	12	11	**2.5V**	-
B6	EXP1_SE_IO_8	14	13	EXP1_SE_IO_9	A7
D8	EXP1_SE_IO_10	16	15	EXP1_SE_IO_11	C9
-	**2.5V**	18	17	**2.5V**	-
B7	EXP1_SE_IO_12	20	19	EXP1_SE_IO_13	A4
B5	EXP1_SE_IO_14	22	21	EXP1_SE_IO_15	C8
-	**2.5V**	24	23	**2.5V**	-
C7	EXP1_SE_IO_16	26	25	EXP1_SE_IO_17	A3
C6	EXP1_SE_IO_18	28	27	EXP1_SE_IO_19	B4
-	**2.5V**	30	29	**2.5V**	-
D6	EXP1_SE_IO_20	32	31	EXP1_SE_IO_21	D9
E8	EXP1_SE_IO_22	34	33	EXP1_SE_IO_23	D5
-	**2.5V**	36	35	**2.5V**	-
F7	EXP1_SE_IO_24	38	37	EXP1_SE_IO_25	E7
E5	EXP1_SE_IO_26	40	39	EXP1_SE_IO_27	E6
AB14	EXP1_DIFF_CLK_IN_p	42	41	EXP1_SE_IO_28	F8
AC14	EXP1_DIFF_CLK_IN_n	44	43	EXP1_SE_CLK_IN	E10
-	**GND**	46	45	**GND**	-
G7	EXP1_SE_IO_30	48	47	EXP1_SE_IO_29	H7
H8	EXP1_SE_IO_31	50	49	EXP1_SE_CLK_OUT	B12
-	**GND**	52	51	**GND**	-
W9	EXP1_DIFF_p20	54	53	EXP1_DIFF_p21	V8
W8	EXP1_DIFF_n20	56	55	EXP1_DIFF_n21	V9
-	**GND**	58	57	**GND**	-
AB19	EXP1_DIFF_p18	60	59	EXP1_SE_IO_32	G9
AC19	EXP1_DIFF_n18	62	61	EXP1_SE_IO_33	J8
-	**GND**	64	63	**GND**	-
AA7	EXP1_DIFF_p16	66	65	EXP1_DIFF_p19	Y7
AA8	EXP1_DIFF_n16	68	67	EXP1_DIFF_n19	Y8
-	**GND**	70	69	**GND**	-
AC18	EXP1_DIFF_CLK_OUT_p	72	71	EXP1_DIFF_p17	AA5
AB17	EXP1_DIFF_CLK_OUT_n	74	73	EXP1_DIFF_n17	AB5
-	**GND**	76	75	**GND**	-
AB9	EXP1_DIFF_p14	78	77	EXP1_DIFF_p15	AC12
AA9	EXP1_DIFF_n14	80	79	EXP1_DIFF_n15	AC13
AD6	EXP1_DIFF_p12	82	81	EXP1_DIFF_p13	AE5
AC7	EXP1_DIFF_n12	84	83	EXP1_DIFF_n13	AD4
-	**3.3V**	86	85	**3.3V**	-
AB6	EXP1_RCLK_DIFF_p10	88	87	EXP1_DIFF_p11	AC6
AB7	EXP1_RCLK_DIFF_n10	90	89	EXP1_DIFF_n11	AD5
-	**3.3V**	92	91	**3.3V**	-
AD9	EXP1_DIFF_p8	94	93	EXP1_DIFF_p9	AE6
AC9	EXP1_DIFF_n8	96	95	EXP1_DIFF_n9	AF5
-	**3.3V**	98	97	**3.3V**	-
AE8	EXP1_DIFF_p6	100	99	EXP1_DIFF_p7	AC8
AE7	EXP1_DIFF_n6	102	101	EXP1_DIFF_n7	AD8
-	**3.3V**	104	103	**3.3V**	-
AF4	EXP1_DIFF_p4	106	105	EXP1_DIFF_p5	AD10
AF3	EXP1_DIFF_n4	108	107	EXP1_DIFF_n5	AE10
-	**3.3V**	110	109	**3.3V**	-
AF7	EXP1_DIFF_p2	112	111	EXP1_DIFF_p3	AE11
AF8	EXP1_DIFF_n2	114	113	EXP1_DIFF_n3	AD11
-	**3.3V**	116	115	**3.3V**	-
AF9	EXP1_DIFF_p0	118	117	EXP1_DIFF_p1	AF12
AF10	EXP1_DIFF_n0	120	119	EXP1_DIFF_n1	AE12
-	**GND**	122	121	**GND**	-
-	**GND**	124	123	**GND**	-
-	**GND**	126	125	**GND**	-
-	**GND**	128	127	**GND**	-
-	**GND**	130	129	**GND**	-
-	**GND**	132	131	**GND**	-

Table 20 - EXP Connector "JX1" Pin-out

3.0 Test Designs

This section describes the factory test design that is pre-programmed into the Intel P30 BPI Flash. This design is used to verify some of the functionality of the board. The remaining production tests are not included with the kit but may be downloaded at the Avnet DRC website: www.em.avnet.com/drc.

If the flash has been erased, the MCS file containing the test design is available on the Design Resource Center web site: www.em.avnet.com/drc. To program, add a BPI UP flash to the V5FX30T device in Impact. Select the factory test .mcs file you wish to program into the flash and select the program option after right clicking on the newly added BPI device. Make sure JP5 has the jumper placed in the 1-2 position so that the FPGA will configure in BPI mode.

Jumper Setting to Enable BPI Configuration: JP5 : 1-2

All factory test designs use a terminal session as the user interface. Using a straight-through serial cable, connect the Virtex-5 FXT Evaluation Board to a PC. Open a terminal session and configure it for 19200 baud, 8 data bits, no parity, 1 stop bit and no flow control (19200-8-N-1-N). Turn on power to the board at SW7 and the Avnet Factory Test banner will display in the Terminal session.

Other test designs that are available the Avnet DRC website are the Ethernet test and the USB UART test. Below are the descriptions of what each test performs.

3.1 Factory Test

The Factory Test verifies the electrical connectivity of the DDR SDRAM, Flash memory, the user LEDs, and the switches. The user can initiate the tests by typing 'test <enter>' in a terminal session configured as 19200-8-N-1-N. Some of the tests require user inputs and observation (watching the LEDs and pressing the switches). The cumulative results are displayed at the completion of test processes.

3.2 Ethernet Test

The Ethernet Test design provides the user with the ability to ping the Virtex-5 FXT Evaluation Board to verify network connectivity via the on-board National 10/100/1000 Mbps Ethernet PHY. The National PHY supports auto-MDIX mode, which allows either a straight-through or a cross-over Ethernet cable to be used. The default IP address of the board is 172.16.158.147. To ping the board, plug an Ethernet cable from the wall into the RJ45 connector labeled "J1". Then change the IP address of the board to match the subnet of a PC or network it's connected to using a terminal program configured as 19200-8-N-1-N. At the prompt, type 'i' and then enter the new IP address for the board (first three fields must match the IP address of the PC: MMM.MMM.MMM.xxx; the last field must be different). Use periods '.' between fields and hit the <enter> key when finished. Then open a command shell on the PC (Start Menu -> Run, cmd) and type 'ping MMM.MMM.MMM.xxx'. You should see four replies to the ping request.

3.3 USB UART Test

This test requires that the Silicon Labs CP2102 device drivers be installed on the test PC. Those drivers are available on the Avnet DRC website: www.em.avnet.com/drc. This test design is a replica of the standard factory test with the only difference being the USB UART is being used as the std_in and std_out RS232 device. If the drivers for the CP2102 are installed correctly and the board is powered on with the USB cable connected between the PC and the Virtex-5 FXT Evaluation Board the device will show up in the Device Manager of the PC as a COM port. The terminal session settings must use the corresponding COM port for the CP2102 in order to use this interface.

4.0 Revisions

V1.0	Initial release for production board (BD-V5FXT-EVL30-G)	May 20th, 2008

Appendix A

This section provides a description of the jumper settings for Virtex-5 FXT Evaluation Board. The board is ready to use out of the box with the default jumper settings. The following figure depicts a map of the component side of the board with Jumper/Header/Connector locations detailed.

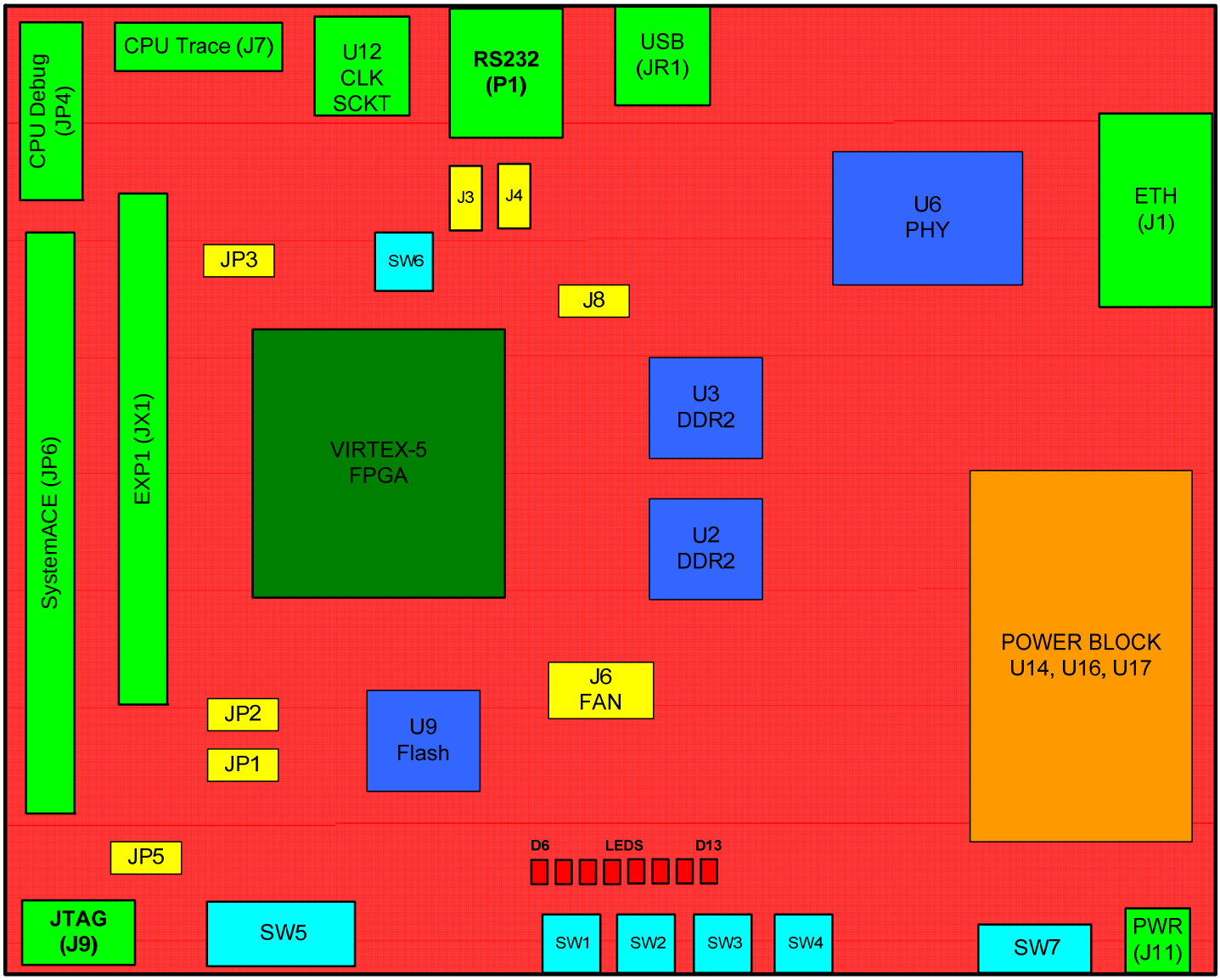

Figure 15 - Virtex-5 FXT Evaluation Board Placement

JP1 "FLASH WP" – Flash Write-protect Enable, install a shunt across pins 2-3 to protect programmed data in the Flash memory. Default: 1-2, read/write enabled (unprotected).

JP2 "VIO1 DP" – Vcco select for banks 4 and 18. These are the banks that have all of the EXP differential pair signals connected to them. If differential signaling is to be used for signals, this jumper must be set in the 2-3 position. If these signals are to be used as single ended signals either the 2.5V or 3.3V setting may be used. Default: position 2-3, 2.5V.

JP3 "VIO1 SE" – Vcco select for bank 16. All EXP single ended signals are connected to this bank. Jumper position 1-2 selects 3.3V while jumper position 2-3 selects 2.5V. Default: position 2-3, 2.5V.

JP5 "BPI/JTAG" – Enable either BPI configuration mode or JTAG configuration mode. Default: 1-2, BPI configuration.

J3 “RTS” – Install a shunt to connect the second RX port of the RS232 transceiver to the DB9 connector for hardware handshaking. This can be used to implement the ready to send (RTS) signal. Default: Open.

J4 “CTS” – Install a shunt to connect the second TX port of the RS232 transceiver to the DB9 connector for hardware handshaking. This can be used to implement the clear to send (CTS) signal. Default: Open

J6 “FAN” – A three pin header that allows the user to connect a 5V active heat sink or fan to help cool the FPGA if needed. Pins 1 and 3 are GND, Pin 2 supplies 5V.

J8 “HSWAP” - Enables pull-ups on the Virtex-5 I/O pins during configuration. Install a jumper to enable the configuration pull-ups. Default: Open; pull-ups disabled.

SW6 “RECFG” - Pressing SW6 forces the FPGA to reconfigure itself. This feature will only work when the FPGA is set to configure in BPI mode and a valid FPGA image is stored in the flash.